2021 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2021)

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2021 IEEE Conference on Postgraduate Research in Microelectronics and Electronics (PRIMEASIA 2021)

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Message From the General Chair

On behalf of the Organizing Committee, we would like to welcome all participants to Virtual IEEE Asia Pacific Conference Circuit and System (APCCAS2021) and IEEE Asia Pacific Conference on Postgraduate Research in Mircroelectronic and Electronic (PrimeAsia2021) held in Park Royal Hotel Penang , Malaysia from 23rd to 25th November 2021. The theme of the conference is "**Intelligent Technology and Innovations for Sustainable Society**". The objective of the APPCAS 2021 is to share the latest research in the areas related to circuit and system. PrimeAsia 2021 aims to provide opportunity for postgraduate students (Masters and PhD) to present their research work and to interact with scientists and engineers in the research community and industry. It is expected that this conference will enable interactive discussions and exchange ideas among attendees and forge further meaningful collaborations.

APCCAS&PrimeAsia is proud of having distinguished keynote speakers: Professor Dr. Akinori Konno (Shizuoka University), 2. Professor Dr. Shimeng Yu (Georgia Institute of Technology), Professor Dr. Harikrishnan Ramiah (University Malaya), Mr. Ikura Masami (Former Toyota Tsuho Nexty Electronics, Research Fellow Prince of Songkla University), Professor Dr. Massimo Alioto (National University Singapore), Prof Pui-In (Elvis) Mak (University of Macau), Chip Hong Chang (Online) (National Technical University, Singapore), Mr Suresh (VP of Design Center, Intel Malaysia) and Dr Bo Chen, (Cadence Malaysia/Singapore). We would like to thank them for their presence here and their contributions.

APCCAS&PrimeAsia 2021 will not be a successful conference without the submission of technical papers from researches who have invested their time and energy writing on a variety of topics, which includes Analog and Mixed Signal Circuits and Systems, Digital Circuits and System, Power/Energy Devices, Circuits and Systems, Communication Circuits and System, Internet of Things Circuits and Systems, Imaging System and Technologies, High Speed and Optical Wire lined Circuits and Systems, Biomedical and Healthcare Circuits and Systems, Digital Signal Processing, Artificial Intelligent Circuits and Systems, Nano electronics, Devices and System Integration, Signal Processing, Control and Communications, Multimedia Systems and Applications, Education in Circuits and Systems, RF Integrated Circuit Design and Energy Harvesting, Integrated Power Management Unit (PMU), Gerontology Circuits and Systems and Automotive Circuits and Systems. Thus, we would like to thank all authors for supporting APCCAS&PrimeAsia 2021 and wish you a fruitful discussion. The technical program committee members and external reviewers also deserved a pat on the back for a job well done reviewing the submitted papers whilst maintaining high standard of quality for this conference. APCCAS2021 also would like to congratulate those papers which has been accepted for TCASI and TCASII journal publication.

Finally, APCCAS&PrimeAsia 2021would not be possible without the dedicated work and efforts of the organizing committee and its volunteers who worked tirelessly in every aspect. We wish to express our gratitude for your hard work and commitment towards making APCCAS&PrimeAsia 2021a success. Thank you.

Wan Zuha Wan Hasan, *PhD SMIEE*
Professor
General Chair
APCCAS2021 and PrimeAsa2021

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Dye Sensitized Solar Cell	Mohd Amrallah Mustafa	Universiti Putra Malaysia
Ultra-Low-Power and agile IC design: towards battery-less and low-cost distributed sensing	Nasri Sulaiman	Universiti Putra Malaysia
Tutorial: Radio over IP Embedded System	Tang Tong Boon	Universiti Teknologi PETRONAS
CMOS Device Modeling	Lini Lee	Multimedia University

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Keynote 7: Towards Energy-Autonomous Bluetooth-Low-Energy Radios for IoT Applications	Nasri Sulaiman	Universiti Putra Malaysia
Keynote 8: Security of Edge AI – A new challenge to deep learning accelerators	Asral Bahari Jambek	Universiti Malaysia Perlis,
Keynote 9: Technology as an Enabler For Sustainable Growth – The Opportunity Ahead	Kalai Selvan Subramaniam	Infinecs Systems Sdn. Bhd

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Electronic Design Automation & High Speed and Optical Wire lined Circuits and Systems	Kalai Selvan Subramaniam	Infinecs Systems Sdn. Bhd
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Digital Circuits and Systems 2	Kwen Siong Chong	Zero-Error Systems Pte Ltd (S)
Power/Energy Devices, Circuits and Systems & Integrated Power Management Unit (PMU)	Yongfu Li	Shanghai Jiao Tong University
Tutorial: Ultra-Low-Power and agile IC design: towards battery-less and low-cost distributed sensing	Kyung Ki Kim	Daegu University, South Korea
Imaging System and Technologies & Multimedia Systems and Applications	Tutun Juhana	Institut Teknologi Bandung, Bandung, Indonesia
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Keynote Speakers

Keynote 1: Development of Pre-dyed Dye-sensitized and Perovskite Solar Cells

Akinori Konno
Professor,
Graduate School of Science and Technology,
Shizuoka University, Hamamatsu, Japan

Abstract:

Developing highly efficient and low-cost solar cells as an alternative to conventional silicone solar cell has been attracted much interest. In this regard, the dye-sensitized solar cell (DSC) has been intensively studied as a promising system due to its reasonably high energy conversion efficiency and its much lower fabrication cost. We reported the pre-dye method based on dye-sensitized solar cells (DSCs) of ZnO compact layer has been fabricated on transparent conducting oxide glass and plastic polymer substrates at low temperature. Plastic substrate because of the low heat resistance, cannot undertake high temperature calcination.In order to improve lower porosity and bad interparticle connectivity, hot-press method was applied to plastic substrate photoelectrode. The results demonstrate that the compact layer can effectively reduce the short circuit from transparent conducting oxide to electrolyte in dye-sensitized solar cells, leading to an increase of open-circuit photovoltage, and the power conversion efficiency. Also, in order to increase conversion efficiency, one of important points is how to enhance absorption of photon in wide wavelength region. The research showed two different kinds of pigments which have been mixed to improve absorption band.[1] In addition to DSCs, perovskite solar cells (PSCs) have been developed intensively because of rapid increase in its efficiency.[2] We have also developed PSCs using CuI as a hole transport material. In early studies, application of CuI to PSC gave only poor efficiencies (1-2 %). Recently remarkable improvement has been achieved by introducing carbon nanotube into CuI layer. The contact between perovskite and CuI seems to play essential role for fabricating efficient PSCs.

Biodata

1988 Ph.D. Graduate School of Science, Tohoku University
1988-1996 Assistant Professor at Graduate School of Science and Engineering, Tokyo Institute of Technology
1996-2009 Associate Professor at Faculty of Engineering, Shizuoka University
2009- Professor at Faculty of Engineering, Shizuoka University

Keynote 2: Radio Frequency Energy Harvesting for Healthcare Wearable

Harikrishnan Ramiah
Associate Professor,
University Malaya, Malaysia

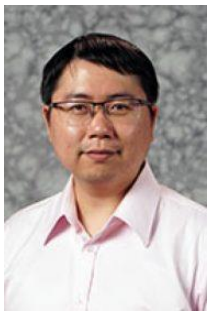
Abstract:

The use of the wearable device for human as well as domestic/wildlife animals for the continuous monitoring of health care will facilitate the involvement of the patients in the prevention, management of chronic diseases, even for pandemic and post-pandemic situations. So that wearable devices have huge market potential in upcoming days, but their usage has been limited due to frequent powering up of such devices is still a challenge. Batteries are the most widespread solution but add size, weight is unattractive to humans and periodic recharging is not possible for wildlife animals. However, the widespread adoption of these devices depends very much on their ability to operate for long periods without the need to frequently change, recharge, or even use batteries. In this context, energy harvesting (EH) is a disruptive technology that can pave the road towards the massive utilization of wireless wearable sensors for patient self-monitoring and daily healthcare. Radio-frequency (RF) transmissions from commercial telecommunication networks represent reliable ambient energy that can be harvested as they are ubiquitous in urban and suburban areas. The state-of-the-art in RF EH for wearable devices specifically targeting the global system of mobile 900/1800 cellular, 700 MHz digital terrestrial television networks, and Wi-Fi coverage as ambient RF energy sources are showcased. Furthermore, Limitations, challenges, and design considerations of fully integrated RF energy harvester are presented, which is useful for other researchers that work in the same area. The author will deliver recent advances towards the development of an efficient RF energy harvester and thorough ideas for the future development of RFEH.

Biodata

Harikrishnan Ramiah is currently an Associate Professor at Department of Electrical Engineering, University of Malaya, working in the area of RFIC/RFEH design. He received his B.Eng(Hons), MSc and PhD degrees in Electrical and Electronic Engineering, in the field of Analog and Digital IC design from Universiti Sains Malaysia in 2000, 2003 and 2008 respectively. In the year 2003, he was with SiresLabs Sdn. Bhd, CyberJaya, Malaysia. At the year 2002 he was attached to Intel Technology Sdn. Bhd. Harikrishnan was the recipient of Intel Fellowship Grant Award, 2000-2008.
Harikrishnan is the Director of the Centre of Industry Reserch 4.0 (CRI 4.0) and the Head of Analog, Digital & RF Research group at University of Malaya. His work revolves in providing expert solution to industry in the strength of IR 4.0. Through CRI 4.0, he regulates expert collaborative effort of the faculties in University of Malaya outsourcing solution to SME and MNC. He had produced silicon verified IPs in the field of Analog, RF and RFEH Integrated Circuit Design. With a reputable research output and solution, he has secured several international, national and industrial grant from the year 2014 till date. He serves as an Associate Editor of IEEE Access in a recognition towards his research credibility. He is a Chartered Engineer and the Fellow of Institute of Electrical Technology (IET). He is also a Professional Engineer registered under the Board of Engineers, Malaysia. He is a Senior Member of the Institute of Electrical and Electronics Engineer (IEEE) and member of The Institute of Electronics, Information and Communication Engineers (IEICE). His research work has resulted in several reputable technical publications in the field of Electrical & Electronics Engineering. His main research interest includes Analog Integrated Circuit Design, RFIC Design, VLSI system design and RF/Piezoelectric/Thermal/Electromagnetic Energy Harvesting Power Management Module Design.

Keynote 3: RRAM for Compute-in-Memory: From Inference to Training



Shimeng Yu
Associate Professor,
School of Electrical and Computer Engineering,
Georgia Institute of Technology

Abstract:

To efficiently deploy machine learning applications to the edge, compute-in-memory (CIM) based hardware accelerator is a promising solution with improved throughput and energy efficiency. Instant-on inference is further enabled by emerging non-volatile memory technologies such as resistive random access memory (RRAM). This presentation reviews the recent progresses of the RRAM based CIM accelerator design. First, the multilevel states RRAM characteristics are measured from a test vehicle to examine the key device properties for inference. Second, a benchmark is performed to study the scalability of the RRAM CIM inference engine and the feasibility towards monolithic 3D integration that stacks RRAM arrays on top of advanced logic process node. Third, grand challenges associated with in-situ training are presented. To support accurate and fast in-situ training and enable subsequent inference in an integrated platform, a hybrid precision synapse that combines RRAM with volatile memory (e.g. capacitor) is designed and evaluated at system-level. Prospects and future research needs are discussed.

Biodata

Shimeng Yu is currently an associate professor of electrical and computer engineering at Georgia Institute of Technology. He received the B.S. degree in microelectronics from Peking University in 2009, and the M.S. degree and Ph.D. degree in electrical engineering from Stanford University in 2011 and 2013, respectively. From 2013 to 2018, he was an assistant professor at Arizona State University. Prof. Yu's research interests are the semiconductor devices and integrated circuits for energy-efficient computing systems. His research expertise is on the emerging non-volatile memories for applications such as deep learning accelerator, in-memory computing, 3D integration, and hardware security. Among Prof. Yu's honors, he was a recipient of NSF Faculty Early CAREER Award in 2016, IEEE Electron Devices Society (EDS) Early Career Award in 2017, ACM Special Interests Group on Design Automation (SIGDA) Outstanding New Faculty Award in 2018, Semiconductor Research Corporation (SRC) Young Faculty Award in 2019, ACM/IEEE Design Automation Conference (DAC) Under-40 Innovators Award in 2020, and IEEE Circuits and Systems Society (CASS) Distinguished Lecturer for 2021-2022, etc. He is a senior member of the IEEE.

Keynote 4: New issues and proposals for new technology development seen from application examples of AI + CONNECTED technology for automotives

Mr. Masami Ikura
Former Toyota Tsusho Nexty Electronics, Thailand
Research Fellow,
Faculty of Electronics Engineering, Prince of Songkla University, Thailand

Abstract:

Innovative new technologies such as AR, 5G, and artificial intelligence are being applied and applied to the consumer, industry, automotive, and medical markets without restrictions. Looking on an automotive industry, it has just started to be applied to private cars one after another, but it is also being applied to commercial vehicles by on-time logistics, multimodal, real-time asset monitoring, etc., and it is expanding more and more. In the automotive market, which supports people's lives with the keywords of safety and security, "AI + CONNECTED" has begun to be put into practical use. Optimal route search algorithms using artificial intelligence used for these, technologies for improving processing performance, and communication networks Remote monitoring / remote update in cooperation with, and test methods that previously required a huge amount of time are now being adopted more and more in other fields. On the contrary, it is expected that the development efficiency and quality assurance will be improved by incorporating the semiconductor technology of advanced information processing system, security field, and consumer / industrial into the in-vehicle system. In this lecture, we will introduce an example of applying communication / artificial intelligence technology for automotives to the industrial world based on the above situation, and it may happen in the future that was found in the case from the standpoint of an ASIC / FPGA semiconductor designer. We describe the limits of possible technological development and the future prospects for new technological development in terms of hardware and software.

Biodata

Masami IKURA received the master degree in Embedded System of Tellecommunication engineering faculty from the TOKAI University in 2010. He is also a research fellow at Prince Of Songklar University in Thailand, now. His working background is focus a hardware design since 1990. Currenty, he works for TOYOTA TSUSHO NEXTY ELECTRONICS THAINALND CORP,.LTD. Also his responsible for a Chief Technology Officer. He is also a techical publish editor of an ASIC/FPGA principal design in the Embedded System hardware/firmware. His publishment is widely introduced in internet, AMAZON and so on. He is concentrated to technical business planning for the AI and CONNECTED markets with reference to automotive electronics technology. A very important task under a NEW-NORMAL environment, he is leading an AI-FPGA edge computing systems in industrial market with Prince Of Songklar University and his in-house research team.

Keynote 5:Intelligent Systems with Ultra-Wide Power-Performance Adaptation - Going Well beyond the Diminishing Returns of Voltage Scaling

Massimo Alioto
Professor,
National University of Singapore

Abstract:

Wide power-performance adaptation has become crucial in always-on nearly real-time and energy-autonomous SoCs that are subject to wide variability in the power availability and the performance target, as required by applications such as AI, vision and audio cognition. Wide adaptation is indeed a prerequisite to assure sustained operation in spite of the widely fluctuating energy/power source, and to grant swift response upon the occurrence of events of interest (e.g., on-chip data analytics), while maintaining extremely low consumption in the common case. These requirements have led to a strong demand for SoCs having an extremely wide performance-power scalability and adaptation, which vastly exceeds the capabilities of conventional wide voltage scaling. In this talk, recent directions to drastically extend the performance-power scalability of digital, analog and power management circuits and architectures are presented. Silicon demonstrations of better-than-voltage-scaling adaptation to the workload are illustrated for the data path, the clock path and the memory sub-system. Several silicon demonstrations are presented for accelerators, processors and SRAMs with enhanced peak performance above traditionally allowed at nominal voltage, yet at reduced minimum energy. Energy-quality scaling is explored as additional dimension to break the conventional performance-energy tradeoff in error-resilient applications such as AI and vision, from networks on chip to memories and accelerators. Further performance and energy improvements are discussed through uncommonly flexible in-memory broad-purpose computing frameworks for true data locality, from buffering to signal conditioning and neural net workloads. Finally, challenges and opportunities for the decade ahead are discussed to enable a new generation of always-on intelligent systems with divergently high peak performance and low minimum power.

Biodata

Massimo Alioto is a Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, and is the Director of the Integrated Circuits and Embedded Systems area and the FD-FAbrICS research center on intelligent&connected systems. He held positions at the University of Siena, Intel Labs CRL, University of Michigan Ann Arbor, University of California Berkeley, EPFL - Lausanne.

He is (co)author of 300 publications on journals and conference proceedings, and four books with Springer. His primary research interests include ultra-low power circuits and systems, self-powered integrated systems, near-threshold circuits for green computing, widely energy-scalable integrated systems, circuits for machine intelligence, hardware security, and emerging technologies.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems, Distinguished Lecturer for the IEEE Solid-State Circuits Society, and was Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. Previously, Prof. Alioto was the Chair of the “VLSI Systems and Applications” Technical Committee of the IEEE Circuits and Systems Society (2010-2012), as well as Distinguished Lecturer (2009-2010) and member of the Board of Governors (2015-2020).

Keynote 6:The State-of-the-Art and Next Generation Simulation Technologies for Analog, Mixed-Signal and Memory Design

Dr Bo Chen
Cadence, Singapore

Abstract

With the modern and most advanced semiconductor process technologies, the circuit design complexity and the device count on a single chip have been increased tremendously, far beyond the reach of the traditional SPICE technology. Over the years, Cadence has developed the state-of-the-art technologies from the distributed simulation including the multi-threading and cloud infrastructure to parasitics optimized for large postlayout design, the partition-based FastSpice technology for memory simulation as well as IEEE-1801-based mixed-signal simulation methodology for low power design. In this session, an overview on how current Cadence simulation technologies address the design challenges will be introduced and the best practices for verifying mixed-signal design will be briefed.

Biodata

Dr Chen graduated from National University of Singapore with Ph.D in electrical engineering. Before joining Cadence Design Systems as an application engineer, he was a device modeling engineer and circuit design engineer in a few companies developing from RFIC products to optical transceiver. Together with his colleagues, he has been helping all Cadence customers across south east Asia to adopt Cadence technologies, such as Intel, Infineon, MediaTek, GlobalFoundries and Silterra, et al. With nearly twenty years of Cadence working experience, Dr Chen is familiar with the custom IC design methodologies with the focus on the analog, mixed-signal and RF simulation technologies and products.

Keynote 7: Towards Energy-Autonomous Bluetooth-Low-Energy Radios for IoT Applications

Pui-In (Elvis) Mak
Professor,
University of Macau, China

Abstract:

This talk overviews the motivation, challenges and solutions of realizing energy-harvesting Bluetooth Low-Energy (BLE) receiver and transmitter in 28-nm CMOS; both are the key enablers of energy-autonomous IoT devices. They feature a fully-integrated micropower manager to customize the internal supply and bias voltages for both active and sleep modes. Circuitries enabling sub-0.3V operation are introduced for the low-noise amplifier (LNA), voltage-controlled oscillator (VCO), phased-locked loop (PLL) and power amplifier (PA).

Biodata

Pui-In (Elvis) Mak received the Ph.D. degree from University of Macau (UM), Macao, China, in 2006. He is currently Full Professor at UM Faculty of Science and Technology – ECE, and Deputy Director at the UM State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests are on analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations. He is currently the Associate Editor of IEEE Journal of Solid-State Circuits (’18-) and IEEE Solid-State Circuits Letters (’17-). He is/was the TPC Member of A-SSCC (’13-’16), ESSCIRC (’16-’17) and ISSCC (’17-’19). He is/was Distinguished Lecturer of IEEE Circuits and Systems Society (’14-’15) and IEEE Solid-State Circuits Society (’17-’18). He was inducted as an Overseas Expert of the Chinese Academy of Sciences since 2018. He is a Fellow of the IEEE, IET and RSC.

Keynote 8: Security of Edge AI – A new challenge to deep learning accelerators

Chip Hong Chang, Associate Professor, Nanyang Technology University (NTU) of Singapore

Chip Hong Chang
Associate Professor,
Nanyang Technology University (NTU) of Singapore

Abstract:

The flourishing of Internet of Things (IoT) has rekindled on-premise computing to allow data to be analyzed closer to the source. To support edge Artificial Intelligence (AI), hardware accelerators, open-source AI model compilers and commercially available toolkits have evolved to facilitate the development and deployment of applications that use AI at its core. This "model once, run optimized anywhere" paradigm shift in deep learning computations introduces new attack surfaces and threat models that are methodologically different from existing software-based attack and defense mechanisms. Existing adversarial examples modify the input samples presented to an AI application either digitally or physically to cause a misclassification. Nevertheless, these input-based perturbations are not robust or stealthy on multi-view target. To generate a good adversarial example for misclassifying a real-world target of variational viewing angle, lighting and distance, a decent number of pristine samples of the target object are required. The feasible perturbations are substantial and visually perceptible. A new glitch injection attack on edge DNN accelerator capable of misclassifying a target under variational viewpoints will be presented. The attack pattern for each target of interest consists of sparse instantaneous glitches, which can be derived from just one sample of the target. I will also address the limitation of existing detectors of input-based adversarial examples, which are mostly designed based on sophisticated offline analyses. A new hardware-oriented and lightweight countermeasure will be introduced for in-situ detection of adversarial inputs feeding through a spatial DNN accelerator architecture or a third-party DNN Intellectual Property (IP) implemented on the edge.

Biodata

Chip Hong Chang is an Associate Professor at the Nanyang Technological University (NTU) of Singapore. He held concurrent appointments at NTU as Assistant Chair of Alumni of the School of EEE from 2008 to 2014, Deputy Director of the Center for High Performance Embedded Systems from 2000 to 2011, and Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. He has coedited five books, and have published 13 book chapters, more than 100 international journal papers (>70 are in IEEE), more than 180 refereed international conference papers (mostly in IEEE), and have delivered over 40 colloquia and invited seminars. His current research interests include hardware security and trustable computing, low-power and fault-tolerant computing, residue number systems, and application-specific digital signal processing algorithms and architectures. Dr. Chang currently serves as the Senior Area Editor of IEEE Transactions on Information Forensic and Security (TIFS), and Associate Editor of the IEEE Transactions on Circuits and Systems-I (TCAS-I) and IEEE Transactions on Very Large Scale Integration (TVLSI) Systems. He was the Associate Editor of the IEEE TIFS and IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) from 2016 to 2019, IEEE Access from 2013 to 2019, IEEE TCAS-I from 2010 to 2013, Integration, the VLSI Journal from 2013 to 2015, Springer Journal of Hardware and System Security from 2016 to 2020 and Microelectronics Journal from 2014 to 2020. He also guest edited eight journal special issues including IEEE TCAS-I, IEEE Transactions on Dependable and Secure Computing (TDSC), IEEE TCAD and IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS). He has held key appointments in the organizing and technical program committees of more

than 60 international conferences (mostly IEEE), including the General Co-Chair of 2018 IEEE Asia-Pacific Conference on Circuits and Systems and the inaugural Workshop Chair and Steering Committee of the ACM CCS satellite workshop on Attacks and Solutions in Hardware Security. He is the 2018-2019 IEEE CASS Distinguished Lecturer, a Fellow of the IEEE and the IET.

Keynote 9: Technology as an Enabler For Sustainable Growth – The Opportunity Ahead

Mr. Suresh Kumar
Design Engineering Vice President, Chipset Silicon Group, Intel

Abstract:

As communities globally emerge from the experience of the pandemic, expectations and aspirations have been fundamentally reset. In many ways, technology in its various forms has been at the core of sustaining life for the last 18 months. The adoption of digitalization has accelerated and transformed every aspect of life, perhaps by a decade. This has created opportunities for us, Electrical and Electronics engineers to contribute to reshaping society and helping build a new norm which is fairer, more inclusive and sustainable for the long term. Technology, when developed responsibly will allow us to touch & transform the lives of every person on the planet in ways, as never before imagined. This keynote discusses the facets of life that have changed through the pandemic as well as the huge opportunities that lie ahead for the IEEE community.

Biodata

Suresh Kumar is a Design Engineering Vice-President, in the Chipset Silicon Group at Intel. He leads hardware design development of next-generation Mobile/Desktop PC and Server Products. Suresh also serves as General Manager of Intel Malaysia Design Center and has more than 25 years of industry experience.

Tutorial Speakers

Tutorial 1A: Dye Sensitized Solar Cell Tutorial

Professor Ir. Dr. Suhaidi Shafie

Dr. Mohd. Amrallah B. Mustafa

Abstract

The tutorial is designed for beginner for the researcher to introduce them to DSSC. The basic construction of DSSCs consists of three main parts (Dye-sensitized photoelectrode, electrolyte and counter electrode) with a sandwich of two conducting substrates. The use of oxide semiconducting materials such as Tin(II) oxide(SnO), Titanium dioxide (TiO2) or Zinc oxide (ZnO) which act as a scaffold for dye molecules. It also presents the medium for electron charge transfer when the electron reaches its conduction band. However, TiO2 has considered the most used and efficient semiconductor due to its numerous superior characteristics, such as low toxicity, high chemical stability and mesoporous microstructure. After this tutorial, all participants get the knowledge of DSSCs and can fabricate their own DSSCs.

Biodata

Associate Professor Ir. Ts. Dr. Suhaidi Shafie received the Doctor of Engineering in Nanovision Technology from Shizuoka University in 2008.He is currently an Associate Professor in the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia and the Head of Functional Devices Laboratory, Institute of Advanced Technology, Universiti Putra Malaysia. Dr. Suhaidi research work focuses on Optical Devices especially in the field of Dye Sensitized Solar Cell. He has more than seven years of experience in the fabrication of high efficiency and flexible dye sensitized solar cell.He is a senior member of IEEE Circuits and Systems Society and was the chapter chair of IEEE Circuits and Systems Society Malaysia Chapter for 2017 - 2018. He is also a Professional Engineer and Professional Technologist registered under Board of Engineer, Malaysia and Malaysian Board of Technologist, respectively.

Dr. Mohd Amrallah Mustafa received his PhD. (Eng.) in Nanovision Technology from Shizuoka University in 2013. He is currently a Senior Lecturer in the Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Putra Malaysia. Dr. Mohd Amrallah research work focuses in the field of Dye Sensitized Solar Cell and he has more than five years of experiences in the fabrication of high efficiency and flexible dye sensitized solar cell. He is a member of IEEE Circuits and Systems Society and currently is the Vice-Chair of IEEE Circuits and Systems Society Malaysia Chapter

Tutorial 1B: Ultra-Low-Power and agile IC design: towards battery-less and low-cost distributed sensing

Dr. Orazio Aiello

Abstract

The vision of a world where pervasive integrated electronic systems embedded in everyday life objects (e.g. household appliances, surveillance cameras, healthcare systems) are fully interconnected to collect process, and exchange useful information requires energy-autonomous systems for distributed sensing and data acquisition. The low-cost requirement demands a small area, low design effort, digital-like shrinkage across CMOS generations, and design/technology portability. The possibility to exploit the digital (automated) design flow even for analog building blocks can dramatically reduce the design effort of any system-on-chip that faces the analog signal. In this framework, the tutorial illustrates the concepts and the design flows which enable the implementation of analog functions by true digital circuits**.** These approaches make the IC design suitable to nanoscale IC technologies in near-threshold and voltage/energy/technology scalability. The final aim is to move toward integrated building block able to operate battery-less but powered by harvested source of energy.

Biodata

https://www.linkedin.com/in/orazioaiello/

Tutorial 2A: Radio over IP Embedded System Tutorial

Mr. Wira Firdaus Haji Yaakob

Abstract

Radio over Internet Protocol (RoIP) is an integration of Voice over Internet Protocol (VoIP) with two-way radio control signals such as Push to Talk (PTT) and Carrier Operated Relay (COR) in digital format (audio, video). It provides end to end digital signaling from a handset radio to any other communication devices in the world such as smartphones, PCs, tablets, smartwatches, VoIP and Public Switched Telephone Network (PSTN). RoIP enables connection between different radios of different frequency bands to each other within or beyond Loss of Signal (LOS). Therefore, RoIP enables long distance bidirectional communication between a remote location to any other locations in the world.

This tutorial is specifically aimed for beginners who intended to have a basic understanding of RoIP. It will get you up to speed on the fundamentals of RoIP, the RoIP building blocks and what each does. It also provides understanding of RoIP applications, challenges and implementation. At the end of the tutorial, you will know what are the applications of RoIP and how to apply it in your communication world such as for emergency response. This tutorial is essential for embedded system engineers too. It will help to enhance your knowledge in terms of RoIP systems and their integration with radio networks.

Biodata

Wira Firdaus Haji Yaakob has more than 20 years industrial working experience in digital system design from silicon to embedded systems. He is currently the Technical Manager, Digital Systems Design, SAPURA Secured Technology Sdn. Bhd. Prior to joining SAPURA, he joined a few other companies including Seagate Technology, Altera Corporation, MIMOS Bhd. and as Head of Embedded Systems in Malaysia Microelectronic Solutions Sdn Bhd. He has conducted training to engineers in more than 20 countries across 4 continents. At SAPURA, he is responsible as a technical lead for tactical communication gateway development. He was elected as technical judge for University of Technical Malaysia (UTEM)'s Innovation and Design Expo (IDEX) 2015. He was also appointed as an industrial advisory panel (IAP) for industrial collaboration with USM and UTEM and recently appointed as adjunct lecturer at Universiti Teknologi Petronas (UTP).

Tutorial 2B: CMOS Device Modeling Tutorial

Dr. Philip Tan Beow Yew

Abstract

This tutorial is specially design for beginners who intended to have a quick but clear understanding of CMOS SPICE model. It points out the key basic concepts of CMOS SPICE models. Now, you do not need to be an experts who understand most of the physical equations in order to do the basic SPICE model extraction and apply the models for circuit design use. You just need to understand the key equations that will cover the fundamental physical characteristic of today's deep submicron CMOS transistors. SPICE model extraction is basically to find the appropriate values for the parameters in these physical equations that will give us the accurate electrical behavior that matches to the silicon data. After this tutorial, extracting or modifying a SPICE model file is possible for everyone.

Biodata

Dr. Philip Tan Beow Yew has more than 20 years hands-on working experience on extracting SPICE models for deep submicron CMOS transistors. He is currently the Senior Manager of Device Modeling, Silterra Malaysia Sdn. Bhd. Foundry. He has introduced physical equation in SPICE model to capture the Hook Shaped Idsat behavior due to STI stress in channel width direction when he was an engineer. He has lead his group (LogicHV) to excel in model extraction by introducing new Binning-Hybrid-Macro extraction methodology that combines the advantages from Global models, Binning models, Hybrid models and Sub-Circuit models. He initiated the development of LogicHV Device Modeling Software Tools, called LEVERAGE to automate the device modeling works. Currently, his group is capable to do IV and CV measurements and extract device models using this in-house developed software tools. He has put together a book called "Device Modeling Notes" that serves as an essential guideline for new device modeling engineers. He has been the instructor for Integrated Circuit Overview class for Silterra new hires for more than 10 years. Before involving in SPICE modeling works, he has spent a year On-Job-Training as a Process Integration Engineer at LSI Logic Corporation in Oregon, USA. He has given SPICE Modeling tutorial class in 2017 IEEE PrimeAsia conference and 2007 IEEE Regional Symposium on Microelectronic (RSM) conference. He has published 35 international and national IEEE conference papers. He was invited as Keynote Speaker for 2017 IEEE PrimeAsia conference, Kuala Lumpur. He was invited as the reviewer for IEEE Electron Device Letters and IEEE Transactions on Electron Devices journals. He was a Senior Member of IEEE Electron Devices Society.

GeronCAS

The world's population is AGEING: virtually every country in the world is experiencing growth in the number and proportion of older persons in their population. Ageing society has become one of the most significant social transformations of the 21st century, impacting all society sectors, namely healthcare, financial, employment, housing, transportation, etc. By 2050, there will be more than 2 billion people over the age of 60 in the world – about 25% of the world's population, positioning Ageing and Older Adults as one of the main agenda in 2030 Sustainable Development Goal (SDGs). Moreover, combined with a massive increase in technology adoption by older adults and a growing number of elderly-care providers, we expect more tech devices empowering older adults (i.e., gerontechnology) in the foreseeable future.

Following the success of the 1st GeronCAS hybrid workshop in 2020, the GeronCAS workshop 2021 will continue to stimulate interest in technology solutions addressing older adults' well-being. This year, the first edition GeronCAS Student Design Competition (SDC) is introduced to continue to encourage technology solution creation aligned with CAS, addressing older adults' well-being. GeronCAS SDC seeks technology solutions in personalizing older adult's well-being by accounting for individual variability (i.e., condition & needs).

*GeronCAS strives to be the reference platform for researchers and industry practitioners, and stakeholders to develop cutting-edge CAS-based technology solutions in the overarching Precision Ageing domain, directed towards the emerging needs of the older adults.

Dr Yongfu Li

Biodata

Yongfu Li (S'09–M'14-SM'18) received the B.Eng. and Ph.D. degrees from the Department of Electrical and Computing Engineering, National University of Singapore (NUS), Singapore.

He is currently an Associate Professor with the Department of Micro and Nano Electronics Engineering and MoE Key Lab of Artificial Intelligence, Shanghai Jiao Tong University, China. He was a research engineer with NUS, from 2013 to 2014. He was a senior engineer (2014-2016), principal engineer (2016-2018) and member of technical staff (2018-2019) with GLOBALFOUNDRIES, as a Design-to-Manufacturing (DFM) Computer-Aided Design (CAD) research and development engineer. His research interests include analog/mixed signal circuits, data converters, power converters, bioemdical signal processing with deep learning technique and DFM circuit automation.

Technical Program Schedule

IEEE Asia Pacific Conference on Circuits and Systems (APCCAS2021) &
IEEE Conference on Postgraduate Research in Microelectronics and Electronics (PRIMEASIA2021)

			22/11/2021 (Monday): Tutorial & Workshop	
Duration	Start Time	End time	Parallel Session A	Parallel Session B
0:30	8:30	9:00	Registration	
2:00	9:00	11:00	Tutorial: Dye Sensitized Solar Cell by Prof Ir. Dr. Suhaidi Shafie & Dr. Mohd. Amrallah B. Mustafa	Tutorial: Ultra-Low-Power and agile IC design: towards battery-less and low-cost distributed sensing by Dr. Orazio Aiello
0:30	11:00	11:30	Tea Break	
2:00	11:30	13:30	Tutorial: Radio over IP Embedded System by Mr. Wira Firdaus Haji Yaakob	Tutorial: CMOS Device Modeling by Dr. Philip Tan Beow Yew

	Malaysia Time		23/11/2021 (Tuesday)		
Dura-tion	Start Time	End time	Parallel Session A	Parallel Session B	Parallel Session C
0:20	9:30	9:50	Opening Ceremony		
0:45	9:50	10:35	Keynote 1: Akinori Konno, Professor, Graduate School of Science and Technology, Shizuoka University, Hamamatsu, Japan Title: Development of Pre-dyed Dye-sensitized and Perovskite Solar Cells		
0:15	10:35	10:50	Tea Break		
1:40	10:50	12:30	Analog and Mixed Signal Circuits and Systems 1	Digital Circuits and Systems 1	Artificial Intelligent Circuits and Systems
1:30	12:30	14:00	Lunch Break		
0:45	14:00	14:45	Keynote 2: Harikrishnan Ramiah, Associate Professor, University Malaya, Malaysia Title: Radio Frequency Energy Harvesting for Healthcare Wearable		
0:30	14:45	15:15	IEEE CASS Senior Membership Drive		
2:00	15:15	17:15	PrimeAsia 2021	Imaging System and Technologies & Multimedia Systems and Applications	Neural Networks and Neuromorphic Engineering
0:10	17:15	17:25	Tea Break		
0:20	17:25	17:45	Mentoring Program by IEEE CAS		

	Malaysia Time		24/11/2021 (Wednesday)		
Dura -tion	Start Time	End time	Parallel Session A	Parallel Session B	Parallel Session C
0:45	9:30	10:15	Keynote 3: Shimeng Yu, Associate Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology Title: RRAM for Compute-in-Memory: From Inference to Training		
0:15	10:15	10:30	Tea Break		
0:45	10:30	11:15	Keynote 4: Masami Ikura, Toyota Tsusho Nexty Electronics, Thailand Title: New issues and proposals for new technology development seen from application examples of AI + CONNECTED technology for automotives		
1:40	11:15	12:55	Analog and Mixed Signal Circuits and Systems 2	Digital Circuits and Systems 2	Communication Circuits and Systems & Signal Processing, Control and Communications
1:05	12:55	14:00	Lunch Break		
0:45	14:00	14:45	Keynote 5: Massimo Alioto, Professor, National University of Singapore Title: Intelligent Systems with Ultra-Wide Power-Performance Adaptation - Going Well beyond the Diminishing Returns of Voltage Scaling		
0:45	14:45	15:30	Keynote 6: Dr Bo Chen, Cadence, Singapore Title: The State-of-the-Art and Next Generation Simulation Technologies for Analog, Mixed-Signal and Memory Design		
0:10	15:30	15:40	Tea Break		
2:00	15:40	17:40	RF Integrated Circuit Design and Energy Harvesting	Digital Circuits and Systems & Digital Signal Processing	Nano electronics, Devices and System Integration & Sensors and Interfaces & Automotive Circuits and Systems
0:20	17:40	18:00	Mentoring Program by CAS		

	Malaysia Time		25/11/2021 (Thursday)		
Dura -tion	Start Time	End time	Parallel Session A	Parallel Session B	Parallel Session C
0:45	9:30	10:15	Keynote 7: Pui-In (Elvis) Mak, Professor, University of Macau, China Title: Towards Energy-Autonomous Bluetooth-Low-Energy Radios for IoT Applications		
0:15	10:15	10:30	Tea Break		
0:45	10:30	11:15	Keynote 8: Chip Hong Chang, Associate Professor, Nanyang Technology University (NTU) of Singapore Title: Security of Edge AI – A new challenge to deep learning accelerators		
1:20	11:15	12:35	Analog and Mixed Signal Circuits and Systems 3	Biomedical and Healthcare Circuits and Systems	Power/Energy Devices, Circuits and Systems & Integrated Power Management Unit (PMU)
1:25	12:35	14:00	Lunch Break		
0:45	14:00	14:45	Keynote 9: Mr Suresh, VP of Design Center, Intel Title: Technology as an Enabler For Sustainable Growth – The Opportunity Ahead		
1:40	14:45	16:25	GeronCAS Workshop	Analog and Mixed Signal Circuits and Systems 4	Electronic Design Automation & High Speed and Optical Wire lined Circuits and Systems
0:15	16:25	16:40	Tea Break		
0:20	16:40	17:00	Closing Ceremony		

Technical Program Abstract

Date	:	22/11/2021 (Monday)
Session	:	Tutorial & Workshop
Time	:	9:00 - 11:00

Tutorial Title	:	: Dye Sensitized Solar Cell
Speakers	:	Prof Ir. Dr. Suhaidi Shafie & Dr. Mohd. Amrallah B. Mustafa
Session Chair		Mohd Amrallah Mustafa, Universiti Putra Malaysia
Abstract	:	The tutorial is designed for beginner for the researcher to introduce them to DSSC. The basic construction of DSSCs consists of three main parts (Dye-sensitized photoelectrode, electrolyte and counter electrode) with a sandwich of two conducting substrates. The use of oxide semiconducting materials such as Tin(II) oxide(SnO), Titanium dioxide (TiO2) or Zinc oxide (ZnO) which act as a scaffold for dye molecules. It also presents the medium for electron charge transfer when the electron reaches its conduction band. However, TiO2 has considered the most used and efficient semiconductor due to its numerous superior characteristics, such as low toxicity, high chemical stability and mesoporous microstructure. After this tutorial, all participants get the knowledge of DSSCs and can fabricate their own DSSCs.

Tutorial Title	:	Tutorial 1B: Ultra-Low-Power and agile IC design: towards battery-less and low-cost distributed sensing
Speakers	:	Dr. Orazio Aiello
Session Chair		Nasri Sulaiman, Universiti Putra Malaysia
Abstract	:	Abstract: The vision of a world where pervasive integrated electronic systems embedded in everyday life objects (e.g. household appliances, surveillance cameras, healthcare systems) are fully interconnected to collect process, and exchange useful information requires energy-autonomous systems for distributed sensing and data acquisition. The low-cost requirement demands a small area, low design effort, digital-like shrinkage across CMOS generations, and design/technology portability. The possibility to exploit the digital (automated) design flow even for analog building blocks can dramatically reduce the design effort of any system-on-chip that faces the analog signal. In this framework, the tutorial illustrates the concepts and the design flows which enable the implementation of analog functions by true digital circuits. These approaches make the IC design suitable to nanoscale IC technologies in near-threshold and voltage/energy/technology scalability. The final aim is to move toward integrated building block able to operate battery-less but powered by harvested source of energy.

Date	:	22/11/2021 (Monday)
Session	:	Tutorial & Workshop
Time	:	11:30 - 13:30

Tutorial Title	:	Radio over IP Embedded System Tutorial
Speakers	:	Mr. Wira Firdaus Haji Yaakob
Session Chair		Tang Tong Boon, Universiti Teknologi PETRONAS
Abstract	:	Radio over Internet Protocol (RoIP) is an integration of Voice over Internet Protocol (VoIP) with two-way radio control signals such as Push to Talk (PTT) and Carrier Operated Relay (COR) in digital format (audio, video). It provides end to end digital signaling from a handset radio to any other communication devices in the world such as smartphones, PCs, tablets, smartwatches, VoIP and Public Switched Telephone Network (PSTN). RoIP enables connection between different radios of different frequency bands to each other within or beyond Loss of Signal (LOS). Therefore, RoIP enables long distance bidirectional communication between a remote location to any other locations in the world. This tutorial is specifically aimed for beginners who intended to have a basic understanding of RoIP. It will get you up to speed on the fundamentals of RoIP, the RoIP building blocks and what each does. It also provides understanding of RoIP applications, challenges and implementation. At the end of the tutorial, you will know what are the applications of RoIP and how to apply it in your communication world such as for emergency response. This tutorial is essential for embedded system engineers too. It will help to enhance your knowledge in terms of RoIP systems and their integration with radio networks.

Tutorial Title	:	**CMOS Device Modeling Tutorial**
Speakers	:	Philip Tan Beow Yew
Session Chair		Lini Lee, Multimedia University
Abstract	:	Abstract: This tutorial is specially design for beginners who intended to have a quick but clear understanding of CMOS SPICE model. It points out the key basic concepts of CMOS SPICE models. Now, you do not need to be an experts who understand most of the physical equations in order to do the basic SPICE model extraction and apply the models for circuit design use. You just need to understand the key equations that will cover the fundamental physical characteristic of today's deep submicron CMOS transistors. SPICE model extraction is basically to find the appropriate values for the parameters in these physical equations that will give us the accurate electrical behavior that matches to the silicon data. After this tutorial, extracting or modifying a SPICE model file is possible for everyone.

Date	:	23/11/2021 (Tuesday)
Session	:	Analog and Mixed Signal Circuits and Systems 1
Time	:	10:50 - 12:30
Session Chair	:	Mohd Tafir Mustaffa, Universiti Sains

Paper ID	:	1570727369
Paper Title	:	A Resistor-Less CMOS Bandgap Reference with High-Order Temperature Compensation
Authors	:	Yung-Hui Chung, Jia-Fong Shih, Yu-Hsiang Wang
Abstract	:	This paper presents a resistor-less high-precision CMOS bandgap voltage reference (BGR). A high-order curvature compensation is applied to correct higher-order nonlinear temperature terms of the emitter-base voltage (VEB) and meet the high-precision request. With this nonlinearity correction method, the CTAT voltage VEB can be better linearized over a wide temperature range. Without using resistors, the offset voltage of the BGR output buffer is applied to yield the PTAT voltage. Using the proportionally weighted sum of negative temperature coefficient (TC) on VEB and positive TC on VOS, a highly stable bandgap voltage reference can be achieved. The proposed BGR is implemented in 0.18-µm CMOS technology. The active area of the prototype BGR is 300µm×440µm. A minimum TC of 2.5ppm/°C is achieved over a temperature range from −40°C to 85°C. The maximum total current is 26 µA over the supply voltage ranging from 1.6V to 2V. The BGR output is about 996mV with the power supply noise attenuation of −48dB.

Paper ID	:	1570743551
Paper Title	:	High-speed CMOS ramp generator using proteretic comparator
Authors	:	Salma Khan, Azeemuddin Syed, Arif Sohel
Abstract	:	The ramp generator is a crucial circuit component in the design of switching power supply, analog to digital converters, CMOS image sensors, and many other essential circuits. Conventionally, the ramp generator has been implemented with a CMOS comparator that works on the hysteresis principle, which leads to an inherent systemic delay. This paper aims at improving the overall circuit speed by proposing the design of a ramp generator using CMOS proteretic comparator in 180nm TSMC process. It is established from the post-layout simulation that a speedup of 25% is achieved by replacing a hysteretic comparator with a proteretic comparator, and this is done with a trade-off in power consumption and circuit area.

Paper ID	:	1570750853
Paper Title	:	Fully-differential inverter-based OTA with improved composite transistors

Authors	:	Luis Henrique Rodovalho, Orazio Aiello, Cesar Rodrigues
Abstract	:	The paper deals with fully-differential inverter-based Operational Transconductance Amplifier (OTA) designed using rectangular transistor arrays (RTA) and improved composite transistors (ICT). The two versions of the same OTA are designed and the respective performance has been shown under aggressive supply voltage scaling down to 0.3 V. Post-layout simulations referring to 180~nm CMOS process technology have shown how the ICT solution with its proper body bias offer a higher voltage gain, CMRR, PSRR and a lower power consumption compared to the respective RTA version.

Paper ID	:	1570750855
Paper Title	:	A inverter-based OTA using improved composite transistors and bulk-driven common-mode rejection
Authors	:	Luis Henrique Rodovalho, Orazio Aiello, Cesar Rodrigues
Abstract	:	This work presents a gate-driven fully-differential inverter-based Operational Transconductance Amplifier (OTA) with a proper body bias using both rectangular transistor arrays (RTA) and improved composite transistors (ICT). Two versions of the same OTA were designed and compared with post-layout simulations referring to a 180 nm CMOS process. Simulation results show that the RTA OTA version has a 38 dB voltage gain, achieves a 1.1 kHz GBW for a 10 pF load, and consumes 970 pW total power for a 0.3 V supply voltage. The ICT OTA version shows better performance resulting in 48 dB voltage gain, 0.91 kHz GBW for a 10 pF load, and 810 pW total power consumption for a 0.3 V supply voltage.

Paper ID	:	1570736911
Paper Title	:	An Active Feedback Coefficient Tuning Technique for Compensating TC Variations in CT ΔΣ Modulators
Authors	:	Tobias Wolfer, Eckhard Hennig
Abstract	:	We propose a novel technique to compensate the effects of R-C / gm-C time-constant (TC) errors due to process variation in continuous-time delta-sigma modulators. Local TC error compensation factors are shifted around in the modulator loop to positions where they can be implemented efficiently with tunable circuit structures, such as current-steering digital-to-analog converters (DAC). This approach constitutes an alternative or supplement to existing compensation techniques, including capacitor or gm tuning. We apply the proposed technique to a third-order, single-bit, low-pass continuous-time delta-sigma modulator in cascaded integrator feedback structure. A feedback path tuning scheme is derived analytically and confirmed numerically using behavioral simulations. The modulator circuit was implemented in a 0.35-µm CMOS process using an active feedback coefficient tuning structure based on current-steering DACs. Post-layout simulations show that with this tuning structure, constant performance and stable operation can be obtained over a wide range of TC variation.

Date	:	23/11/2021 (Tuesday)
Session	:	Digital Circuits and Systems 1
Time	:	10:50 - 12:30
Session Chair	:	Maryam M Isa, Universiti Putra Malaysia Duy-Hieu Bui, Vietnam National University, Hanoi

Paper ID	:	1570750467
Paper Title	:	An Approximate Adder with Reduced Error and Optimized Design Metrics
Authors	:	Padmanabhan Balasubramanian, Raunaq Nayar, Douglas Maskell
Abstract	:	This paper presents a new approximate adder with reduced error and optimized design metrics. The proposed approximate adder is based on a modification of an existing approximate adder HERLOA and is called modified HERLOA or M-HERLOA in short. We considered a systematic modification of HERLOA to derive an optimum M-HERLOA. We evaluate the performance of M-HERLOA and other approximate adders in terms of the error characteristics and design metrics. We calculated popular error parameters such as mean absolute error and root mean square error for the approximate adders. We estimated the design metrics of approximate adders based on FPGA and ASIC-type (standard cell based) implementations. We also compare the performance of the accurate adder and different approximate adders based on a digital image processing application by evaluating the peak signal-to-noise ratio and structural similarity index metric. The proposed M-HERLOA reconstructs a digital image that is visually similar to the image reconstructed using the accurate adder. This is achieved with M-HERLOA simultaneously enabling following reductions in design metrics compared to the accurate adder for a 32-bit addition: (i) 9.5% reduction in delay, 9.1% reduction in total power, 7 LUTs less and 18 flip-flops less for a FPGA based implementation, and (ii) 18% reduction in delay, 26.7% reduction in total power and 23.1% reduction in area for an ASIC-type implementation.

Paper ID	:	1570730918
Paper Title	:	:Area-Efficient Finite Field Multiplication in GF(2n) Using Single-Electron Transistors
Authors	:	Chen Zhang, Chunhong Chen, Huapeng Wu
Abstract	:	Unlike metal-oxide-semiconductor field-effect transistors (MOSFETs), single-electron transistors (SETs) exhibit a unique characteristic of Coulomb oscillation which can find many digital applications with area efficiency. Implementation of multiple-input XOR logic gates with SETs is such an example. This paper presents an area-efficient SET-based implementation of finite field multiplications that require a large number of XOR operations and demonstrates a great potential to explore multiplication architectures (such as Karatsuba-algorithm based multiplication) for further area savings. We show that for a 256-bit polynomial multiplier, in

		particular, the SET-based implementation provides up to 30% savings in terms of gate count required when compared with its traditional CMOS-based counterpart.
Paper ID	:	1570743965
Paper Title	:	A 22nm CMOS 0.2V 13.3nW 16T SRAM Using Dynamic Leakage Suppression and Half-Selected Free Technique
Authors	:	Yue Wang, Guowei Chen, Xinyang Yu, Xujiaming Chen, Kiichi Niitsu
Abstract	:	This paper presents a 4kb ultra-low power static random access memory (SRAM) macro in 22nm CMOS with dynamic leakage suppression (DLS) and half-selected-free technique, typically for Internet of Things (IoT) applications requiring operation at low supply voltage. The DLS logic is used in the proposed SRAM cell to achieve ultra-low standby power, which has proved to be capable of reducing the static leakage current by 1899× compared to the conventional 6T SRAM cell. The proposed dual word line (WL) makes it possible to avoid the half-selected issues and reduces the bit line (BL) leakage by 51% compared to single WL. The SPICE simulation results done by SPECTRE simulator show that the 4kb SRAM macro designed in 22nm ultra-low leakage (ULL) CMOS technology process design kit (PDK) achieved the leakage current of 66.5 nA and the maximum operating frequency of 8.5 kHz at the minimum operating voltage of 0.2 V.
Paper ID	:	1570729307
Paper Title	:	A 20 GHz 8-bit All-N-Transistor Logic CLA Using 16-nm FinFET Technology
Authors	:	Tzung-Je Lee, Wen-Shou Yang, Chua-Chin Wang
Abstract	:	This paper presents a 20 GHz 8-bit carry-lookahead adder (CLA) using all-N-transistor (ANT) logic. By using the proposed ANT logic, an auxiliary current path through NMOS transistor is provided such that the speed limitation caused by PMOS is avoided. Besides, the FinFET device is used to improve the speed with the enhanced mobility. Moreover, the analysis of the delay time for the critical path of the 8-bit CLA is also carried out to improve the PDP (Power-Delay Product) by considering the parasitic R-C in FinFET devices. The proposed design is implemented with a typical 16 nm FinFET process.
Paper ID	:	1570731729
Paper Title	:	Sensitivity of FinFET Full-Adders to PVT Variations and Evaluation of a Mitigation Strategy
Authors	:	Gerson Andrade, Ricardo Reis, Eduardo da Costa, Alexandra Zimpeck
Abstract	:	This paper compares three different FinFET full-adder topologies based on elementary logic gates regarding the delay and power aspects, considering a traditional design and a design under process, voltage, and temperature (PVT) variations. The delay suffers a deviation of at least 36%, 58%, and 58.5% with PVT variations. The impact on power is around 62.4% for all types of variability. As PVT variability is a crucial concern in nanotechnologies, we also

evaluated a mitigation approach based on the addition of sleep transistors. We can obtain circuits up to 39.6% more reliable to the PVT influence with this strategy.

Date	:	23/11/2021 (Tuesday)
Session	:	Artificial Intelligent Circuits and Systems
Time	:	10:50 - 12:30
Session Chair	:	Luthffi Idzhar Ismail, Universiti Putra Malaysia

Paper ID	:	1570731916:
Paper Title	:	Moving Drones for Wireless Coverage in a Three-Dimensional Grid Analyzed via Game Theory
Authors	:	Elena Camuffo, Luca Gorghetto, Leonardo Badia
Abstract	:	Drones offer opportunities for networking and control solutions, but also challenges when it comes to their coordination. In this paper, we apply a game theoretic model to multi-agent drone scenarios, to regulate their movement so as to ensure timely positioning but avoiding collisions. Simulations are led through the Nash-Q learning algorithm in order to prove the theoretical analysis and confirm their predicted trajectory dynamics. The results of this work can be exploited as a tool to provide insights for multi-agent control.

Paper ID	:	1570731480:
Paper Title	:	Social Distancing Surveillance System via Inverse Perspective Mapping and Fixed-point Quantization
Authors	:	Chia Chie Lee, Lee Lini, Kan Yeep Choo
Abstract	:	During the Coronavirus Disease 2019 (COVID-19) pandemic, many countries have introduced the social distancing policy in public areas to stop the spread of disease by maintaining a physical distance between people. This paper proposes an Artificial Intelligence (AI)-powered social distancing surveillance system that can detect pedestrians through video surveillance and monitor the social distance between them via Inverse Perspective Mapping (IPM) in real-time. The proposed system was deployed on the devices located at the network edge such as IoT devices and mobile devices to enable real-time response with low data transmission latency. To bypass the restriction on the computational and memory capacity for the edge devices, the proposed system was optimized through fixed-point quantization. From the evaluation results, the optimized models are almost 4 times smaller as compared to the original models. The best trade-off between speed and accuracy can be achieved with a 27.1% improvement in speed and 2% degradation in accuracy.

Paper ID	:	1570740424:
Paper Title	:	Calibration method for improving the linearity of analog-to-digital converters in CMOS image sensor
Authors	:	Hua Fan,

Abstract	:	Random mismatch errors of components in analogto-digital converters (DACs) degrade the linearity performance of converters realized by these components. A unit capacitor calibration method for improving the linearity of the analog-todigital converter (ADC) in CMOS image sensor (CIS) is proposed, which improves the static and dynamic performance of the successive approximation register (SAR) ADC by reordering the unit capacitor. Simulation results show that for a 16-bit SAR ADC with the proposed calibration method, the maximum rootmean-square (rms) of integral nonlinearity (INL) and differential nonlinearity (DNL) are enhanced by 66.83% and 60.70% respectively. The mean value of the spurious free dynamic range (SFDR) is improved by 11.37 dB while the mean value of the signal-to-noise-and-distortion ratio (SNDR) is improved by 11.68 dB.
Paper ID	:	1570745143:
Paper Title	:	AI Technology For NoC Performance Evaluation
Authors	:	Biswajit Bhowmik
Abstract	:	An on-chip network has become a powerful platform for solving complex and large-scale computation problems in the present decade. However, the performance of bus-based architectures, including an increasing number of IP cores in systems-on-chip (SoCs), does not meet the requirements of lower latencies and higher bandwidth for many applications. A network-on-chip (NoC) has become a prevalent solution to overcome the limitations. Performance analysis of NoC's is essential for its architectural design. NoC simulators traditionally investigate performance despite they are slow with varying architectural sizes. This work proposes a machine learning-based framework that evaluates NoC performance quickly. The proposed framework uses the linear regression method to predict different performance metrics by learning the trained dataset speedily and accurately. Varying architectural parameters conduct thorough experiments on a set of mesh NoCs. A highlight of the experiments includes the network latency, hop count, maximum switch, and channel power consumption as 30-80 cycles, 2-11, 25µW, and 240µW, respectively. Further, the proposed framework achieves accuracy up to 94% and a speedup of up to 2228x

Date	:	23/11/2021 (Tuesday)
Session	:	PrimeAsia 2021
Time	:	15:15 - 17:15
Session Chair	:	Mohd Nazim Bin Mohtar, Universiti Putra

Paper ID	:	1570732194:
Paper Title	:	A 585mV, 16.6fJ/cycle, 0.2µW Variation Tolerant Scannable Hybrid Flip-Flop in 65nm CMOS LSTP
Authors	:	Sayandip Kar, Anuj Grover
Abstract	:	In this paper, we propose a novel hybrid scannable flip-flop which can operate at near-threshold and conventional supply voltages. The proposed design improves t dq delay by 39% and static power dissipation by 59% at 0.585V when compared to the transmission gate based master slave flip-flop in 65nm Low Standby Power (LSTP) technology. It consumes 208nW power at 25% data activity and 16.6fJ/cycle at 50MHz during active operation and has a power-delay product of 0.98fJ. The performance and power improvements are brought about by a 15% loss in area which is an acceptable tradeoff in low power performance intensive systems. The proposed design also enables time borrowing, thus averaging out data path variations which can cause failures at low supply voltages

Paper ID	:	1570728899:
Paper Title	:	Evaluation of the Robustness against Adversarial Examples in Hardware-Trojan Detection
Authors	:	Kazuki Yamashita, Kohei Nozawa, Seira Hidano, Shinsaku Kiyomoto, Nozomu Togawa
Abstract	:	Recently, due to the increase of outsourcing in integrated circuit (IC) design and manufacturing, the case that malicious third party vendors insert a malicious circuit, called a hardware-Trojan, into their products has been increasing. To detect the hardware Trojans, machine-learning-based hardware-Trojan detection methods for gate-level netlists using neural networks have been proposed. In these methods, 51 feature values and 11 feature values for detecting hardware Trojans were proposed. On the other hand, adversarial examples (AE) attacks, which add perturbation to circuits, have also been reported. These attacks can actually decrease the identification rate of detecting Trojan nets. In this paper, we set up two classifiers which consist of 51 and 11 feature values respectively and compare the robustness of them when they classify the circuits with AE attacks. The experimental results show that the classifier using 51 feature values performed better against AE attacks.

Paper ID	:	1570737990:

Paper Title	:	A 65-nm CMOS 0.4 V 49.6 nW Voltage Monitor for Small-Form-Factor Biomedical IoT Applications
Authors	:	Xinyang Yu, Guowei Chen, Yue Wang, Xujiaming Chen, Kiichi Niitsu
Abstract	:	This paper presents a low-power voltage monitor for small-form-factor, low-sample-rate biomedical Internet of Things (IoT) applications aiming to convert the analog output voltage 0-0.2 V of a biosensor into digital code. This design consists of 3 oscillators and a periphery logic circuit. A reference oscillator that can provide stable output frequency even supply voltage floats range of 0.35-0.45 V. Two sensitive oscillators which the output frequency will change rapidly due to the output voltage from biosensors. A resistive input stage is used in each sensitive oscillator to improve the linearity of the output. The SPICE simulation performed in 65-nm CMOS technology shows that the nonlinearity error is within -1.56 mV/+1.19 mV when the input voltage is 0-0.2 V, much lower than previous works. The power consumption of this design is 49.6 nW when the voltage supply is 0.4 V.
Paper ID	:	1570738697:
Paper Title	:	Characterization and Conductivity of PMMA by Copolymerization with Polyaniline (PANi)
Authors	:	Helyati Abu Hassan Shaari, Mohd Nazim Mohtar, Muhammad Ramli, Norizah Abdul Rahman
Abstract	:	In this paper, characterization and conductivity of poly(methyl methacrylate)/polyaniline (PMMA/PANi) copolymer is reported. The copolymer was obtained by free-radical polymerization using benzoyl peroxide (BPO) as an initiator. During polymerization, HCl-doped aniline was added into the radical PMMA for a copolymerization to occur. The copolymer ware latter characterized by Fourier Transform Infrared (FTIR) spectroscopy and X-ray Diffraction (XRD) analysis. The FTIR spectrum confirmed the crosslinking between PMMA and PANi. The conductivity analysis acquired using 4-probe method revealed that the copolymer exhibited conductivity of 5 x 10-8 S/cm
Paper ID	:	1570768018:
Paper Title	:	Double Deposition Technique for Organic Thin Film: Effect on Optical and Morphology Properties
Authors	:	Nur Zuraihan, Mohd Nazim Mohtar, Ahmad Ghadafi Ismail, Roslina Mohd Sidek, Suhaidi Shafie, Muhammad Ramli
Abstract	:	Blending of organic semiconducting materials between small molecule and polymer become feasible and practical technique to increase the charge transport of thin films for organic electronic application. Thus, blending of conducting polymer with small molecule semiconductors has been extensively studied in recent years however, results of blending between these two materials have tendency to interrupt the electronic structure of each material and affect the charge transport within molecules. Herein, we investigate the optical and morphological properties of double fabrication of P3HT and TIPS Pentacene thin films deposited on glass substrate by floating transfer method and spin coating technique. Optical properties show that the highest absorption in the visible region on the spectrum for double deposition P3HT: TIPS Pentacene thin films. The surface morphology shows that the

		roughness increases for double fabrication of P3HT: TIPS Pentacene thin films compared to neat P3HT thin films. This work shows the effect of double deposition on the optical and morphology of active layer of organic thin films
Paper ID	:	1570772223:
Paper Title	:	Review Of 3D Networks-On-Chip Simulators and Plugins
Authors	:	Ahmed Al-Hchaimi, Fakhrul Zaman Rokhani, Wameedh Flayyih
Abstract	:	In this paper, a comprehensive review focuses on 3D network-on-chip (NoC) simulators and plugins while paying attention to the 2D simulators as the baseline is presented. Discussions include the programming languages, installation configuration, platforms, and operating systems for the respective simulators. In addition, the simulator's design abstraction level and plugins for design metrics (e.g., power, thermal, and network performance) evaluations are addressed. This review is intended for the early career researcher starting in 3D NoC, offering selection guidelines on the right tools for the targeted NoC architecture, design, and requirements

Date	:	23/11/2021 (Tuesday)
Session	:	Imaging System and Technologies & Multimedia Systems and Applications
Time	:	15:15 - 17:15
Session Chair	:	Asral Bahari Jambek, Universiti Malaysia Perlis

Paper ID	:	1570715245:
Paper Title	:	Motion Assisted Video-based Stereo Matching
Authors	:	Shengyu Gao, Hongyu Wang, Teng Wang, Yang Wang, Xiangyu Zhang, Xin Lou
Abstract	:	This paper presents a method to utilize the movement relationship between adjacent frames for video-based stereo matching. Unlike existing video-based algorithms that need complicated calculation to fuse the information between frames, the proposed method uses the existing motion vector in video encoder or decoder to reconstruct the initial disparity of the target frame from a reference frame. By disparity plane reconstruction, disparity can be initialized in an easy way, such that unnecessary steps in the stereo matching pipeline can be skipped. By taking advantages of the motion relationship between frames, the proposed scheme can achieve better performance with less computation compared with the original method.

Paper ID	:	1570722694:
Paper Title	:	Stereo Point Cloud Refinement for 3D Object Detection
Authors	:	Wangchao Liu, Yang Wang, Teng Wang, Xiangyu Zhang, Xin Lou
Abstract	:	3D object detection has shown advantages over its 2D image based counterpart. This paper proposed a new pipeline to utilize the left and right consistence check on disparity map for stereo point clouds-based 3D object detection. Unlike existing pipeline directly project the depth map to the 3D space, the proposed pipeline first use the left and right consistence to filter out the bad pixels in the disparity map before the projection to stereo point clouds. Experimental results show that by eliminating those bad points, the proposed pipeline can achieve better performance in 3D object detection tasks. Moreover, due to the reduced number of points, the computation cost of 3D object detection can be significantly reduced.

Paper ID	:	1570722806:
Paper Title	:	High Quality Far Infrared Image Colorization Based on Generative Adversarial Network
Authors	:	Hang Wang, Cheng Cheng, Zeyu Hao, Hongbin Sun

Abstract	:	Colorization for far infrared image is a very challenging task in which feature detection is difficult because of the lack of details compared with visible image. In this paper, we propose a high quality far infrared image colorization method based on generative adversarial network. An efficient pre-processing module is used to improve the quality of colorized image quality in low light environment. In addition, since conventional loss function is not sufficient enough for far infrared image colorization, we propose a composite loss function that combines pixel-wise, adversarial and attention losses. Our proposed method is fully-automatic and robust to image pair misalignments. Quantitative and qualitative experiments demonstrate that our proposed method significantly outperforms existing approaches on the KAIST multispectral pedestrian dataset, achieving more natural and plausible colorized images especially in low light environment.
Paper ID	:	1570723070:
Paper Title	:	A Real Time Video Stabilizer Based on Feature Trajectories and Global Mesh Warping
Authors	:	Sheng-Jui Huang, Yi-Hsien Lin, Chi-Hung Weng, Yi-Chang Lu
Abstract	:	Video recording has become one of the key features of digital cameras nowadays. Though the resolution and quality of frames always draw the attentions, the stability issue of amateur videos is less addressed. The amount of data involved in video stabilization makes memory bandwidth a bottleneck. Hence existing hardware accelerators are usually designed using a simple approach of displacement compensation, which has limited performance. In this work, we design a special processor capable of conducting a better stabilization process in real time. The hardware techniques implemented include pipelining, parallel processing, memory interleaving, and data ordering. The chip is synthesized with TSMC 40nm technology. A 11X speedup can be achieved when compared to the software version.

Date	:	23/11/2021 (Tuesday)
Session	:	Neural Networks and Neuromorphic Engineering
Time	:	15:15 - 17:15
Session Chair	:	Nasri Sulaiman, Universiti Putra Malaysia Khanh N. Dang (Vietnam National University

Paper ID	:	1570751912:
Paper Title	:	A Study on Accuracy Improvement of Small Object Detection Using Deep Neural Networks
Authors	:	Junya Morioka, Ryusuke Miyamoto
Abstract	:	The accuracy of visual object detection that estimates locations and classes of target objects in input images has been drastically improved by rapidly advancing technology about deep convolutional neural networks (CNNs). The evaluation of existing methods based on CNNs is usually conducted using major datasets such as MS-COCO, PASCAL-VOC, etc: these datasets include several sizes of target objects. The accuracy of detection larger objects has become excellent by recent methods but it has been still difficult even for recent CNNs to detect small object accurately. To solve this problem, this paper investigates how to improve the accuracy of small object detection with CNNs. For the investigation, two kinds of datasets composed only of small target objects were created: the bird dataset including only flying objects in the sky and the SAVMAP dataset having only mammals on the savannah. Experimental results using the datasets showed that input size, depth of CNN layers, and surrounding context of target objects were important factors for small object detection. Experimental results showed that, EfficientDet-D0 achieved an accuracy of 0.6585 for the bird dataset and 0.6501 for the SAVMAP dataset.

Paper ID	:	1570752115:
Paper Title	:	A Multilayer Perceptron Training Accelerator using Systolic Array
Authors	:	Takeshi Senoo, Akira Jinguji, Ryosuke Kuramochi, Hiroki Nakahara
Abstract	:	As the volume and type of network traffic increase, there is a growing demand for machine learning to detect attacks. There is a use to train a model in a short time. For example, a network intrusion detection (NID) system needs to learn new attack patterns that constantly occur in a short period. We propose a training accelerator as a systolic array on a Xilinx U50 Alveo FPGA card to solve this problem. We found that the accuracy is almost the same as conventional training even when the forward and backward paths are run simultaneously by delaying the weight update. Compared to the Intel Core i9 CPU and NVIDIA RTX 3090 GPU, it was three times faster than the CPU and 2.5 times faster than the GPU. The processing speed per power consumption was 11.5 times better than the CPU and 21.4 times better than the

GPU. From these results, we can conclude that implementing a training accelerator on FPGAs as a systolic array can achieve high speed and high energy efficiency.

Paper ID	:	1570720689:
Paper Title	:	Efficient Techniques for Extending Service Time of Memristor-based Neural Networks
Authors	:	Yu Ma, Chengrui Zhang, Pingqiang Zhou
Abstract	:	Memristor crossbar array (MCA) based accelerators can be used to accelerate neural networks. However, the conductances of memristors are slowly changed in the inference processes because of drift phenomena. As the weights are represented as the conductances, the weights are also changed slowly and the accuracy of neural network degrades. In order to slow down the accuracy degradation, some researchers propose methods using multiple memristors representing one weight, which leads to high area and energy overhead. Other researchers apply BFGS algorithm to determine the input amplitude and duration to reduce drift impact, which needs a huge amount of extra computation and is not practical. In this paper, we propose two techniques to slow down the accuracy degradation by recovering the accuracy after drifting. Firstly, we introduce one label memristor to monitor the drift degree of the crossbar and change the current-result conversion parameter to recover the accuracy. Secondly, we propose an auto-correction technique to correct the conductance of the label memristor. The conductance of the label memristor is used to change the parameter which is used in current-result conversion phase. Experimental results show that our proposed techniques can increase up to 8 times high accuracy (>95%) time and 3 times lifetime (>80%) for MCA based neural networks.

Date	:	24/11/2021 (Wednesday)
Session	:	Analog and Mixed Signal Circuits and Systems 2
Time	:	11:15 - 12:55
Session Chair	:	Mohd Tafir Mustaffa, Universiti Sains Malaysia

Paper ID	:	:1570737092:
Paper Title	:	Asynchronous Time-domain Amperometric Sensor Interface For a Wide Range of Cdl
Authors	:	Jiazhen Zhu, Bartas Abaravicus, Amlan Nag, Srinjoy Mitra
Abstract	:	The linearity and stability of an amperometric sensor can be affected by the size of the double layer capacitor ($\boldsymbol{Cdl}$) in the electrode. A working electrode (WE) with millimeter size area can have a $\boldsymbol{Cdl}$ larger than 10nF, whereas a WE in nanometer range show tens of femto-Farad $\boldsymbol{Cdl}$. We propose an amperometric sensors that is immune to the negative effect introduced by a wide variance of $\boldsymbol{Cdl}$, but does not require and additional mismatch calibration. By using dynamic current mirrors, the resolution of the sensor is increased to over 9bits. We perform extensive simulation to determine linearity ($\boldsymbol{R2}$>$\boldsymbol{0.999}$), DNL and noise floor all within acceptable limits.

Paper ID	:	:1570737217:
Paper Title	:	A PVT-Robust Closed-Loop Dynamic Amplifier Using Three-Stage Floating Inverter Amplifier
Authors	:	Chiwen Cheng, Kenichi Ohhata
Abstract	:	This paper proposes a closed-loop dynamic amplifier using three-stage floating inverter amplifier (FIA). The closed-loop configuration and high open-loop gain owing to the three-stage configuration ensures the gain accuracy and robustness to process, supply voltage, and temperature (PVT) variation. Moreover, careful phase compensation design enables a stable output response, resulting in fast settling. The simulation results show that the proposed circuit can reduce the closed-loop gain error to 0.4% and the error variation due to PVT variation to less than half of that of the conventional circuit.

Paper ID	:	:1570735484:
Paper Title	:	Novel Gate Tracking and N-well Control Circuit for 2 × VDD Tolerant I/O Buffer
Authors	:	Dharmaray Nedalgi, Saroja Siddamal
Abstract	:	This paper presents a 2×VDD tolerant I/O buffer with low voltage (VDD) devices. The novel gate tracking circuit and N-well control circuits in mixed voltage I/O buffer is proposed to solve the unwanted leakage paths and dynamic power loss. The proposed design is verified in 22nm

		FinFET technology. The design can be used for any CMOS technology for 2 × VDD tolerant I/O buffer.
Paper ID	:	:1570735478:
Paper Title	:	2 × VDD tolerant I/O with Considerations of Hot-Carrier Degradation and Gate-Oxide Reliability
Authors	:	Dharmaray Nedalgi, Saroja Siddamal
Abstract	:	This paper presents a 2 × VDD tolerant I/O buffer using 1 × VDD devices, with hot-carrier and gate-oxide reliability considerations. The novel circuit for mixed voltage I/O buffer is proposed to solve the hot-carrier and gate-oxide reliability issues. The proposed circuit is designed in 22nm FinFET technology. The design can be used in any CMOS technology for 2 × VDD tolerant I/O buffer to reduce hot-carrier effect.

Date	:	24/11/2021 (Wednesday)
Session	:	Digital Circuits and Systems 2
Time	:	11:15 - 12:55
Session Chair	:	Kalai Selvan Subramaniam , Infinecs Systems Sdn. Bhd Kwen Siong Chong, Zero-Error Systems Pte Ltd (S)

Paper ID	:	1570744085:
Paper Title	:	A Digital Random Number Generator Based on Regular Sampling of Double Scroll Chaos
Authors	:	Onur Karatas, Salih Ergun
Abstract	:	This paper presents the design of a novel digital random number generator (RNG) based on the distribution of regular samples from a double scroll chaotic system. In this study, a double scroll chaotic system is designed by using the Euler approximation and the non-linearity feature of sawtooth wave in a 3rd order ordinary differential equation (ODE). By examining the distribution of the values of chaotic state variables, it is demonstrated that the distribution has at least two regions and a binary sequence can be obtained by exploiting these two regions. The XOR is used to combine the resulting binary sequences obtained from these two regions, and thus, the RNG is designed. The RNG output satisfies all statistical randomness tests in the NIST 800-22 package without postprocessing. The proposed RNG is implemented using Verilog hardware description language and prototyped on a KCU105 Evaluation Board Xilinx Ultrascale Field Programmable Gate Array (FPGA) with less than 1% LUT and Flip-Flop utilization and data throughput of up to 1.3125 Mbps.

Paper ID	:	1570723287:
Paper Title	:	A Random Number Generator Based on Metastability of Oscillators
Authors	:	Recep Günay, Salih Ergun
Abstract	:	1570723287 An irregular sampling of regular waveform based true random number generator (TRNG) utilizing a tetrahedral oscillator as entropy source is proposed. The tetrahedral oscillator is composed of multiple nested rings which increases entropy due to metastability. By integrating tetrahedral oscillator with irregular sampling method, the proposed RNG is faster and more robust to external interference attacks than regular sampling of tetrahedral oscillator, it uses much less hardware resources than regular ring oscillator based RNGs. In total, 5 tetrahedral oscillators are used as the entropy source and they are combined with an XOR gate. This XOR output is used to sample a faster regular clock, which should have a duty cycle as close to 50% as possible, to generate the random bit. The randomness of the bit stream was proved with National Institute of Standard and Technology (NIST) 800-22 Test Suites. The proposed design uses 93 LUTs and 14 FFs while consuming 100mW of power and having a throughput of 1.7MHz. The speed is 17 times faster than regular sampling of

		tetrahedral and the resource usage is 16 times lower than regular ring oscillator based RNG designs.
Paper ID	:	1570768065:
Paper Title	:	Design and implementation of GPIO subsystem using external foundry I/O buffer
Authors	:	Kean Hong Boey
Abstract	:	Due to business and manufacturing capacity reasons, semiconductor companies may choose to outsource fabrication, assembly or testing. In this paper, design method of the low speed I/O subsystem in the platform controller hub (PCH) comprising of both hard intellectual property (IP) and soft IP, and the evolution of the implementation leading to the final adaptation with external foundry buffer is presented. Novel techniques to map Intel analog buffer with external foundry buffer to enable direct reuse of existing GPIO Chassis controller (soft IP). The design method and implementation successfully enabled the first PCH fabricated at external foundry, with zero post silicon bugs in the low speed I/O subsystem.
Paper ID	:	1570737055:
Paper Title	:	Digital Background Correction for Channel Mismatch and Third-Order Nonlinearity of TI-ADCs with VCOs
Authors	:	Takao Kihara
Abstract	:	A time-interleaved analog-to-digital converter (TI-ADC) with voltage controlled oscillators (VCOs) can efficiently convert radio-frequency (RF), a few gigahertz, signals into digital ones with medium resolution. This ADC, however, suffers from aliasing signals, and harmonic distortion (HD) and intermodulation (IM) products owing to the channel mismatches and the nonlinearity of the VCO gain, respectively. We first present a digital background correction to reduce the mismatch aliasing signals and the third-order HD and IM products of four-channel TI-ADCs with VCOs. Our method utilizes the complex and decimated signals, sent from a direct-RF receiver, and adaptive filters with cross-correlation functions of these signals. Then, we implement the correction circuit with 24-bit floating point arithmetic to compromise between the accuracy and power consumption. Simulations show that the correction improves the two-tone spurious-free dynamic range (SFDR) of a TI-ADC with a sampling frequency of 3, 680 MHz from 54.8 dB to 66.7 dB and the circuit designed with a 65-nm CMOS technology operates at 4.3 mW and a rate of 57.5 MS/s.
Paper ID	:	1570732444:
Paper Title	:	Novel March Test Algorithm Optimization Strategy for Improving Unlinked Faults Detection
Authors	:	Aiman Zakwan Jidin, Razaidi Hussin, Mohd Syafiq Mispan, Weng Lee
Abstract	:	March-series test algorithms have proven to be popular choices for Memory BIST implementation, owing to its simplicity yet having a good fault coverage. However, March test

algorithms with low test complexities are incapable to detect some unlinked Single-Cell faults and many Double-Cell faults. This paper presents a new optimization strategy aimed to improve the fault coverage of the existing March test algorithms by detecting the previously undetectable Single-Cell faults and Double-Cell faults. It is achieved by optimizing the test operation sequences of the existing March test algorithms through an automation program, to achieve higher fault coverage while maintaining the same test complexity as the original March algorithm. Performance analysis shows that the fault coverage can be improved from 44% to 72% for March LR, by using the proposed optimization strategy.

Date	:	24/11/2021 (Wednesday)
Session	:	Communication Circuits and Systems & Signal Processing, Control and Communications
Time	:	11:15 - 12:55
Session Chair	:	Nasri Sulaiman, Universiti Putra Malaysia

Paper ID	:	1570731915:
Paper Title	:	Resource Sharing in the Internet of Things and Selfish Behaviors of the Agents
Authors	:	Lorenza Prospero, Roberto Costa, Leonardo Badia
Abstract	:	Resource sharing is an issue for many different fields of applications, giving rise to the so-called "Tragedy of the commons." This is particularly important in reference to the upcoming Internet of Things, where selfish behaviors from individual users may jeopardize a cooperative network behavior, on which most network functions in this scenario rely. In this paper, we analyze two ways of splitting resources in the context of channel allocation for wireless systems. We describe the outcomes of the different strategies and we identify some criteria for the emergence of selfish behaviors in such games.

Paper ID	:	1570737237:
Paper Title	:	Post-Processing of K-best MIMO Detection for High-Order Modulations
Authors	:	Yu-Xin Liu, Ya-Xin Dai, Yeong-Luh Ueng
Abstract	:	This paper presents an iterative post-processing scheme for conventional K-best MIMO detection based on repeating the K-best search from a single root node. Utilizing the partial Euclidean distance and the detected path in the conventional detection process, the root node can be determined for each post-processing iteration. Once the correct root node is determined in post-processing, we can use a smaller value of K in the post-processing process to obtain the correct path. Moreover, the proposed scheme is only enabled when the partial Euclidean distance of the detected path is extremely large and considered to be incorrect to reduce the latency and the computational complexity. Based on simulation results, the proposed method provides a notable improvement in performance while maintaining a similar complexity for MIMO systems using high-order modulations.

Paper ID	:	1570728360:
Paper Title	:	Sequential Linear-Dynamic Programming for Reliability Control in Wind Energy Conversion Systems
Authors	:	Hana Baili

Abstract : This paper addresses the problem of reliability control to promote power balance in energy systems with wind generation. Reliability control is reformulated as a trajectory optimization or optimal control problem for a hybrid stochastic differential system. Accordingly, in theory, the dynamic programming principle provides the only closed form exact solution to the problem of reliability control. But in practice, its complexity resides in the resolution of the Hamilton-Jacobi-Bellman equation. In most cases, indeed, Bellman's equation cannot be solved analytically. This paper explores a feasible alternative: successive approximations of the exact solution that could be referred to as sequential linear-dynamic programming or SLDP in abridged notation. On the one hand, these successive approximations stipulate by construction a stochastic optimal control of the feedback type, and on the other hand, they enjoy the properties of cost convergence and strict monotonicity over the course of the iterations. Significant result has been achieved in the implementation of the SLDP approach.

Date	:	24/11/2021 (Wednesday)
Session	:	RF Integrated Circuit Design and Energy Harvesting
Time	:	15:40 - 17:40
Session Chair	:	Jasronita Jasni, Universiti Putra Malaysia

Paper ID	:	1570738974:
Paper Title	:	A Broadband Tri-Coil Based Transformer Design for Mm-wave Cascode Amplifiers
Authors	:	Haoyang Jia, Guangyin Feng, Yanjie Wang
Abstract	:	This paper presents a broadband transformer design based on three coils with mutual magnetic coupling for cascode amplifiers. To demonstrate benefits of the proposed tri-coil transformer, a single-stage cascode low noise amplifier is designed in 40nm CMOS process. The LNA with proposed tri-coil transformer exhibits significant stability and bandwidth enhancement. The simulated results show that the LNA achieves the 3-dB bandwidth of 27GHz, and factional bandwidth of 52.4%. At 54GHz, the simulated noise figure and gain of single-stage LNA are 3.6dB and 11.07dB, respectively.

Paper ID	:	1570722569:
Paper Title	:	A 0.1V Input Energy Harvesting Charge Pump with Dynamic Gate Biasing and Capacitance Scaling
Authors	:	Jack Kee Yong, Harikrishnan Ramiah, Kishore Kumar Pakkirisami Churchill, Gabriel Chong
Abstract	:	This paper reports the investigation in the pumping capacitance to the charge pump performance. The work proposed a capacitance optimization technique on cascading charge pump which achieves higher power conversion efficiency (PCE) with a lower capacitance. This paper also reports a cross-couple charge pump (CCCP) with 40% (PCE) at 100mV. It features a dynamic gate-bias technique which can improve forward current drivability and reduce reverse-leakage current. The circuit is simulated in 65-nm CMOS technology.

Paper ID	:	1570722066:
Paper Title	:	A Differential RF Front-end CMOS Transformer Matching for Ambient RF Energy Harvesting Systems
Authors	:	Wen Xun Lian, Harikrishnan Ramiah, Gabriel Chong, Kishore Kumar Pakkirisami Churchill
Abstract	:	This paper presents a fully integrated CMOS front-end matching network for ambient RF energy harvesting (RFEH) systems. The proposed method utilizes an on-chip step-up stacked transformer integrated to provide impedance transformation and passive voltage boosting. Besides, the on-chip transformer act as a balun which generates differential signal to drive a 5-stage Cross-Coupled Differential-Drive (CCDD) rectifier. Simulation results on a standard 65-

		nm CMOS process for harvesting ambient RF energy at 900MHz shows the proposed solution attains a peak sensitivity of -16.5 dBm at an output voltage of 1V.
Paper ID	:	1570715789:
Paper Title	:	Dynamic Tail Biased Class-C Voltage-Controlled-Oscillator with Double-Balanced Mixer Design
Authors	:	Wen Cheng Lai
Abstract	:	This article proposes low-power class-C voltage-controlled oscillator (VCO) with double-balanced mixer. The oscillator consists of a dual-resonance LC resonator in shunt with one pair of capacitive cross-coupled nMOSFETs. The common source of cross-coupled nMOSFETs is connected to the ground through a tail transistor in shunt with a capacitor, dynamic bias is applied to the gate of the tail. The proposed oscillator has been implemented with the tsmc 0.18µm CMOS technology and the core current and DC consumption of the oscillator are 2.535 mA and 2.99 mW, respectively at the dc drain-source bias of 1.18V. The oscillator can generate differential high-band and low-band signals at 4.286GHz and 2.94GHz respectively. The die area of the class C oscillator is 1.187×1.109 mm2. The layout dimension of the mixer is 0.6×0.7 mm2.
Paper ID	:	1570746631:
Paper Title	:	Design of Diode-Connected and Cross-Connected CMOS Rectifers with Adaptive Tuning for RF Energy Harvesting
Authors	:	Xiaofei Li, Yan Lu, Rui Martins
Abstract	:	Distributed IoT devices require energy harvesting solutions for autonomous operation. Among the popular ambient energy sources (solar, wind, vibration), RF energy is special because of the transmission by humans while the other sources mainly emerge from Nature. In other words, when compared with other sources RF energy is easier to control. In an RF energy harvesting system the rectifier is the critical component. This paper addresses first the comparison between cross-connected and diode-connected CMOS rectifiers most commonly used in the energy harvesting system. Then, we discuss VTH compensation in the rectifier with adaptive bias tuning methods to improve the PCE performance of CMOS rectifiers.
Paper ID	:	1570749194:
Paper Title	:	A Wideband CMOS Power Amplifier with Integrated Digital Linearizer and Tunable Transformer
Authors	:	Selvakumar Mariappan, Jagadheswaran Rajendran, Narendra Aridas, Andrei Grebennikov, Arokia Nathan, Siddik Yarman ,
Abstract	:	This paper presents a fully integrated wideband CMOS power amplifier (PA) with Digitally Assisted Wideband Pre-Distorter (DAWPD) and tunable transformer. The DAWPD is implemented at the driver amplifier to establish a pre-distorter linearizing mechanism across the wide frequency bandwidth. The DAWPD mechanism has an integrated Digital Linearizer

(DL), which is controlled via digital bits. The DAWPD-PA also integrates with a tunable transformer employed at its output matching network to achieve optimum efficiency and output power performance across a wideband frequency. The DAWPD-PA has been fabricated in CMOS 130 nm and has an operating bandwidth of 1 GHz from 1.7 to 2.7 GHz. The gain achieved is 26.9 to 29.7 dB across the frequency. The linear output power and PAE achieved across the operating frequency are 24.0 to 25.1 dBm and 34.5 to 38.8%.

Date	:	24/11/2021 (Wednesday)
Session	:	Digital Circuits and Systems & Digital Signal Processing
Time	:	15:40 - 17:40
Session Chair	:	Lini Lee, Multimedia University Anastacia Alvarez, University of the Philippines

Paper ID	:	1570738717:
Paper Title	:	An Automation Program for March Algorithm Fault Detection Analysis
Authors	:	Aiman Zakwan Jidin, Razaidi Hussin, Weng Lee, Mohd Syafiq Mispan
Abstract	:	The efficiency of a Memory BIST for embedded memory testing depends on the fault coverage of the implemented test algorithm. The fault detection performance analysis on a March algorithm is indispensable to determine its fault coverage. This analysis process is very tedious and time-consuming, since there are many fault models to be analyzed, and their sensitizers and detectors must be identified within the algorithm test operation sequences. This paper presents the development of an automation program that is capable to analyze a March algorithm fault detection performance autonomously. It comprises of reading and extracting information from the input algorithm, identifying the value trend of the memory cells, identifying the pair of sensitizer and detector of each fault model, and finally producing a detailed fault detection analysis result and the fault coverage. The output results from the proposed automation program execution show the identical fault detection analysis as the manual analysis, which was completed in less than 3 ms.

Paper ID	:	1570729133:
Paper Title	:	A 2.5-GHz 2×VDD 16-nm FinFET Digital Output Buffer with Slew Rate and Duty Cycle Self-Adjustment
Authors	:	Tzung-Je Lee, Wen-Jian Su, Lean Karlo Tolentino, Chua-Chin Wang
Abstract	:	This paper presents a 2×VDD, PVT-insensitive (process, voltage, and temperature) output buffer that has a slew rate and duty cycle self-adjustment. It complies with the slew rate, system voltage, and duty cycle requirements for DDR4 SDRAMS. Low Vth transistors which are always turned on are selected as drivers in the Output Stage to prevent output current fluctuations and increase the driving current. These transistors' gates are stabilized by both driving currents and a capacitor rejecting any interference by the noise coupled from GND. The output buffer is realized using TSMC 16-nm FinFET CMOS process. The core area is 0.1412\(\times\)0.0794 mm\(^2\). At 2.5 GHz, it has maintained a slew rate of 6.4 and 8.7 V/ns and a duty cycle of 48.3 to 49.2% at a maximum load capacitance of 30 pF. Whether at normal voltage mode (VDD) or high voltage mode (VDDIO), the \(\Delta\)SR improvement is approximately at least 20% after driving current auto-tuning.

Paper ID	:	1570741391:
Paper Title	:	Digraph Filter Design Based on Directed Laplacian Matrix and Least Squares Method
Authors	:	Chien-Cheng Tseng, Su-Ling Lee
Abstract	:	In this paper, the digraph filter design based on directed Laplacian matrix (DLM) and least squares method is presented. First, the eigen-decomposition of DLM is used to define the digraph Fourier transform (DGFT). Then, the spectral properties of DGFT are studied and applied to specify the ideal spectral response of the digraph filter. Next, the coefficients of polynomial digraph filter are determined by the least squares method which minimizes the integral absolute squared errors between ideal response and actual spectral response of filter. The matrix inversion can be used to compute the optimal solution. Finally, the numerical example of noise reduction application is demonstrated to show the effectiveness of the designed digraph filter.
Paper ID	:	1570712970:
Paper Title	:	Robust Multi-Source Direction of Arrival Estimation Using a Single Acoustic Vector Sensor
Authors	:	Jianhua Geng, SiFan Wang, Juan Li, Jingwei Li, Xiangyu Zhang, Xin Lou ,
Abstract	:	In conventional approaches of acoustic vector sensor (AVS) based direction of arrival (DOA) estimation under noisy and reverberant environment, all the raw time-frequency (TF) data are inputted for reliable TF points extraction, which is found not only redundant but also detrimental. In this work, the conventional AVS-based DOA estimation pipeline is reconfigured by introducing a frame-wise-single-source clustering (FWSSC) step which is used to minimize the possible contaminated TF points consumed by the following step such as single source points (SSP) detection and direct path dominant (DPD). Outliers are then removed based on the results of FWSSC. In the proposed FWSSC, the intensity vector instead of the estimated steering vector is used for single-centroid TF point clustering. It is shown that due to the reduced number of potentially contaminated TF points, the accuracy and robustness of DOA estimation can be significantly improved, especially for the cases where the angular differences between the sources are small. The proposed DOA estimation pipeline is applicable to any TF analysis based algorithms.
Paper ID	:	1570750550:
Paper Title	:	Hardware-oriented Memory-limited Online Artifact Subspace Reconstruction (HMO-ASR) Algorithm
Authors	:	Lan-Da Van, You-Cheng Tu, Chiyuan Chang, Tzyy-ping Jung
Abstract	:	Recently, many algorithms have been proposed to remove elusive non-brain signals (as known as "artifacts") from electroencephalogram (EEG). However, the limited memory of portable devices can reduce the capabilities of artifact removal algorithms. To address this challenge, we propose an HMO-ASR algorithm. The proposed HMO-ASR algorithm consists of (1) two-level window-based preprocessing including PCA-based and modified z-score-based

preprocessing to clean the data in each window, (2) iterative mean, standard deviation, and covariance update using a parallel algorithm to achieve window-based processing, and (3) early eigenvector matrix determination to save the computation. The HMO-ASR method can be implemented with limited memory on mobile devices or application-specific integrated circuits using the three procedures described above. The study results showed that the proposed HMO-ASR algorithm can achieve comparable performance to those obtained by the offline ASR algorithm with 99.34% memory size reduction.

Date	:	24/11/2021 (Wednesday)
Session	:	Nano electronics, Devices and System Integration & Sensors and Interfaces & Automotive Circuits and Systems
Time	:	15:40 - 17:40
Session Chair	:	Haslina Jaafar, Universiti Putra Malaysia

Paper ID	:	1570747846:
Paper Title	:	SD-PUF: An Area Efficient PUF with Signature Improvement for STT-mCell Based Circuits
Authors	:	KW Xu, D Zhang, YQ Cheng
Abstract	:	As the hardware security gets more and more attentions, Physically Unclonable Function (PUF) has been proposed to provide chip authentication and Intellectual Property (IP) protection effectively. The conventional PUF requires many response clock cycles and independent PUF components, resulting in increased power consumption and area overhead. Recently, STT-mCell has emerged as a promising spintronic device to be used in logic circuit design with significant area and power benefits. However, it is challenging to guarantee the hardware security of this kind of STT-mCell based circuit. In this work, we propose a novel STT-mCell Delay based PUF design (SD-PUF) and exploit the unique manufacturing process variation (PV) on STT-mCell write latency. We introduce a new methodology to select appropriate logic gates in the all-spin chip to generate a unique identification key. Finally, a masking scheme is applied for signature improvement. The experimental results show that the uniqueness of the improved signature is 49.61% and the SD-PUF has significant area benefits over other designs.

Paper ID	:	1570729820:
Paper Title	:	A Single-ended Low Power 16-nm FinFET 6T SRAM Design with PDP Reduction Circuit
Authors	:	Chua-Chin Wang, Ralph Gerard Sangalang, I-Ting Tseng
Abstract	:	This investigation proposed an SRAM utilizing an ultra-low power cell, implemented using the 16-nm FinFET CMOS technology. Voltage supply selection of the static RAM cells is done by gating the wordline (WL) enable. There are two operation modes of the SRAM, i.e., the normal and standby mode. In standby mode, the cell wordline is not activated, where the cell operates on a lower voltage level so that the stored bit status is retained. This, in turn, lowers the power consumption of the cell in standby mode. On the other hand, the normal mode is activated when the wordline of the cell is enabled. In this mode, the cells are using the normal voltage supply of the system. Theoretical derivations and an all-PVT-corner post-layout simulations were provided for verification of the functionality and performance. An SRAM of 1-kb capacity is designed based on the propose cell. It is also featured a power delay

		product reduction circuit. The simulations show an energy per access of 11.8 fJ, which is the lowest to date.
Paper ID	:	1570742529:
Paper Title	:	MAGIC-Based Nonvolatile Binary Counters
Authors	:	Xingzhi Fu, Hui Xu, Yinan Wang, Wei Wang, Xi Zhu, Weihe Wang, Zhiwei Li
Abstract	:	Counter is one of the basic parts of a digital device. Traditional counters based on Complementary Metal Oxide Semiconductor (CMOS) cannot maintain the data after power down. It may require the extra power and time consumption to store the counting results in memory. Using non-volatile memory to construct the counter can solve these problems. In this paper, we design a 4-bit up-down counter by using the Memristor-Aided LoGIC (MAGIC) and auxiliary CMOS circuits. Furthermore, we verify the design through LTSPICE simulations. The simulation results show that the proposed counter operate correctly, that converts the counting result into a binary number, and stores them in the memristors. Compared with CMOS-based counters, this design has great advantages on area, power and nonvolatility.
Paper ID	:	1570720203:
Paper Title	:	A 118 dBΩ 190 MHz CMOS Transimpedance Amplifier Using Phase Compensator for MEMS Beam Oscillator
Authors	:	Hua Chen, Guoyong Li, Zhen Meng, Ke Liu, Yuepeng Yan
Abstract	:	This paper proposes an ultra-high-gain wideband CMOS transimpedance amplifier (TIA) for driving the ultrahigh-motional-resistance MEMS resonator. A phase compensator made by a tunable capacitor and resistors provides a lead phase compensation for the TIA. Moreover, the compensator produces a stable input bias voltage for the inverted-based Cherry Hooper amplifier, whose output bias is stabilized by tunable transistors. The common-gate amplifier uses a high-resistance load resistor to ensure a gain of 80 dBΩ, and the Cherry-Hooper amplifier uses a high-gm inverter and a high feedback resistor to provide a gain of 35 dB. A dual power supply of 1.2/1.8 V was used to save power. Based on the 0.18 μm CMOS process, the TIA simulation shows the gain is 118 dBΩ, the bandwidth is 190 MHz, the input-referred current noise is 20.9 pA/√Hz, and the power without test buffer is only 0.45 mW. The MEMS oscillator starts up within 0.5 ms with a swing of 1.128 Vp-p, and the phase noise is -96.59 dBc/Hz, 99.2 dBc/Hz at 10 kHz and 100 kHz offset, respectively.
Paper ID	:	1570738280:
Paper Title	:	A Readout Circuit for Tactile Sensor with Crosstalk Suppression and Non-Uniformity Compensation

Authors	:	Yao Li, Yiqiang Zhao, Mao Ye, Yong Chen
Abstract	:	This paper presents a high-performance readout circuit for tactile sensors based on the piezoresistance effect. Zero-potential and correlated double sampling methods are combined to suppress the undesired crosstalk issue, and the on-chip current digital-to-analog converter is proposed to compensate for the non-uniformity. Low-power successive-approximation-register analog -to-digital converter and customized serial peripheral interface are designed to perform digital quantization and communication. The prototype is fabricated in a 180-nm CMOS process, occupying an area of 4.8 mm² and consuming power of 285 μW at a 3.3-V/1.8-V supply. The chip is experimentally verified in a board system which achieves a non-uniformity compensation efficiency of 83%.

Paper ID	:	1570731817:
Paper Title	:	Process Compensated Diagnostic Circuit For Impending Fault Detection In SRAM Write Drivers
Authors	:	Swapnil Bansal, Anuj Grover
Abstract	:	In life-critical applications like automobile systems, functional safety is of utmost importance. Early diagnosis of unforeseen faults and failures in the memory subsystem is necessary to prevent any potential threat to life. It is observed that Electromigration induced ageing failures such as open and short resistive defects pose extreme reliability concerns in the safe operation of SRAMs. This paper analyzes the consequences of resistive defects in the Write Driver periphery circuit in 65nm technology node. In the presence of defects in a conventional write driver circuit using a Negative BL scheme, the writability and the bit line discharge level degrades, eventually leading to write errors. We propose a process compensated circuit to detect and locate small resistive faults, as low as 3-4KOhm, in SRAM write drivers, before they result in functional failure. The test circuit can be easily integrated with the memory BIST.

Date	:	25/11/2021 (Thursday)
Session	:	Analog and Mixed Signal Circuits and Systems 3
Time	:	11:15 - 12:35
Session Chair	:	Suhaidi Shafie, Universiti Putra Malaysia

Paper ID	:	1570750124:
Paper Title	:	A Low Power Sample-and-Hold Circuit with Improved Dynamic Bias for Pipelined ADC
Authors	:	Xiaodan Zhou, Tao Liu, Zehao Li, Yujie Wang, Xiong Zhou, Shiheng Yang, Liu Jiaxin, Qiang Li,, ,
Abstract	:	A low power and high-speed sample-and-hold (S/H) circuit which is suitable for the 16bit pipelined analog-to-digital converter (ADC) is proposed. By using the dynamic bias technique, The OTA in the S/H is realized with lower power dissipation. This S/H is fabricated in 0.18µm mixed signal CMOS process and occupies 0.128mm2. It is integrated in a 16bit 25MS/s pipelined ADC which delivers up to 96.2dB spur-free dynamic range (SFDR) and 75.5dB signal to noise and distortion ratio (SINAD) with 30.1MHz input tone, while the power dissipation is only 34.7mW.

Paper ID	:	1570731271:
Paper Title	:	Monolithic Implementation of Chaos Modulated VCO based Random Number Generator
Authors	:	Ömer Güngör, Salih Ergun
Abstract	:	This paper introduces the implementation of a monolithic random number generator. For that purpose, dual oscillator architecture with an irregular sampling of a regular signal is designed and simulated. The irregular sampling clock is generated by voltage controlled oscillator, which is modulated by a continuous-time chaotic oscillator. The proposed architecture is fully CMOS compatible and suitable for monolithic implementation. Therefore, it is robust against tempering attacks and external interference. It is designed in TSMC 180 nm process and requires a chip area of 0.004 mm2. To the best of the authors' knowledge, this work is the first monolithic implementation of chaos modulated VCO-based random number generator

Paper ID	:	1570735483:
Paper Title	:	CMOS Temperature Sensor Integrated with High-Speed 10-bit Differential SAR ADC
Authors	:	Siti Idzura Yusuf, Suhaidi Shafie

Abstract	:	Signal with noise could degrade the digital output of temperature sensor. This can be overcome by implementation of differential input signaling of ADC. Thus, this paper presents design and analysis of CMOS temperature sensor integrated with 10-bit differential SAR ADC to prevent noise signal effect. The circuit has been designed using 0.18µm CMOS process technology. The sensing circuit is based on bandgap reference (BGR) topology that generates complimentary to absolute temperature (CTAT) voltage. The proposed temperature sensor produced 1.89mV/^{o}C sensitivity with maximum accuracy ±1.0^{o}C.
Paper ID	:	1570721469:
Paper Title	:	Multi-Chips High-Speed and High-Voltage Amplifier
Authors	:	Wen Li
Abstract	:	A linear amplifying circuit with high voltage, high slew rate and wide bandwidth is presented in this paper. The circuit topology is by dividing the amplifier circuit into three chips and applying different substrate voltage to each chip so that the amplifier's maximum output voltage can achieve almost twice the withstand voltage. The circuit is verified with a 200V 0.25-um SOI-LDMOS process technology . The experimental result shows that the maximum output voltage can achieve 425 Vpp with the Slew rate of 1120 V/us and bandwidth of 2.3 MHz. The multi-chips hybrid amplifier is expected to be used for many industrial applications.

Date	:	25/11/2021 (Thursday)
Session	:	Biomedical and Healthcare Circuits and Systems
Time	:	11:15 - 12:35
Session Chair	:	Tang Tong Boon, Universiti Teknologi PETRONAS

Paper ID	:	1570730181
Paper Title	:	A 10-bit Current-Steering DAC for Urinary Bladder Volume Measurement
Authors	:	Yuki Nishimura, Akio Shimizu, Sumio Fukai, Yohei Ishikawa
Abstract	:	A 10-bit current-steering digital-to-analog converter (DAC) is proposed to measure a urinary bladder volume. The proposed DAC is composed of a 4-bit bull current DAC, a 4-bit push-pull current DAC, and a 2-bit push-pull current DAC. Since output voltage range of three DACs is limited for the urinary bladder volume measurement, the resolution and power consumption of DAC are reduced. The proposed DAC is fabricated by phenitec 0.6 µm 1P3M CMOS process.

Paper ID	:	1570724459
Paper Title	:	Fourier-Domain OCT Imaging Processor with Improved Memory Efficiency
Authors	:	Song-Nien Tang,
Abstract	:	This paper presents a display processing unit for the image formation of the Fourier-domain optical coherence tomography (FDOCT) system. Using the proposed design, the FDOCT imaging operations involving the re-sampler, the real-valued fast Fourier transform (RFFT) and the image display processing can be efficiently performed using a hardware processor, allowing high-frame-rate OCT image display with the direct generation of gray-scale image data. Compared to previous works, the proposed design improved the memory efficiency in terms of the RAM size, the control complexity and the logarithm table size for the re-sampler, the RFFT and the display processing units, respectively. The presented FDOCT imaging processor was verified using an FPGA-SoC platform through the software-hardware cooperation with accesses of the raw data obtained from the FDOCT front-end equipment.

Paper ID	:	1570738513
Paper Title	:	:A real-time correlational combination algorithm to improve SNR for multi-channel neural recordings
Authors	:	Liyang Wang, Sio-Hang Pun, Peng Un Mak, Achim Klug, Bai-Jun Zhang, Mang I Vai, Tim Lei
Abstract	:	This paper presents a Correlational Combination (CC) algorithm and its hardware implementation to be used in future multi-channel real-time spike sorting systems. Preprocessing of neural spikes are required to eliminate duplication for neural spikes

recorded from a neural probe with densely spaced recording channels. In this work, we proposed using Pearson's correlation to identify duplicated neural spikes and to combine them selectively to improve SNR for a representative spike prior to performing spike sorting. Other approaches (Single Selection and Average All) were also compared with simulated multi-channel neural spikes and CC has the highest SNR for both software and hardware implementations. A hardware implementation of the CC algorithm was realized with a Xilinx Zynq-UltraScale+ field programmable gate array (FPGA). A SNR improvement of 93% was achieved when compared to the other approaches. A processing latency of 1.58µs for the CC hardware module was achieved when a 250MHz system clock was used to drive the FPGA.

Date	:	25/11/2021 (Thursday)
Session	:	Power/Energy Devices, Circuits and Systems & Integrated Power Management Unit (PMU)
Time	:	11:15 - 12:35
Session Chair	:	Norhafiz Azis, Universiti Putra Malaysia Yongfu Li, Shanghai Jiao Tong University

Paper ID	:	1570732213
Paper Title	:	An Isolated ZVS DC/DC Converter with Diode-connected MOSFET in Rectifier
Authors	:	Najmehossadat Nourieh, Yichuang Sun, Oluyomi Simpson
Abstract	:	This paper presents an isolated resonant zero-voltage switching ZVS converter with a diode-connected MOSFET in a rectifier. The active resonant network is composed of a transformer leakage inductance, a resonant capacitor and a diode-connected MOSFET. The output capacitor of the main switches together with their reverse-recovery diodes provide zero-voltage switching condition for all switches. The input voltage/current of the proposed circuit is 0.35V/500uA while the output voltage/current is 1.5V/75uA. The simulated circuit in PSIM is presented to verify the proposed converter performance.

Paper ID	:	1570738551
Paper Title	:	Implementation of 12nm Graphene Flakes in TiO2/G Composite for High Power Conversion in DSSCs
Authors	:	Muhammad Afiq Bin Mohd Rizo Afiq Rizo, Mohd Amrallah Mustafa, Suhaidi Shafie, Haslina Jaafar, Wan Zuha Wan Hasan, Nasri Sulaiman ,
Abstract	:	Due to its high electron mobility, chemical characteristics, low cost, and environmental friendliness, graphene is a promising material and alternative way for achieving high performance in dye-sensitized solar cells (DSSCs). It is zero electron-volt energy bandgap allows it to improve electron transport efficiency and light absorption. The TiO2/G composite was synthesized by using the TiO2 process methodology. The different quantities of graphene flakes were applied and photovoltaic performance, internal impedance, and absorbance were determined. As a consequence, this graphene doping enhanced overall performance increased by 11.41% of its efficiency for a thickness of 13 compared with pure TiO2.

Paper ID	:	1570731957
Paper Title	:	:A 1.2μW, 1.7μV rms ECG acquisition IC with low-noise Amplifier and full-digital Heartbeat detector

Authors	:	Yanhan Zeng, Zhixian Li, Weijian Chen, Wei Zhou
Abstract	:	In this paper, a full-digital heartbeat detection system-on-chip (SoC) with low-noise analog front end (AFE)is presented. With the use of transconductance bootstrap and source degradation, the noise of AFE can be greatly reduced. The SoC is implemented in a 0.18μm CMOS process and consumes 1.2μW from a 1.2V supply, of which AFE and heart rate detector consume 0.8 μW and 0.4 μW, respectively. Besides, the noise from 1Hz to 1kHz is only 1.7 μVrms. The gain of instrument amplifier is 33dB, and the cutoff frequency of high and low frequency are 0.4Hz and 40kHz respectively.

Paper ID	:	1570731961
Paper Title	:	:A 2.8μA, sub-1μs output-capacitorless LDO with Transient Detecting Control
Authors	:	Tianxian Wu, Yanhan Zeng, Xu Li, Weijian Chen, Zhixian Li
Abstract	:	In this paper, a low power and fast transient response output-capacitorless LDO for digital applications is implemented in a 0.18-μm standard CMOS technology. An adaptive biasing class-AB amplifier circuit is proposed to provide both high gain and large slew rate with low quiescent current. Meanwhile, a push-pull slew rate enhance stage controlled by transient detecting control (TDC) generator is proposed to further improve the transient response of the proposed LDO. Simulation results show that the quiescent current is only 2.8μA and the settling time of the output voltage with the load current steps from 1mA to 50mA in a edge time of 1ns is less than 2μs. Moreover, the line regulation and load regulation are 0.727mV/V and 2μV/mA, respectively.

Date	:	25/11/2021 (Thursday)
Session	:	Analog and Mixed Signal Circuits and Systems
Time	:	14:45 - 16:25
Session Chair	:	Asrulnizam Abd Manaf, Universiti Sains Malaysia

Paper ID	:	1570731821
Paper Title	:	:A low-power 6-bit successive approximation register ADC using a new split capacitor array method
Authors	:	Noushin Ghaderi, Leandro Lorenzelli, Andrea Adami
Abstract	:	In this paper, the design of a 6-bits successive approximation register (SAR) analog to digital convertor (ADC) in 0.18 µm technology is presented. This paper proposes the new SAR based on the monotonic switching structure for single-ended input signal, in which the capacitors are just arranged at a single input node of the comparator. Therefore, the number of capacitors is decreased by half. In addition, the special split capacitor structure is merged with the monotonic switching to considerably reduce the capacitor size. Using the split capacitor method, the switching energy can be reduced by 37%, while by adding the proposed method to the split capacitor method, it will be reduced to the half value of the split capacitor method. In addition, due to the existence of smaller capacitances than the conventional split capacitor method, the settling speed and input bandwidth increase. A dynamic comparator is used to decrease the static power consumption of ADC. In addition, very low power D-FFs based on transmission logic are used in the SAR control logic part to further reduce the power consumption.

Paper ID	:	1570733465
Paper Title	:	:A Fully Integrated Low-Power Capacitive Sensor Frontend With Automatic Tuning Scheme
Authors	:	Mortaza Mojarad, Milad Diba
Abstract	:	In this paper, a reconfigurable low-noise fully integrated capacitive sensor frontend with an on-chip tuning scheme is proposed to enhance the flexibility, reliability, and accuracy with a low power consumption. The sensor frontend is composed of a charge sensitive amplifier with a new reset network followed by three band-pass amplifiers to further amplify the output signal and also to achieve a Gaussian pulse shaping. The frontend can process the signals of both polarities and the effect of the sensor dark current on the output is negligible. The readout circuit is simulated using a standard 0.18 µm CMOS process. The post-layout simulation results prove a highly tunable conversion gain and show a maximum value of 25.7 mV/fC and equivalent noise charge (ENC) of about 106 e-rms with a power consumption of 371 µW.

Paper ID	:	1570748671
Paper Title	:	Analysis and Optimization of Sense Amplifier for Compute SRAM
Authors	:	Jian Chen, Wenfeng Zhao, Yuqi Wang, Yajun Ha
Abstract	:	In-SRAM computing generally presents a very distinct bitline discharging behavior, so that a suitable sensing topology is vital for the good performance of a compute SRAM. Two recent sensing topologies, namely the symmetric single-ended sensing amplifier (SA) and the asymmetric differential SA, have been proposed in previous designs. However, it is not so straightforward to see which of the two sensing topologies is better in terms of read delay and read energy consumption, and no previous work has ever had a clear answer to this. In this paper, we perform a comprehensive analysis of these two sensing topologies, and find that the asymmetric differential SA performs faster than the symmetric single-ended SA. In addition, we propose an improved asymmetric differential SA with a novel pre-charging scheme. Compared to the state-of-the-art, experimental results show that our proposed SA has reduced its read delay by 17% and the total read energy by 8%, in an 8Kb compute SRAM using a 55nm CMOS technology.

Date	:	25/11/2021 (Thursday)
Session	:	Electronic Design Automation & High Speed and Optical Wire lined Circuits and Systems
Time	:	14:45 - 16:25
Session Chair	:	Kalai Selvan Subramaniam , Infinecs Systems Sdn. Bhd

Paper ID	:	1570721340
Paper Title	:	A Game Theory Model for Multi Robot Cooperation in Industry 4.0 Scenarios
Authors	:	Elvina Gindullina, Eleonora Peagno, Giovanni Peron, Leonardo Badia
Abstract	:	Multiple autonomous robots are expected to interact in Industry 4.0 scenarios, which makes it key to identify distributed techniques for their control and coordination. Game theory has a strong potential to be an excellent representation methodology for the establishment of cooperation among distributed robotic agents. In this paper, we consider a model of two industrial robots within a production line and we show how to describe their interaction, with their different objectives and control being kept into account. We also formalize a Bayesian game that takes into account imperfections in the system, such as the possibility that the robots make a wrong evaluation on a specific item in production. For both the standard static game and its Bayesian version, we compute the Nash equilibrium and we argue how it ultimately represents a point of convergence of the distributed control of the robots.

Paper ID	:	1570750108:
Paper Title	:	Theoretical and Experimental Analysis of Traveling Salesman Walk Problem
Authors	:	Yasuhiro Takashima, Yuichi Nakamura
Abstract	:	In this paper, we formulate Traveling Salesmen Walk (TSW) problem as integer linear programming. Traveling Salesman Problem is one of the most popular combinatorial optimization problems. However, one constraint is too strict to use this problem for the practical situation. Thus, we transform the problem to the TSW problem by relaxing the constraint. To solve TSW, we formulate it as integer linear programming (ILP). We confirm the resultant tour of TSW is 12\% shorter than that of TSP, empirically. We also propose Unsatisfaction of Triangle Inequality as the measurement of the hardness of Traveling Salesman Problem variants. We also confirm that there is a correlation between the ratio of unsatisfying triangle inequality and the optimization run-time, empirically.

Paper ID	:	1570749596

Paper Title	:	Scalable Synthesis of 3-D Crossbars for Flow-based Computing
Authors	:	Dwaipayan Chakraborty, John Pruden
Abstract	:	Faced with the demise of Moore's law, the field of computer architecture is currently undergoing rapid evolution. Emerging devices, like memristors, play a crucial role in this development. Computer design is a computationally challengingask, but the tools that currently exist for designing memristor-based computing units produce designs that are slow, or power-hungry, or both. In this paper, we propose a design automation techniques which are uniquely geared towards a low-latency, low-power variant of memristor-based computation. We develop logical operations between crossbars which exploit sneak paths as a computational mechanism, and leverage the compositional power of and-inverter graphs for scalable synthesis of crossbar circuits which utilize these fundamental operations as building blocks. In order to take advantage of the latest developments in fabrication, we devise a method to build 3-D crossbars while maintaining functionality. Designs produced by our method outperform state-of-the-art designs in the average case, and by several orders of magnitude in the best cases.
Paper ID	:	1570723200
Paper Title	:	A 720-mVpp 224-Gb/s PAM4 Optical Receiver with Multiple Peaking Techniques in 130-nm SiGe BiCMOS
Authors	:	Zhang Qiu,
Abstract	:	This work discusses a large output-swing 224-Gb/s PAM4 optical receiver with multiple peaking techniques in 130-nm SiGe BiCMOS. The receiver consists of a trans-impedance amplifier (TIA), a continuous-time linear equalizer (CTLE), and a 2-stage single-to-differential converter (S2D). An RC parallel structure is implemented in the TIA, effectively broadening the bandwidth. Moreover, multiple peaking techniques, including RC emitter degeneration, shunt-inductive peaking and T-coil peaking, are adopted to extend the bandwidth to 61 GHz. To minimize the output mismatch, inductors in S2D are typically chosen in different magnitude. Consuming 96.85-mW power, the designed system achieves a differential conversion gain of 58 dBΩ, while the imbalances in amplitude and phase are limited to 0.2 dB and 1.6°, respectively.
Paper ID	:	1570731929
Paper Title	:	100-Gb/s PAM-4 VCSEL Driver and TIA for Short-Reach 400G-1.6T Optical Interconnects
Authors	:	Nan Qi, Donglai Lu, Jian He, Weizhong Li, Jian Liu, Xi Xiao, Liyuan Liu, Nanjian Wu, Yong Chen, Sikai Chen, Ningmei Yu
Abstract	:	This paper presents a chipset with a multichannel vertical-cavity-surface-emitting laser (VCSEL) driver and a trans-impedance amplifier (TIA) in a 180-nm SiGe BiCMOS process. With the target of 400G-1.6T short-reach applications, a high-speed linear gain is developed for fourlevel pulse amplitude modulation (PAM-4). The VCSEL driver employs a second-order continuous-time linear equalizer to compensate for non-linear input channel loss, while

exploiting an RC-degenerated output stage with inductive shunt peaking to extend the bandwidth. The TIA uses the resistive feedback topology along with a series-peaking inductor to improve its input bandwidth. The measurements show that the VCSEL driver operates up to 100 Gb/s with a 280-mVpp PAM-4 signal. The TIA scores a 61.5-dBΩ trans-impedance gain, a 36-GHz BW and a 16-pA/√Hz averaged input-referred noise.

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After a careful reviewing process, all accepted papers after proper registration and presentation, will be published in the APCCAS 2022 Conference Proceedings, which will be published by IEEE and being archived into IEEE Xplore. Selected papers are invited to submit extended full papers to IEEE Transaction on Circuits and Systems I (TCAS-I), IEEE Transaction on Circuits and Systems I (TCAS-II) or IEEE Open Journal of Circuits and Systems (OJCAS).

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Easychair System: http://www.easychair.org/conferences/?conf=apccas2022

Important Dates

- Submission Deadline: July 21, 2022
- Notification Date: September 1, 2022
- Conference Dates: Nov.21-25, 2022

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