Book of Abstracts

3rd International Conference

on

IEEE Electron Devices Kolkata Conference (EDKCON 2024)

Organized by
IEEE EDS Kolkata Chapter

30th November- 1st December, 2024

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About EDKCON Series of Conference:

Organized by IEEE EDS Kolkata Chapter, EDKCON series of Conferences is expected to bring together researchers, educators, students from across academia, government, industry, and non-governmental organizations to discuss, share and promote current works and recent accomplishments across all aspects of Electron Devices, circuits, Nanotechnology and VLSI. This conference provides a platform for researchers and practitioners to explore how nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices, optoelectronic devices, low power devices, high-speed devices, process technology, device modeling and simulation, VLSI and embedded system can drive disruptive advancements for the next generation.

Key Factors of the EDKCON 2024

- **EDKCON 2024** brings together researchers, educators, students from across academia, government, industry and non-governmental organizations to discuss share and promote current works and recent accomplishments across all aspects of the **Electron Devices, Circuits, Nanotechnology and VLSI**.
- **Low Registration Fee with waiver for IEEE Members** (IEEE Member=Rs 6500.00; Non-IEEE member= Rs 7000.00; IEEE Student Member= Rs 5000.00; Non-IEEE Student member = Rs 6000.00)
- Received a **large number of submissions** (**a total of 508 submissions**)
- Assigned A Total **181 Reviewers** from India and Abroad. Approx. 25% of total Reviewers are from Abroad and the rest are from India.
- Each manuscript has been reviewed twice or thrice. In brief almost 38**% of the total papers have been reviewed thrice**.
- **Acceptance ratio is 29.5% (150 out of 508) which is in line with the top tier international conferences**
- Each and every manuscript has been checked for Plagiarism and Similarity Reports have been generated using the **iThenticate CrossCheck or Turnitin**
- To enhance the quality of the conference, **1 Plenary Talks, 9 key note Talks and 32 Invited Talks** have been scheduled in EDKCON 2024.
- All the accepted papers will be submitted for possible consideration to be included into **IEEE Xplore** after being presented in the conference (as per IEEE No show policy)
- A Total **Six journals (2 SCI, 2 Scopus and 1 ESCI)** have shown their interests to publish the extended version of selected papers from EDKCON 2024.
- 1 **Tutorial Session (Topic: SMART FACIAL RECOGNITION SYSTEM DEPLOYMENT USING AMD XILINX PYNQ FPGA BOARD):** EDKCON 2024, in collaboration with the IEEE Electron Devices Society (IEEE-EDS) is offering education short courses with hands-on tutorial at the conference.
- **Design Contest:** A design contest held by EDKCON 2024 **to provide a platform to showcase innovative hardware and software solutions to real-world problems**. Whether it's enhancing efficiency, promoting sustainability, improving accessibility, or addressing societal challenges, EDKCON 2024 providing scope to exhibit the creative ideas come to life.

List of the Invited Speakers at EDKCON 2024

Jacopo Iannacci, PhD
MicroSystems Technology Research Unit, Center for Sensors and Devices (SD), Fondazione Bruno Kessler, Italy
Title of the talk: A fresh concept of Hardware supporting the transition to 6G and Future Networks – Pivoting on Micro/Nanotechnologies

Prof. (Dr.) P. K. Basu
Ex-Professor, Institute of Radio Physics and Electronics, Calcutta University, India
Title of the talk: Acharya Jagadish Chandra's Light Tunnelling Experiment and Its century-long impact on Electronics, Communication and Physics

Dr. Rajnish Sharma
Vice Chancellor, Chitkara University – Himachal Pradesh, India
Title of the Talk: Exploring novel materials using Quantum ATK tool for diverse electronic applications

Dr. T. R. Lenka
Associate Professor, Department of Electronics and Communication Engineering, National Institute of Technology Silchar
Title of the talk: III-Nitride/β-Ga2O3 Nano-HEMT for Emerging Nanoelectronics Applications

Dr. Koushik Guha
Head of Department of Electronics and Communication Engineering, Associate Dean (Academic), Former Associate Dean (Students Welfare), National Institute of Technology Silchar
Title of the talk: Intersection of biology, medicine and engineering: venturing into a new era of research

Dr. Shubham Sahay
Dept. of ECE, IIT Kanpur
Title of the talk: Neuromorphic Computing: Quo Vadis?

Dr. Ratul Kr Baruah, F-IETE, SM-IEEE

Associate Professor, Electronics and Communication Engineering, Tezpur University, Assam-784028, INDIA

Title of the talk: Interconnects for Large-Area Flexible Circuits

Dr. Rupam Goswami, SM-IEEEE

Asst. Professor, Electronics and Communication Engineering, Tezpur University

Click here to view the short CV of Dr. Rupam Goswami

Title of the talk: Random Telegraph Noise in MOS Transistors

Dr. Sitangshu Bhattacharya

Assistant Professor, Department of Electronics and Communication Engineering

Indian Institute of Information Technology

Title of the talk: Ultrafast electron-hole recombination in two-dimensional transition metal di-chalcogenides

Prof. Chayanika Bose

Professor, Jadavpur University, Kolkata, India

Title of the Talk (WIE Session): Semiconductor LASER

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Effect of Hole Transport Layer on Tin based Perovskite Solar Cells

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Abstract- Due to the adverse effect of lead in the atmosphere scientist developed a tin based perovskite absorber in hybrid perovskite solar cell. Hybrid perovskite solar cell will be the new replacement for Si based solar cell. In this paper, an numerical analysis of different organic and inorganic hole transport layer (HTL) in Tin based perovskite solar cell. Basically Organic HTL (Spiro-OMETAD) and Inorganic HTL (Cu_2O, NiO, CsSCN) material has been used in this Tin based perovskite structure. The thickness (in µm) and electrons affinity (in eV) of the different HTL layer also varied and observed the result. As per numerical simulation perform by Scaps-1D, we can conclude that highest PCE obtain by thickness variation for NiO is 23.93and also it maintain its efficiency throughout the thickness variation of .050 µm to .350 µm thickness also we can observed that under electron affinity variation highest PCE obtained by Cu_2O (electron affinity 3.40eV) is 24.12%.So we can conclude that for ZnO as an electron transport layer we can use inorganic HTL (Cu_2O, NiO) to obtain better efficiency compare to organic HTL(Spiro-OMETAD).

***Keywords*: Electron transport layer, Hole transport layer, Hybrid Perovskite Solar cell**

Investigation of Analog and Digital Performance for Gallium-Arsenide GS GAA FETs

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Abstract: This paper investigates the effectiveness of GaAs as a fin material for both analog and digital applications in GaAs Gate-Stack Gate-All-Around FinFET with spacers. Various analog and digital parameters such as drain current, I_{on}, I_{off}, switching speed, SS (subthreshold swing), g_m (transconductance), output conductance, transconductance generation factor (TGF), intrinsic gain (A_v), early voltage, C_{gg} and Cut-off Frequency have been examined. The simulated results indicate that incorporating GS and high-k gate spacers significantly enhanced the device's DC and AC performance metrics.

***Keywords:** High-K Gate Spacer (ZrO_2), Gallium Arsenide (GaAs), Gate Stack, GAA FinFET.*

Reliability Study of Interface Traps in Gate-All-Around Tunnel FET: A TCAD Simulation Approach

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Abstract: Threshold voltage hysteresis in transistor characteristics is common for CMOS device reliability. Scaling impacts electrostatic performance, prompting reliability analysis. A key check involves varying gate voltage sweeping frequency to observe hysteresis changes. This phenomenon is often not fully discussed. Our study focuses on trap charging/discharging at the silicon channel-insulator interface of gate-all-around tunnel field-effect transistors (GAA TFETs), using Silvaco ATLAS TCAD. We model interface traps causing threshold voltage instabilities, analyzing energy band diagrams, trap occupancy probability based on gate voltage, and its impact on transfer characteristics' sweep. We explore hysteresis changes across sweep frequencies, temperatures, and gate voltage ranges.

Keywords*: Hysteresis, reliability, charge trapping, sweep frequencies, CMOS*

Theoretical Study of Optoelectronic Nanoparticles Optical Absorption Enhancement

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Abstract: In optoelectronic substances, whose energy band configurations are dictated by the Kane three band model, we have shown using operator algebra, the amount of light absorbed per thickness is proportional to the square root of $\left\{(\hbar\omega)^2-\left(E_g\right)^2\right\}$ ($\hbar\omega$ and $\left(E_g\right)$ represent the energy of incident radiation and band-gap, respectively), rather than $\left\{(\hbar\omega)-\left(E_g\right)\right\}$, as is commonly known in the literature.

Keywords*: Kane three band model; optical absorption coefficient; optical matrix elements.*

Examining the Effect of Size-Dimensional Nanoparticles on Susceptibilities in Two-Dimensional (2D)

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Abstract: We examine the dielectric and quantum wells susceptibilities to magnetic fields constructed of CdS, CdSe, and CdTe materials under parallel magnetic fields, in light of a recently proposed law of electron-dispersion. We note that the susceptibility ratio in this instance departs from the widely renowned 33% rule and that the quenching of diamagnetic susceptibility takes place at a crucial zone.

Keywords: *Quantum wells; magnetic susceptibilities; quenching*

Nonlinear Molecular Quantum Dynamics in an Entirely Nonhomogeneous DNA Chain Voltage

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Abstract: The double helix in this instance is demonstrated to voltage more readily because to the kinks fashioned through the restricted cavity of base -pairs. A restock causes a quantum phase transition (QPT), which results in denaturation. When the temperature effect is full into consideration throughout the refill phase, the structural properties of B- DNA may be diagrammed by means of the Heisenberg-spin-system (HSS). The replenishment results in the non-equilibrium effect in the quantum phase transition and defects such as kinks and antikinks, whose temperature-dependent density levels and replenishment time, respectively. Furthermore, defects like as kinks and antikinks, which symbolize dynamic voltage of the flexible bar and correspond having an axis voltage in the DNA molecule, are created as a result of local denaturation brought on by replenish-induced quantum phase transition. Here, it is proposed that applying this conclusion to the DNA rod-like-chain (RLC) model will produce voltage as a result of these faults.

Keywords*: Kinks; DEOXYRIBONUCLEIC ACID; voltage; Quantum phase transition*

Comparative Study of Performance Analysis on Secure DSSS Multiuser Detection Under Near-Far Environment

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Abstract:
The research presents a practical, inexpensive method for improving communication in Direct Sequence Spread Spectrum (DSSS) multiuser systems rather than single users to address the near-far issue in CDMA systems. There are numerous security applications for the current telecommunication system's hearability issue, which needs to be improved. This work proposes a comparison analysis of Bit Error Rate (BER) vs. Signal to Noise Ratio under near-far environments using the Multi User Detection Decorelator (MUD-Decorrelator) & MUD-Decision Feedback method.Instead of employing a single user and a MUD-Decorelator, the modulated signal's BER is changed via a MUD-Decision Feedback system. Both approaches' transmitted and received Power Spectral Densities (PSD) indicate that the signal's properties have not changed. To make clear the security of the systems and signals, the intermediate PSD is also shown here. This study presents an illustrated performance analysis of the MUD-Decorelator method and the MUD-Decision feedback approach.

Keywords:
BER; Signal to Noise Ratio; PSD; Near-far; CDMA; DSSS; MUD-Decorrelator; MUD-Decision Feedback

ASIC Flow Implementation on a 32-bit RISC-V Processor using Cadence

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Abstract- This document presents the design and ASIC flow implementation of a single-cycle microarchitecture of RV32I. RISC-V is chosen for its open-source ISA, which makes it accessible without any cost and offers similar capabilities as proprietary architectures like ARM and x86. The RV32I microarchitecture was designed using Verilog and comprises modules such as Instruction Fetch, Register Memory, Instruction Memory, ALU, and Control Unit. The functionality of the design was verified in Cadence Simvision tool, and it was compiled and elaborated in Cadence NClaunch tool. The design was synthesized error-free in Cadence Genus tool using TSMC 45nm technology libraries. The RTL design was validated by performing a Logic Equivalence Check (LEC) in Cadence LEC-Conformal tool, which verified that the design is perfectly mapped to gate-level netlist. Physical design was implemented in Cadence Innovus tool, and the timing of the design was verified in Cadence Tempus tool using the constraint files provided by TSMC 45nm technology.

Keywords- *RV32I, RISCV, ARM, ISA, RTL, Verilog, LEC, STA.*

Integration of Metallic Moth-Eye Nanostructures for Enhanced Photovoltaic Efficiency in All-Inorganic Perovskite Solar Cells

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Abstract: All-inorganic halide perovskite absorbers promise to revolutionize perovskite solar cells (PSCs). Utilizing the finite difference time-domain methodology of Lumerical suite, this study reports analysis and comparison of optical performances of all inorganic halide PSCs comprising different metallic moth-eye nanostructures in the $CsPbI_3$ absorber with its planar counterpart. Our results reveal that incorporation of Ni moth-eye nanostructure facilitates superior light absorption, enhanced short circuit current density (59.89 mA/cm^2), increased generation rate (1.25×10^{28} $m^{-3}s^{-1}$), which eventually results in a high ultimate efficiency of 32.26% for ITO/TiO_2/$CsPbI_3$/Spiro OMeTAD/Al PSCs. Notably, the integration of Ni moth-eye nanostructures yields better photovoltaic performance compared to other metals such as Al, Au, and Ag. This advancement underscores the potential of meticulous solar cell design to boost the efficacy of all inorganic PSCs further.

Keywords*: Solar cell performance; All-inorganic perovskite solar cell; moth-eye nanostructure; FDTD Simulation*

Study of Three-Subband Electron Mobility in AlGaAs based Semi-Non-Square Quantum Well Structures

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Abstract: We study the effect of semi-non-square potential profiles, such as semi-parabolic (SP) and semi-cubic (SC) on multisubband electron mobility μ under the influence of externally applied electric field F in $Al_xGa_{1-x}As$ based quantum well (QW) structures. Here, different scattering mechanisms are taken for computation of μ such as ionized impurity (ii-) and alloy disorder (al-) producing mobilities μ^{ii} and μ^{al}. A maximum of three subband occupancy is achieved. Interestingly, as F enhances from -20 kV/cm, μ increases with F and shows step-like increments at the subband transitions. However, μ decreases with an increase in F during double and single subband occupancy. The results show that μ (SCQW) > μ (SPQW) for all values of F. This is mainly due to the dominance of al-scattering in SPQW compared to SCQW. Additionally, the increased number of occupied subbands introduces more scattering channels in QW which significantly affects μ.

Keywords*: Semi-Parabolic; Semi-Cubic quantum well; multisubband electron mobility; intra- & inter-subband scattering*

Horticulture 4.0: Transforming Agriculture with IoT-Based Need-Specific Irrigation

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Abstract: — India, being a case of a water crisis growing at an exponential rate due to inefficient irrigation practices, needs innovative solutions. Conventional manual irrigation has been running off at a rapid speed, depleting the groundwater and putting at stake agricultural productivity and food security. Studies say that, by 2050, India is going to face serious water shortages. This paper presents an IoT-based irrigation system for addressing this challenge. Since this system can exactly monitor the content of water in the soil, need-based irrigation can be enabled, optimizing water utilization without overdose or underdose. This solution, based on open-source hardware, is a very cheap way to revolutionize agriculture.

***Keywords**: Horticulture, IoT, Irrigation, Cloud, Sensors*

Systematic Optimization of $InBi_2S_4Cl$ Absorber Layer in Perovskite Solar Cells for Enhanced Photovoltaic Performance

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Abstract: In this study, a new perovskite solar cell utilizing $InBi_2S_4Cl$ as an absorber layer has been developed and optimized owing to its superior optical and electrical properties. Both the photovoltaic (PV) performance and the stability of the cell were significantly improved. The optimization process was conducted using SCAPS 1D software. By systematically varying and optimizing the thickness (0.1 to 1 µm) and bulk defect density (BDD- 1×1010 to 1×1014 /cm3) of the absorber layer, the optimized cell achieved the following PV parameters: VOC of 0.67 V, JSC of 18.51 mA/cm², fill factor (FF) of 67.26%, and power conversion efficiency (PCE) of 10.91%.
***Keywords**: Simulations; perovskites; optimization; scaps -1d.*

Bandwidth Improvement of Slits-Slots with DGS Circular Patch Antenna for Wireless Communication

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Abstract: Wideband antennas are important components in modern communication systems, offering flexibility and efficiency across various applications Microstrip antenna is very popular because of its good performance, high gain, wide bandwidth, small size etc. in this designed antenna a wideband microstrip antenna with slits-slots cut into the circle-shaped patch. The simulated antenna is resonant at the frequency of 3.2 GHz from the frequency range of 2.67 GHz to 4.97 GHz. The proposed wideband antenna has achieved a gain of 2.34 dBi, reflection coefficients of –37.18 db and VSWR 1.0 respectively, at the resonant frequency of 3.2 GHz. Simulated antenna also achieved good bandwidth of 2.3 GHz. Defected Ground Structure (DGS) technique has been used in the ground layer for achieving the wide bandwidth. This simulated wideband microstrip antenna could be used in Wi-Fi (IEEE 802.11ac), LTE, and emerging 5G wireless communication.

Keywords*: Microstrip Patch Antenna; Slits-Slots; Bandwidth; Defected Ground Structure.*

Comparative Analysis of Power Consumption and Transistor Current for 6T And 9T SRAM

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Abstract: This study examines the differences in transistor current flow and power consumption between 6T and 9T SRAM cells. With an emphasis on energy efficiency, it assesses both transient and DC power usage during read and write operations. In order to gain insights into reliability and performance, transistor current flow during these processes is also measured. The results help to optimize memory architectures for performance and energy economy..

Keywords*: power consumption, energy efficiency, read and write operations, optimization*

Design of T-shape Tunnel FET with Enhanced Drain current Characteristics at 30nm Technology

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Abstract: Conventional field-effect Transistors (FETs) exhibit suboptimal energy efficiency, whereas tunnel Field-Effect Transistors (TFETs) represent a novel category characterized by significantly enhanced efficiency. TFETs leverage a distinct quantum mechanical phenomenon for electron transportation, enabling operation at notably reduced voltage levels. Integration of TFETs with Complementary Metal-Oxide-Semiconductor (CMOS) technology holds the promise of substantially reducing power consumption in integrated circuits. The assessment of a novel transistor architecture's functionality hinged on an analysis of its electrical characteristics. The investigation revealed minimal leakage current during the off state (desirable) and efficient conduction in the on state (favorable). Notably, the transition between on and off states was found to be exceptionally precise. The research endeavor is centered on characterizing surface potential and electric field through the solution of Poisson's equation, employing a parabolic approximation technique for constructing an accurate device configuration. To affirm the validity of the proposed framework, the analytical outcomes are juxtaposed with data derived from Synopsys TCAD simulations.

Keywords*: T-Shape TFET, Tunnelling, Threshold Voltage, transconductance, current ratio, Synopsys Santurus EDA Tools, Origin Pro Tools.*

Asymmetrically doping dependent Nonlinear Electron Mobility in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ wide quantum well MODFET structure

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Abstract: A cusp like nonlinear electron mobility is obtained in $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ based quantum well (QW) MODFET structure by asymmetrically varying doping concentrations nd1 and nd2, keeping (nd1+nd2) unchanged. The modified subband wave functions yield oscillatory subband mobility via inter-subband interactions. Our results explore the effect of doping asymmetry on QW-MODFET structure.

Keywords*: Wide quantum well (WQW), Oscillatory subband mobility, Subband wave functions, $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ quantum well MODFET structures (QW-MODFET).*

Performance Analysis Of Magnitude Comparator Using An Adiabatic Technique

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Abstract: As the complexity of System-on-Chip (SoC) designs continues to advance, the challenges associated with power dissipation and heat generation become increasingly pronounced. To enhance power optimization, there's a growing need for innovative energy-saving techniques. Furthermore, the usage of low-power arithmetic circuits has become essential in the development of cutting-edge computing devices. Regular conventional VLSI circuit design techniques based on static CMOS logic gates and synchronous clocking methods suffer from high static and dynamic power consumption, limited energy efficiency, and challenges in implementing clock gating. Static power consumption, where power is dissipated even when the circuit is idle, can be a major concern in battery-operated devices. Dynamic power consumption is a result of charging and discharging capacitors during signal transitions. In contrast, adiabatic logic introduces an innovative solution by minimizing energy dissipation during switching events. This approach significantly reduces both static and dynamic power consumption, making it a more energy-efficient choice for power-constrained applications. Additionally, adiabatic logic mitigates clock gating challenges and offers an avenue to enhance the overall energy efficiency of Very Large-Scale Integration (VLSI) circuits. Adiabatic techniques, therefore, have become essential in modern VLSI design, addressing critical power optimization concerns while maintaining or even improving performance levels. In this paper, our focus is on designing an ECRL(Efficient Charge Recovery Logic) based magnitude comparator using 32nm CMOS transistors technology. The designed comparator is then realized and implemented in LT SPICE and then compared with conventional magnitude comparator.

Keywords: *magnitude comparator;adiabatic technique; power dissipation;Efficient charge recovery logic;LT spice*

Performance Analysis of Biosensor Based on Inverted T shaped Junctionless FinFET

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Abstract: This paper shows a comprehensive investigation on detecting biological species using a junctionless FinFET with an inverse T-shaped fin, designed at the 14 nm technology node. The device features a 4 nm nano-cavity on each side of the channel, positioned between the gate and the fin. This cavity serves as a sensor for biological molecules. To minimize leakage current, the proposed structure incorporates a double oxide material surrounding the channel and cavity. The cavity is designed with a rectangular shape. The analysis, conducted using a TCAD simulation tool, focuses on the sensitivity of the biosensor. Different biomolecules, including Keratin (K=8), Streptavidin (K=2.15), Aminopropyltriethoxysilane (APTES), and, are examined to assess the biosensor's performance. The results demonstrate the device's potential for highly efficient and accurate biosensing by analyzing its electrical characteristics, sensitivity, and detection limits. Proposed biosensor shown the 42% higher sensitivity when the no charge particles added in the cavity and dielectric constant vary from 2.15 to 8.

Keywords: *biosensor, Inverted T shaped, threshold, Sensitivity Mosfet, Technology Computer-Aided Design*

Predictive Modeling for Bandgap Tuning in Perovskite Solar Cell using Machine Learning

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Abstract: Perovskite solar cells (PSCs) have rapidly advanced, gaining attention for their high efficiency and affordability. In this paper, we have used machine learning (ML) models to analyse extensive data on perovskite compositions and bandgaps, aiming to identify optimal material combinations to enhance PSC performance. We have developed a ML-based approach focused on bandgap tuning, which has been a crucial factor for maximizing the photo conversion efficiency of PSCs. Traditional methods have often involved time-consuming and resource-intensive trial- and-error methods. In contrast, our approach using ML models have streamlined this process, significantly reducing the resources and time required for bandgap optimization, making PSC production more efficient and cost-effective. We have implemented three ML models—Linear Regression, Random Forest, and Neural Networks, to predict bandgap values from a comprehensive dataset of perovskite compositions. Our results have indicated that Linear Regression has outperformed the others, achieving a root mean square error (RMSE) of 0.0031 and a Pearson Correlation Coefficient of 0.99997, demonstrating precise and reliable predictions. By utilizing machine learning–based prediction, this work has not only reduced reliance on traditional methods but also accelerated the development of high-performance PSCs, contributing to the ongoing evolution of sustainable and economically viable solar energy solutions.

Keywords*: Machine Learning, Perovskite Solar Cell, Bandgap tuning, Property prediction*

An Integrated Framework for Real-time Analysis and Observability of Wireless Sensor Data Using AWS Edge Service Capabilities

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Abstract: Wireless sensor networks generate vast data offering insightful information for applications from industrial monitoring to smart cities. Wireless sensor network assisted internet of things has got many applications and the expansion in this field mandates efficient data management and processing. Optimizing energy consumption in these networks is critical for increasing the efficiency and lifespan of these networks. Earlier cloud computing methodology usually faces challenges in bandwidth, latency and reliability. This research work encompasses edge computing in wireless sensor networks and its benefits in processing huge data using AWS IoT Greengrass and explores the novel use case of visualizing AWS sensor data with AWS Quick Sight. Integrating AWS IoT services and Quick Sight demonstrates how organizations may reduce wireless sensor data energy consumption by outsourcing data processing, sustaining efficiency, and acquiring significant information for enhanced performance. Visualization gives meaningful insights to the data, and it will help in taking informed decisions. The implementation of edge computing will reduce network congestion and lessen costs related to infrastructure. This is a key factor which not only improves the performance of IoT applications but also helps in scalability of cloud-based infrastructure. The comparative study of edge computing and traditional cloud computing highlights better latency, efficiency, reliability and scalability. By combining wireless sensor networks and AWS IoT services a significant advancement is made towards intelligent and sustainable IoT systems.

Keywords*: AWS Quick Sight, AWS IoT Greengrass, Edge Computing, Internet of Thing, Wireless sensors.*

Study the improved efficiency of the Lead-Free CsSnI3 Perovskite Solar Cells with variation of absorber layer in SCAPS-1D

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Abstract: *In this research work, a novel orderly study was conducted to explore the different parameters effect of thickness of the protection tier on adeptness of the FTO/TiO_2/$CsSnI_3$/Cu_2O/Au Perovskite solar cell by SCAPS-1D. To realize the optimized power conversion efficiency (PCE), acceptor density of the Perovskite absorption layer is (N_A=2×10^{19} cm^{-3}) with a 40nm TiO_2 layer, 300 nm for the Perovskite absorption layer ($CsSnI_3$) and 10 nm Cu_2O as HTL, with Au as electrode. After optimization process, efficiency reached from 13.60% to 17.17%. A result indicates the enhancement performance of the Perovskite solar cells (PSC).*

Keywords: *Perovskite, Electron Transport layer, CsSnI3, SCAPS-1D, ZnO:Ga.*

Advanced Gas Sensor Design: A Machine Learning Perspective on Photonic Crystals

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Abstract: A machine learning based novel approach has been proposed to design a photonic crystal (PhC) based gas sensor for the detection of SF_6, CH_4, and CO_2. In this work, we have implemented both the algorithm Support Vector Machine (SVM) and Random Forest (RF) and compared both classifiers, achieving the highest accuracy of 97.01% for SVM in case of gas classification. We have designed the sensor integrating machine learning models for real-time classification. We have run extensive simulations that provide dataset over a wide range of temperatures and pressures. Using this dataset, we have trained and optimized SVM and RF classifiers. The accuracies of gas detection get improved with machine learning along with simple sensor designs, which then presents an effective tool for density prediction. This work has opened pathways toward developing efficient, compact, and highly accurate gas sensors for environmental applications.

Keywords: *Photonic Crystal; Gas Sensor; Machine Learning; Gas Detection; SVM; RF.*

Hardware Implementation of Two level Authentication Algorithm using Cryptography with Steganography for Text-Image Security

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Abstract: This paper proposes two level authentication for an image communication through world wide web. The algorithm presented here mainly consist of techniques combined with symmetric key cryptography and LSB based steganography. Here two factor authentication are used that requires two forms of identification to access sensitive data. Symmetric key algorithms are algorithm for cryptography that use the same cryptographic keys for both the encryption of plaintext and the decryption of cipher text to maintain a private and secure communication. LSB steganography is commonly used technique for hiding secret messages within images. This algorithm can detoriate the secret message quality but still secret message is mostly recognized and is smoothed fine and noise reduced using Gaussian filter. Here the algorithm is implemented in software(using MATLAB) and in hardware(using FPGA and PSoC).

Keywords *Steganography, Cryptography, MATLAB, FPGA, PSoC, LSB Technique*

Investigation of FinFET with multi-channel structures on device characteristics

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Abstract: The primary objective of this article is to investigate the device-level architecture and functionality of fin field-effect transistors (FinFETs). Three distinct FinFET structures are analyzed, the standard or conventional FinFET, the Dual Metal Gate FinFET, and the Dual Fin FinFET. This research delves into the concept of dual or multi-fin configurations, which introduce additional channels to the device. By enhancing gate control, these configurations aim to significantly improve the electrical performance of FinFETs. Detailed analyses of each structure will provide insights into their respective benefits and potential applications in advancing semiconductor technology. The Dual FinFET turns out to be superior in performance as it has a high drive-on current of (ION) = 3.34 × 10-4 A and a lower off-state current of (IOFF) = 1.34 × 10-17 A. Also, the subthreshold slope (SS) is observed to be 48.43 mV/decade, compared to the other two structures such as conventional FinFET and Dual Metal Gate FinFET. The software used for simulation is SILVACO TCAD (Technology Computer Aided Design). (Times New Roman 10, Justified). This template provides instructions for preparing the book of abstract to be published in DevIC 2021.

Keywords*: Dual fin FinFET; Subthreshold slope; High k dielectric*

DC Analysis of T shape gate, L shape gate, Y shape gate, Field-plate gate AlGaN/GaN based HEMT

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Abstract: In this work, a T shape gate, L shape gate, Y shape gate and Field-plate gate is designed and its DC analysis is done respectively. The gate length of 100 nm is taken for all the designed AlGaN/GaN high electron mobility transistor(HEMT). From DC analysis an increase in drain current is seen for L shape and field plate gate HEMT. Also, T shape gate and L shape gate show a higher transconductance while T shape HEMT and Y shape gate HEMT have same transconductance. A low drain induced barrier lowering(DIBL) and Sub-threshold swing(SS) is observed for Y shape gate HEMT and T shape gate HEMT. An improved transconductance efficiency is seen for Y shape gate HEMT and T shape gate HEMT. Different design offers different advantage based on application like as an amplifier.

Keywords *High Electron Mobility Transistor (HEMT), AlGaN/GaN, T shape gate, L shape gate, Y shape gate, Field plate(FP) gate, Transconductance, Sub-threshold swing, DIBL*

Chaotic Image encryption scheme implemented in FPGA for security enhance

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Abstract: The internet has always faced significant security challenges when it comes to transferring information. Throughout and following the recent outbreak, it has become evident that as digital transactions surge, so do incidents of hacking and breaches. This highlights the growing need for secure transaction methods. In response, this paper introduces a novel cryptographic approach for image encryption and decryption, utilizing chaotic algorithms. To ensure the robustness of the encryption, we perform a series of rigorous performance evaluations, including Histogram, Entropy, NPCR, UACI Analyses. This study showcases the implementation of a one-dimensional reduce Henon chaotic map on an FPGA board, enhancing both the encryption and integrity of images.

Keywords*: chaos, encryption, FPGA, security*

A Novel ASK Reversible Gate and Its Implementation in Ripple Carry Adder Design

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Abstract:
Reversible logic is gaining increasing significance in diverse research areas, including quantum computing, nanotechnology, and optical computing. The exploration of reversible gates has emerged as a cutting-edge research area, driving a wave of innovative developments aimed at maximizing resource efficiency. Adders are essential in multipliers, especially in digital signal processing (DSP) applications. Reversible logic gates represent a major breakthrough in digital circuit design due to their ability to perform operations without loss. This work presents a novel 4x4 reversible gate and explores its potential in designing highly efficient digital circuits. The study examines the use of the suggested gate in implementing a full adder and a ripple carry adder. The improved efficiency and potential for scalable quantum computing of the new full adder and ripple carry adder designs are illustrated by their superior performance in terms of garbage outputs, ancilla inputs, and quantum cost when compared to the conventional architectures.

***Keywords**: Ancilla Inputs; Garbage outputs; Low power; Ripple Carry Adder(RCA); Quantum Cost.*

Securing the Future of Communication with Quantum Cryptography

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Abstract: The study of quantum cryptography has become a ray of hope in the constantly changing field of cybersecurity. Quantum cryptography uses the remarkable qualities of quantum mechanics to provide a level of security that classical cryptography finds difficult to achieve in light of the growing threats to digital information. This thorough analysis explores the many facets of quantum cryptography, including emerging quantum networks, practical applications, cryptographic protocols, and basic concepts. This review explains the intricacies of cost, infrastructure, and integration, and compares them with the continuous technological developments that indicate that it is ready for broad adoption. The impending threat of quantum computers, which calls for a switch to quantum-safe cryptography, looms large amid the promise of quantum security. Quantum-safe algorithms are important because they provide strong security against quantum attacks.

***Keywords**: Quantum computing, Quantum cryptography, QKD, Quantum safe cryptography, Quantum network*

Classifying the Tongue Contours for Assistive Devices

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Abstract: As artificial intelligence and machine learning become more prevalent, they are becoming an increasingly significant part of our daily lives. This improved human-machine interactions. Especially in the medical field, developing automatic detection systems to diagnose diseases and tumors. These systems classify affected areas, analyse symptoms, and develop assistive devices, among others. With these assistive devices, disabled people could continue living their regular lives much easier. This improved access to healthcare, as well as the quality of life of people with disabilities, is an invaluable benefit of AI and ML. In this paper, a hybrid approach is employed to classify ultrasonic tongue contours for the purpose of creating assistive devices. The dataset used in this paper is open-source medical imaging data. Noise reduction techniques like Spackle Reducing Anisotropic Diffusion (SRAD) and Non-local Means (NLM) are applied to enhance the quality of ultrasound videos and make them more suitable for further analysis. Performance metrics for classifying tongue contours are presented. An accuracy rate of 87.80 percent is obtained, and the precision, sensitivity, specificity, and F1 score of the test are calculated.
Keywords*: ultrasound images; Convolution neural network (CNN); assistive device; Spackle Reducing Anisotropic Diffusion (SRAD); Non-local Means (NLM); Peak Signal-to-Noise Ratio (PSNR); Contrast-to-Noise Ratio (CNR).*

PERFORMANCE OF HFO2 ON HIGH ELECTRON MOBILITY TRANSISTOR COMPATIBLE FOR MICROWAVE APPLICATIONS

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Abstract: Present work comprises of High Electron Mobility Transistor (HEMT) with Gallium Nitride (GaN) which is utilized for microwave applications. Proposed HEMT device is applicable for high-power applications due to presence of GaN because GaN has exceptional material properties such as wide band gap material. Present work has shown use of High-K technology, Hafnium Oxide (HfO2) as a passivation layer. After simulation analysis, obtained electrical parameters are such as drain current is 0.13 A/mm, maximum conduction band energy is 5.5eV, electric field is 4×106 V/mm, potential is 3.5v and conduction current density 2.87×107 A/cm2. Application of proposed HEMT device is satellite communication, microwave, RADAR. TCAD Silvaco Software has been used for simulation of proposed HEMT device.

Keywords*:* HEMT, HfO_2, High-k and Silvaco TCAD Software

Enhancing Biosensing Sensitivity through Simulation-Based Study of N+ Pocket Doped Vertical NC-TFET

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Abstract: In the present article, a more sensitive biosensor built on a Vertical Negative Capacitance TFET is designed and analyzed. The biosensor uses a gate stack with an N+ pocket of SiGe in the source area and a silicon-doped HfO2 ferroelectric layer. The device's performance is increased even more by including the SiGe N+ pocket in the source region, which makes the electron injection process more efficient. A decrease in the off-state surface potential is made possible by the gate stack, which comprises silicon-doped HfO2 ferroelectric with a thickness of 1 nm. This effectively prevents electron tunneling from the source region and a shallow off-state current, which further raises the biosensor's signal-to-noise ratio. The source region's integration with SiGe's N+ pocket improves the electron injection process, enabling effective and regulated carrier transport. This enhances the entire device's functionality and increases the biosensor's sensitivity to biomolecule detection.

Keywords*: Vertical Negative Capacitance TFET; Biosensor; Silicon-doped HfO2 ferroelectric; N+ pocket of SiGe, Sensitivity; Off-state current; Gate capacitance coupling; Biomolecule detection.*

Novel Sign-Magnitude Binary to Balanced-Ternary Encoder on Basys3 Artix7 FPGA

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Abstract: In the realm of digital systems, binary representation has been the predominant method for data encoding and processing. However, alternative numbering systems such as ternary (base-3) have gained considerable attention over binary due to its ability to reduce interconnect complexity for identical data processing. Balanced ternary offer several advantages over unbalanced ternary in certain applications. This report outlines novel binary to balanced ternary encoder that accepts 9-bit sign-magnitude binary data (-255 to +255) and generates 6-trit ternary equivalent in BET (Binary Encoded Ternary) format. The theoretical analysis is explained and the corresponding verilog code is simulated using Xilinx-vivado software to validate the idea. After behavioral simulation, the circuit is synthesized and implemented for the target device Xilinx Basys3 Artix-7 FPGA: XC7A35T-1CPG236C. Post implementation bit stream is downloaded on to the target FPGA for prototype verification.

Keywords*: Balanced Ternary, Basys3 Artix7 FPGA, Binary System, FPGA Design Flow, Verilog-HDL.*

Application of Machine Learning Approaches for Power Estimation of Digital VLSI Circuits at Register Transfer Level

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Abstract: This paper presents an approach to estimate power consumption in digital VLSI circuits at the Register Transfer Level (RTL) using machine learning techniques. With the scarcity of publicly available datasets in the VLSI domain, we automated the generation of a dataset using Python and TCL scripts. The dataset consists of 1100 samples of various digital designs, synthesized using Cadence Genus. We applied several machine learning models to predict power consumption, and the performance of the models was evaluated based on R-squared and Root Mean Square Error (RMSE). The results demonstrated the potential for machine learning models to estimate power accurately and efficiently in VLSI circuits.

Keywords*: power estimation, machine learning, Very Large Scale Integration (VLSI), Register Transfer Level (RTL)*

Improved Deepmaxoutmodel for Disease Prediction in Healthcare IoT Cloud System

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Abstract: The Internet of Medical Things IoMT has grown rapidly due to the growing popularity of wearable technology and its applications in health monitoring systems. The IoMT significantly reduces the death rate by facilitating early sickness identification. Predicting cardiac disease is among the most significant issues with clinical dataset analysis. Finding the key components of heart disease prediction is the goal of the suggested investigation, which makes use of machine learning techniques. Despite several studies on the issue, the accuracy of the findings on the diagnosis of heart illness is low. The purpose of this paper is to provide an innovative framework for healthcare monitoring that includes the following phases. Data preprocessing, feature extraction, acquisition of data, and prediction are the primary stages. The process of acquiring data is at the IoTs layer. The medical data is considered in this case (benchmark datasets of different illnesses). The data pre-processing operations of data cleaning and data filtering at the cloud layer are applied to the data obtained from the IoT sensors (considering the dataset), where the data normalization process will take place. Subsequently, statistical features and raw features are extracted. The multi-layered Deepmaxout model will predict the diseases during in the prediction phase. Lastly, the evaluation of the suggested approach is compared to existing methods using several types of metrics.

Keywords*: IoT; Health Monitoring; Feature Extraction; Prediction Model*

An IoT-based Hardware System for Road Accident Detection and Notification using CNN-LSTM Algorithm

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Abstract:

According to the WHO, approximately 1.3 million people die each year globally due to road accidents and the rate has increased by 17% in 2021 compared to 2020. There are certain causes behind the fatalities but, the most up-rising issue is not receiving medical emergency services in time. So, a solution regarding accident detection and notification is the most needed. This does not only help to save millions of lives rather can create a positive impact on society. We aim to develop an IoT-based hardware system that can be installed in a car as an auxiliary device to detect an accident and deliver notifications with the exact location, to the relatives and the nearest emergency centres. The device is composed of Raspberry Pi along with other sensors like an Accelerometer, Gyroscope, GPS, and a GSM module to collect the data. Then the data is analysed and a notification is sent if any accident occurs. To analyse and classify the data, the Convolution Neural Network and Long Short-Term Memory hybrid model is used. The model is trained with a time-series dataset collected via the device and it predicts the occurrence with 92% accuracy. The comparative performance is presented in terms of Accuracy, Precision, Recall, and F1-Score.

Keywords*: Internet of Things (IoT); Sensors; GPS; GSM; CNN; LSTM*

Design and FPGA Implementation of an Efficient Squarer Circuit Using Reversible Logic

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Abstract: This paper presents the design and FPGA implementation of an efficient 4x4 squarer circuit using reversible logic. The proposed architecture is developed using the hardware description language Verilog and synthesized with Xilinx Vivado and Xilinx ISE 14.7 tools. The FPGA implementation of proposed design has been done on Artix 7 (Nexys A7). The main improvements in this work include a significant reduction in garbage output, quantum cost, and total reversible logic implementation cost (TRLIC) compared to existing designs. Notably, the proposed architecture achieves quantum cost and TRLIC reductions of 84.34% and 82.10%, respectively. The circuit also demonstrates a remarkably low delay of 1.076 ns, making it suitable for high-speed applications.

Keywords*: Reversible logic, Squarer, Quantum Cost, Verilog, FPGA*

Unveiling Mental Stress: Examining the Impact on College Students' Well-being and Machine Learning Solutions

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Abstract: This study examines the growing mental stress problem, especially among young adults, emphasizing college students' stress levels before tests and online. It explores the effects of variables like test pressure and recruitment stress, frequently disregarded, and assesses stress throughout various life phases. It also aims to establish a correlation between stress and internet usage frequency to comprehend its impact on students' mental health. To identify mental diseases and their applications, the study uses a variety of machine learning (ML) techniques, such as Decision Tree (DT), Random Forest (RF), Logistic Regression (LR), Hist Gradient Boosting (HGB), and K-nearest neighbors (KNN). The paper explores the features of both supervised and unsupervised machine learning algorithms and provides an overview of each. The findings show that DT has the highest accuracy, with a 91\% accuracy rate, closely followed by RF and LR, with 90\% accuracy. KNN and HGB, on the other hand, show somewhat lower accuracy levels of 88\% and 89\%, respectively. This study clarifies the dynamics of mental health among college students and provides information on how to use ML techniques for mental health diagnosis and treatment.

Keywords*: Machine learning, mental illness, college students, mental stress, mental health diagnosis and treatment.*

Advancing Solar Cell Efficiency: Performance Insights into Low Lead $cspb_{0.625}Zn_{0.375}I_2Cl$ Perovskite Solar Cell

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Abstract: This study presents the application of reduced lead, all-inorganic mixed halide perovskite $CsPb_{0.625}Zn_{0.375}I_2Cl$ as a light absorber layer. The proposed solar cell used TiO_2 (Titanium dioxide) as electron transport material (ETL) and Spiro-MeOTAD as hole transport material (HTL). The SCAPS-1D simulator is adopted for this solar cell design. This study presents a performance analysis of a low-lead inorganic solar cell, focusing on the impact of bulk defect as well as the thickness of the $CsPb_{0.625}Zn_{0.375}I_2Cl$. The thickness / bulk defects of $CsPb_{0.625}Zn_{0.375}I_2Cl$ have been varied 100 nm - 1000 nm / 10^{10} cm^{-3} - 10^{19} cm^{-3} respectively. In addition, impact of illumination temperature has been analysed and reported. Findings revealed that increased bulk defects have reduced the PV performance, and the impact is more pronounced on thick absorber layer. An increase in $CsPb_{0.625}Zn_{0.375}I_2Cl$ thickness has raised the PCE, whereas temperature diminished the PV performance. With 23.26% of PCE, the device has delivered best performance, at 1000 nm / $10^{10}cm^{-3}$ of thickness and defect density.

Keywords*: Solar cell; all-inorganic; perovskite*

Doping Dependent Electron Transport Mobility in $Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As$ Double Quantum Well Field Effect Transistor Structure

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Abstract: The doping dependence electron transport mobility μ^t due to different elastic scatterings in $Al_{0.3}Ga_{0.7}As$ / $In_{0.15}Ga_{0.85}As$ double quantum well field effect transistor structure is reported. In the absence of an electric field i.e., $F = 0$, two subbands are occupied. As doping concentration (N_d) increases from 0.5 to 1.5×10^{18} cm^{-3}, μ^t enhances from 3.2 to 4.5×10^4 cm^2/Vs. As $|F|$ increases, μ^t enhances and shows the transition of subband states from two to one at $|F| = 5$ to 13.2 kV/cm for $N_d = 0.5$ to 1.5×10^{18} cm^{-3} respectively. Here, the variation of μ^t with F is decided by the symmetric nature of ionized impurity scattering. Still the asymmetric scattering potential of interface roughness reduces μ^t more for positive F.

***Keywords**: KDouble Quantum Well; Transport Mobility, Scattering matri;, Intersubband Interaction*

Modulation of *I-V* Characteristics in U-Shaped Armchair Graphene Nanoribbon-based Tunnel Diode

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Abstract: Here, the transport characteristics of a U-shaped armchair graphene nanoribbon tunnel diode (AGNR-TD) are modulated by adopting a tight-binding model and non-equilibrium Green's function (NEGF) formalism. Initially, we examine a pristine AGNR (pAGNR) which exhibits ballistic current-voltage (*I-V*) characteristics. To convert ballistics nature to tunnel diode characteristic we considered U-shaped AGNR-TD by introducing a cut of depth (d_c) at the upper edge of pAGNR. This pattern resulted in the formation of a single-barrier TD structure. As d_c increases from 7.38 Å to 22.14 Å, negative differential resistance (NDR) is obtained with a peak-to-valley ratio (PVR) of 2.57. In addition, we analyzed the *I-V* nature and transmission probability by varying the potential barrier width (W_b). As W_b increases from 18.46 Å to 35.5 Å, the corresponding peak current decreases. However, the PVR value rises from 2.57 to 3.18 and the power consumption at the valley drops from 171 nW to 17 nW.

***Keywords**: U-shaped armchair graphene nanoribbon tunnel diode (AGNR-TD), transport properties, non-equilibrium green's function.*

FPGA-based Implementation of Lightweight Block Ciphers

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Abstract: This research explores the design and FPGA-based implementation of several lightweight block cipher architectures, emphasizing their performance metrics. Two lightweight block ciphers, consisting of internal block lengths of 16 bits and 32 bits, were implemented on FPGA platforms using the Virtex-7 device family. Their performance was compared to existing lightweight block ciphers—including Present, Simon, Prince, Rectangle, and Hummingbird—in terms of area, power consumption, and delay. The results demonstrated that the modified Hummingbird cipher, with 16-bit and 32-bit block lengths, exhibited superior efficiency, occupying less space, and consuming less power than its counterparts. Consequently, the enhanced efficiency and reduced resource requirements of the modified Hummingbird cipher position it as an optimal lightweight block cipher for resource constrained environments. This marks a significant advancement in developing cryptographic solutions on FPGA platforms.

Keywords*: FPGA; Hummingbird; lightweight; cryptography*

NavIC Galileo long distance RTK positioning performance

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Abstract: This research thoroughly investigates the kinematic positioning performance of the Navigation with Indian Constellation (NavIC) under static conditions, using data collected from a long baseline in India. The study compares NavIC's Single Point Positioning (SPP), long-baseline kinematic positioning, and L5 signal availability with Galileo's E1 and E5 signals. A Double-Differenced (DD) methodology-based kinematic model is introduced, which demonstrates that NavIC achieves centimeter-level accuracy comparable to Galileo. Although individual performance of NavIC and Galileo is inferior when used separately, their combined use significantly enhances kinematic positioning performance, surpassing the capabilities of each system individually. This combined approach offers improved accuracy and reliability in positioning, benefiting users through enhanced performance in real-world applications.

Keywords*: NavIC; GPS; Double Difference; RTK; Long Distance;*

Temperature-based Routing Protocols for Wireless Body Area Networks (wbans) : A Comparative Analysis

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Abstract: Wireless Body Area Network (WBAN) has evolved and has found enormous applications, especially in the medical field for e-health monitoring. WBAN allows patient data to be collected remotely with the help of various tiny sensors that are present in or on the human body in the form of implanted devices like a pacemaker or wearable devices like skin patches, smart watch, etc. that collect data related to human vital parameters like blood pressure, sugar level, pulse, temperature, etc. The sensor nodes play an important role in routing and sometimes the node's temperature rises beyond the given threshold value, which can lead to adverse effects on the human body. This paper addresses various problems caused due to heat effects and provides an overview of the various types of routing available in WBAN with a focus on temperature-based routing. The various recent existing routing protocols based on thermal-effects have been reviewed over the past few years. The paper provides insight into the objective, problem statement, tool, and technique used in the existing papers. It also summarizes the various advantages, limitations, and future scope, which is useful in providing research direction to researchers who are interested in this particular area of routing. This paper provides an updated review of routing protocols based on temperature, with a focus on the recent protocols thus highlighting the need for research, challenges, and open research issues in this domain.

Keywords*: Temperature based routing, Wireless Body Area Network (WBAN), Routing Protocols, Healthcare.*

Performance Analysis of a Heterojunction Dual Gate Ferroelectric Tunnel FET with variation of Gate Stack Dielectric

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Abstract: In this study, a comparative analysis is performed based on SILVACO ATLAS TCAD for a Heterojunction Dual-Gate Ferroelectric Tunnel FET with different combinations of gate insulator oxide in buffer layer. To increase the device's ON current and minimize ambipolarity, a series combination of high-k and low-k oxide is utilized, together with a ferroelectric layer beneath the gate. The intervention of negative capacitance caused by the ferroelectric layer results internal voltage amplification and hence enables the device to operate at low supply voltage, thereby reducing device power consumption. The addition of ferroelectric and high-k and low-k oxide layers to the gate stack decreased the gate stack's total effective capacitance, which in turn led to a smaller subthreshold swing, which is a crucial parameter for faster device switching. Limiting the ferroelectric layer thickness below its critical thickness results in hysteresis free operation of the device thereby making it suitable for logic operations. When compared to baseline TFETs, ferroelectric TFETs are viable candidates for energy-efficient low power applications in modern CMOS industry.

Keywords*: Heterojunction; High-k and low-k dielectrics; Ferroelectric negative capacitance; subthreshold swing*

Impact of Hole Gas in O_2 sensing Applications in Ge Core Si Shell Nanowires: Quantum Simulation Study

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Abstract: In this study, we investigate the impact of hole gas on the performance of sensing applications using Germanium (Ge) core Silicon (Si) shell nanowires (NWs) through quantum simulation. The unique core-shell structure of Ge/Si NWs offers significant advantages in sensing due to its enhanced electronic properties and high surface-to-volume ratio. Our simulations focus on the behavior of hole gas in the Ge core and its influence on the sensing capabilities of the nanowire. Using advanced quantum mechanical modeling and simulation techniques, we analyze the charge transport characteristics, sensitivity under varying conditions. The incorporation of hole gas in the Ge core is found to significantly alter the electronic properties of the NW, leading to improved sensitivity and faster response times in sensing applications. The study provides detailed insights into the quantum mechanical interactions and charge transport mechanisms within the Ge/Si NW, highlighting the potential for these nanostructures in developing highly sensitive and efficient sensors. Our findings demonstrate that the manipulation of hole gas within the Ge core can be a key factor in enhancing the performance of gas-sensors, paving the way for the development of next-generation diagnostic tools. This work not only advances our understanding of Ge/Si core-shell nanowires but also opens new avenues for their application in the field of gas sensing.

Keywords*: Ge-Si core-shell, Hole Gas, O_2 sensor, Schrödinger solver*

Performance Analysis of Multiplexer based Ternary Multiplier Designed Using FinFET models

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Abstract: Multivalue logics, particularly ternary logic, offer enhanced energy efficiency and reduced circuit complexity, making them advantageous in digital system design. This article investigates the design and performance of a multiplexer-based ternary multiplier implemented using 18 nm FinFET technology. The study evaluates three distinct FinFET models: LVT, SVT, HVT. The performance of these models is assessed through power consumption, transient delay, and power-delay product (PDP). Simulation results reveal that the LVT, SVT, and HVT FinFET models exhibit power consumption values of 4.34 µW, 4.86 µW and 4.29 µW, transient delays of 20.42 ns, 20.48 and 20.45 ns, and PDP values of 88.62, 99.53 and 87.73 (X10^-15 J), respectively. This research contributes to the development of advanced VLSI systems, emphasizing the importance of selecting appropriate FinFET models to optimize the trade-offs between speed, power efficiency, and overall energy consumption in ternary logic circuits. Potential applications include memory systems, digital signal processing, quantum computing, and error detection and correction.

Keywords*: FinFET Technology, Ternary logic, Ternary Multiplexer, Ternary Multiplier*

Time – Dependent Eikonal Solution using Physics informed neural networks

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Abstract: Many scientific and technical fields employ the eikonal equation. Multiple numerical strategies have been devised throughout the years to solve the eikonal problem. Nevertheless, these techniques necessitate significant alterations to accommodate supplementary principles of physics, such as anisotropy, and may even fail to function properly for some intricate variations of the eikonal equation, necessitating the use of approximation methods. Massive 3D situations that require repeated calculations of velocity variations and initial positions face a processing challenge. This paper introduces a method to address the eikonal equation by utilizing PINNs, a relatively new strategy in the realm of physical science. By decreasing a loss function derived from the eikonal equation, the neural network is instructed to construct path durations that align with the underlying partial differential formula. This work employs an adaptive stimulation factor and flexible scaling of the loss factor variables to enhance velocity of convergence and reaction effectiveness. This additionally shows the technique's adaptability in incorporating moderate distortion and topography of surfaces without boundaries, in contrast to traditional approaches that necessitate substantial changes to the algorithm.
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Keywords*: PINNs, Machine learning, Eikonal Equation, PDEs Predictive modeling, Automatic differentiation*

Solution of Allen – Cahn equation using Physics – informed neural networks

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Abstract: Physics-informed neural network integrates the physical properties of a structure through the border cost constraint within the loss property of the neural network. The methodology has demonstrated significant efficacy in estimating the relationship among the outcome of a PDE and its spatio-temporal variables. A unique PINN technique is presented by successively solving the PDE across multiple consecutive sections with only one neural network. The primary concept is to undergo rebuilding the identical neural network to address the PDE across consecutive duration intervals, during adhering to the previously acquired solutions across all prior time segment. The benefits of PINN are demonstrated by the resolution of the Allen-Cahn formulas. These formulas are extensively employed to characterise distinction of phases and reaction-diffusion processes. Novel approaches have been suggested to enhance the suggested PINN scheme. The strategy employs a transfer learning methodology that retains the characteristics acquired from prior training. This research demonstrates that this method considerably enhances the reliability and efficacy of the PINN scheme.
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Keywords*: PINNs, Partial differential equation (PDEs), Allen Cahn equation, Deep learning, Computational physics*

Analysis of AlGaN/GaN-Based HEMT with 3-Step Gate Field Plate for High Power Applications.

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Abstract: The proposed research work investigated a 3-step gate field plated heterojunction FET or high electron mobility transistor (HEMT) based on AlGaN/GaN material system. The proposed structure supports high power and high speed applications. The proposed HEMT achieves a higher transconductance (g_m) of 1.46 S/mm and subthreshold slope of 117 mV/decade. The breakdown voltage of 2250V has been achieved for proposed field plate HEMT. As a result, for this HEMT configuration, which is designed for high-power applications, characteristics like transconductance (g_m), threshold voltage (V_t), breakdown voltage (V_{BR}) and subthreshold slope (S_{sub}) were carefully examined. The Silvaco TCAD Simulation tool has been utilized to carry out every simulation that is described in this research work.

Keywords: *high electron mobility transistor (HEMT), hetero-structure, field plate (FP), breakdown voltage, subthreshold slope (SS), transconductance (g_m).*

Study on Deep Learning based Classification Models for Multiple Sclerosis in MRI datasets

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Abstract: The deep learning-based approach for identifying Multiple Sclerosis in the human brain using MRI datasets has been proposed in this study. Sclerosis affects the functionalities of the spinal cord and central nervous system. The investigations on sclerosis-affected brain cells show improved accuracy though they do not provide accurate treatment and diagnosis planning. This study addresses the challenges encountered in the treatment planning of sclerosis-affected brain disorders by incorporating deep learning techniques. For MRI slice datasets, VGG16, CNN, ResNet50, Inception V3, and for MRI volume, 3D models of Inception V3 and ResNet50 are implemented and tested to identify and extract multiple sclerosis. Categorical loss functions and Adam optimizer are embedded to train the models, enabling to learn of discriminative features for accurate classification of sclerosis-affected cells. Experimental results, axial & sagittal accuracy, f1-score, confusion matrix, and qualitative outcomes, demonstrate promising performance in accurate prediction of multiple sclerosis for the early diagnosis and treatment planning. This study contributes to the effort to develop advanced computational tools for aiding the diagnosis of multiple sclerosis-affected patients.

Keywords: *Accuracy; Deep learning; Classification; Medical Imaging; Multiple Sclerosis; Machine Learning*

Fringing Effects in a Capacitive Micromachined Ultrasonic Transducer with a SiC actuation layer insulated by High dielectric material

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Abstract: Sealed capacitive micromachined ultrasonic transducer (CMUT) mostly consists of two parallel electrodes separated by a structural layer of silicon nitride (Si_3N_4) and a vacuum cavity. Biasing the transducer element generates electrostatic force of attraction where the lines in the field bulge at the boundaries of the layers contributing to fringing effects. These fringing capacitances result in overall increment of the device capacitance. To capture this effect a very simple model of Landau and Lifschitz is incorporated, where the analytical model outputs are well matched with commercially available PZFlex FEM simulated results. Because silicon carbide (SiC) has a higher Young modulus and lower residual stress than Si3N4, it is used as a structural material in the CMUT. The improvement in device capacitance is approximately 13.1% through adjustments in the thickness of gaps and insulation. However, factoring in the relative dielectric constant and the electrode radius, this improvement reduces to around 7.9%. Additionally, introducing a high-k insulating layer enables the upper electrode to be structured on the lower face of the SiC layer. This modification leads to an augmentation in the device's total capacitance. This article also examines HfO2 materials of varied thicknesses.

Keywords: *CMUT, micro-electro-mechanical system (MEMS), SiC, high-k, fringing effect*

Enhancing Public Health Measures with AI and MobilenetV2 for Face Mask Detection

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Abstract: All continents were experiencing a global health crisis brought on by the coronavirus (COVID-19). To properly protect against this infection, it is important to put preventive measures into place. The wearing of face masks in public places is a reliable form of protection. A big issue arises when attempting to detect the presence of masks among huge groups in public areas. The existing face mask detection systems are concisely described in this work. Based on the methodology used, the databases used, and the accuracy attained, we compared the state of the art of face mask detection techniques. This study brought to light the difficulties that still remain in creating a reliable face mask detection system. A two-step system was formed as a solution to this problem. A model was trained in the first stage using MobileNetV2, OpenCV, and Keras/TensorFlow. The training set included both masked and unmasked faces from real-world data as well as data from GitHub and Kaggle. This model achieved a 99.35% accuracy rate. Deep learning methods, especially when optimized, are effective in a wide range of scenarios, including complex and dynamic environments. Hybrid methods can be effective when a combination of techniques is beneficial, such as handling diverse mask types

Keywords*: Keyword1; keyword 2; keyword 3 (Times New Roman 10, Italics, Left Justified)*

Lateral Straggle Based Interface Trap Sensitivity in n-p-n SOI Double Gate TFET

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Abstract—This article reports the impact of interface traps and dopant lateral straggle on a tunnel field-effect transistor (TFET) based on an ***n*–*p*–*n*** silicon body with a double-gate structure. Both gates are on the same side, spanning over two p n junctions. In the proposed device, interface trap analysis is conducted considering a constant doping profile and an analytical doping profile having lateral straggle arising out of the ion implantation process. The article analyzes interface traps by considering variations in lateral straggle from 5 nm to 10 nm in the source and the drain regions. To realize localized interface traps, a framework involving segmented interface traps is adopted taking into account, lateral straggle in the source region. These analyses are systematically investigated through calibrated TCAD simulations with the objective of observing the impact of interface traps in both constant doping and analytical doping profiles.
Keywords: *interface traps; localized; lateral straggle; n-p-n TFET.*

Phase Correction using single Current feedback amplifier

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Abstract: This paper presents a novel realization scheme for a single-CFA (Current Feedback Amplifier) based simple first-order All-Pass Filter (APF) with a grounded capacitor. The proposed topology has been further developed to achieve a second-order design by incorporating a grounded shunt LC-resonator as the phase-selection component. This extension utilizes a single DVCCTA (Differential Voltage Current Conveyor Transconductance Amplifier) based L-simulator is employed to realize the LC-resonator. The impact of device imperfections, including port tracking errors and parasitic capacitors (Cy,z), on the phase responses has been analyzed, revealing a negligible effect. The design maintains a flat unity gain across the intended frequency range, although the usable frequency range is limited by Cy,z. Experimental verification up to 2.4MHz shows measured Total Harmonic Distortion (THD) of the output signal at 0.9% and 2.7% for the first-order and second-order APF, respectively.

Keywords*: Current Feedback Amplifier (CFA; CFA- parasitic–effects, DVCCTA,), Allpass filter, Phase-error*

Development of IoT based n-ZnO/p-rGO Nanohybrid H_2 Sensor Node

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Abstract: — An integrated hydrogen detection node was developed using the n-rGO and p-ZnO combining nanohybrid sensor. The hydrogen detecting performance of this integrated system displayed a decent linear relationship among the detecting signal and hydrogen concentrations in air, for a wide range of hydrogen concentrations from 100 ppm to 10,000 ppm (1% vol.). This ingratiated sensing node was IoT platform based and is connected in the near of the gas measurement setup and the response for set threshold H_2 gas in air of 100 ppm, 500 ppm, 1000 ppm, 5000 ppm and 10000 ppm was tested for 1 hours. Upon the detection of a discernible amount of hydrogen, the system will „wake„ from an idle state to create a wireless data communication link (using IoT) to relay the detection of hydrogen to a central monitoring station (i.e. laptop, desktop, tablet or smart phone). The hydrogen detecting node was created with two operating modes in mind. In the first mode, considerable amounts of hydrogen would be detected and a central monitoring person would be notified if hydrogen was found above a predetermined thresholdIn order to track the amount of hydrogen present, actual hydrogen concentrations as low as 100 ppm are sent to the receiver in the second mode of operation.

***Keywords**:* rGO-ZnO nanohybride; Hydrogen Sensor; IoT platform; Sensore Node

Study of thermal noise in InAsxSb1-x UTB MOS under sub-100 nm range

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Abstract: — We study the effect of device scaling for varied lengths of channel, thicknesses of channel, and thicknesses of insulating layer for varying both gate voltages and frequencies on the thermal noise performance of InAsxSb1-x n-channel ultra-thin body metal oxide semiconductor (UTB-MOS). To verify the existing model, the simulated transfer characteristic curve is compared with published experimental results. The minimum noise figure (NFmin), noise resistance (Rn) and power spectral density of the drain current (SID/ID2) were calculated using the transconductance (gm) and drain current (ID) simulation data. According to our findings, thermal noise in InAsxSb1-x n-channel MOSFETs is dependent on device parameters and can be reduced by appropriately downscaling the channel length, channel thickness, and insulator thickness. When the channel length was decremented from 0.1 µm to 0.04 µm at 1V of gate voltage a 0.75 kΩ decrement in noise resistance is achieved . The channel length decrement also yields a power spectral density of roughly 2.2×10^{-24} Hz^{-1} and a minimum noise figure of roughly 1.3 dB.Further improvements were observed with a reduction in channel thickness.

***Keywords**: Ultra thin body metal–oxide–semiconductor field-effect transistor; power spectral density; transconductance; channel length.*

Investigations on novel Dual Metal Gate-Vertical C-channel Nanosheet FET with f_T of 268 GHz for beyond 5G application

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Abstract: Vertical Channel Nanosheet FETs (Field Effect Transistors) are emerged as a potential solution for advancing semiconductor device performance in the era of continued scaling and improved device integration. This study compares the Drain Characteristics, analog, Radio Frequency (RF) performance between novel Dual Metal Gate (DMG) and Single metal gate (SMG) n-type Vertical C-channel Nanosheet FET (nVCNFET). DMG architecture enhances electron mobility and potential which leads to higher current ratio of 7.4 x 10^{14} and reduced Short Channel Effects. Analog performance of DMG-nVCNFET yields 23.9 % and 9.3 % improved intrinsic gain and Transconductance Generation Factor compared to SMG-nVCNFET as a result of improved transconductance and reduced output conductance. DMG-nVCNFET achieves 82 % higher cut-off frequency (f_T = 268 GHz) and ~ 4 times improved Gain Frequency Product (GFP = 140 THz) compared to SMG-nVCNFET, making it as a promising candidate for beyond 5G (B5G) applications.

Keywords*: Analog/RF; B5G; Dual metal gate; FET; Nanosheet; VCNFET*

Rapid detection of Biomolecules by Quarapul cavity extended source vertical Dielectric Modulated TFET (QESV-DM-TFET) Biosensor

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Abstract: In this This work presents the performance investigation of the quadruple cavity extended source vertical TFET(QESV-DM-TFET) device for the detection of target biomolecules by using the DM approach. The unique structural advantage of the device is that the inclusion of an extended source epitaxial layer enhances the ion current of the device by facilitating both line tunneling and point tunneling for the charge carriers in two directions. The quadruple cavity structure in the device increases the net area of interaction with the target biomolecules, and this can effectively tune the device's electric property to deliver highly sensitive results for detection. The N+ pocket in the extended source region of the QESV-DM-TFET biosensor increases the vertical tunneling further through the medium of the silicon epitaxial region. The device detects the presence of the different target biomolecules using their dielectric constant values, which include streptavidin (K=2.1), Uricase (K=1.57), Biotin (K=3.57) and gelatin(K=12). The simulated QESV-DM-TFET device shows superiority in terms of on(Ion)current sensitivity and switching current sensitivity, switching current sensitivity and the device reports a switching current sensitivity of 109, which is a remarkable improvement in TFET biosensors.

Keywords*: Band to Band Tunneling (BTBT), Biosensor, TFET, Quadruple, Extended Source, Epitaxial layer, Source Pocket.*

Performance Investigation of L-shaped Extended Source TFET based Photosensor for near-infrared Light Sensing Applications

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Abstract: In this manuscript L-shaped TFET is applied to the photosensing application for improved the optical sensitivity for the incident light focused in the optical gate in the near infrared region. The addressed photosensor gets the advantage of the line tunneling mechanism at the tunneling interface resulting in clearly distinguishing of light state current at different wave lengths. Additionally, N^+ pockets help in reduction of corner effects and improves the signal to noise ratio. Spectral sensitivity of 78 is observed owing to improved optical generation rate in the optical gate. Magnitude of SNR is reported as 6.29 x 10^2 db at wavelength of 700nm.

Keywords*: BTBT, Corner effects, photo detection, spectral sensitivity, Tunnel FET.*

Performance Analysis of Double-Gate Junctionless Tunnel FET with a Stepped Channel

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Abstract: In this article, we investigate a junctionless TFET with a stepped channel (SJL-TFET) to demonstrate its superior ON state current (ION), low subthreshold leakage current (IOFF), and high current switching ratio (CSR) compared to conventional uniform JL-TFETs. Metals with appropriate work functions (Φ) are strategically placed above specific regions to induce charge carriers in the source and channel areas. Spacers are inserted between the source and gate metals to separate the source and channel regions. The proposed SJL-TFET device features a stepped gate structure, which optimizes the tunneling area and enhances the tunneling of carriers during the ON state. This design improvement leads to better device performance by achieving a more efficient carrier tunneling process. Performance metrics obtained from 2D-TCAD simulations show that the proposed SJL TFET offers approximately a three-decade improvement in ON state current and about a one-decade reduction in subthreshold leakage current. The enhanced DC characteristics of the SJL TFET are primarily due to the improved tunneling efficiency facilitated by the stepped gate structure over the channel.

Keywords: *CSR, Junction less TFET, SS, Tunnel FET.*

Optimization of Doping Profile in Carbon Nanotube Field Effect Transistor

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Abstract: The impact of various doping profiles in the source, drain, and channel regions of a (19,0) carbon nanotube field-effect transistor is examined. The advantages of selective doping techniques are highlighted for their effectiveness in reducing scattering and improving current flow. Gate-All-Around CNT FETs significantly improve carrier mobility through the channel region, particularly those with selective doping strategies. The promising prospects of selective doping in Gate-All-Around CNT FETs are emphasized, providing a pathway to optimized device performance. Sub-threshold swing (SS), on/off current ratio (ION/OFF), and drain-induced barrier lowering (DIBL) are analyzed.

Keywords*: Carbon Nanotube Field effect transistor(CNTFET), Doping Profile, Non-Equilibrium Green's Functions, Neumann boundary condition, Gate all around.*

Supercapacitor-Based power delivery system to enhance the discharge duration for EVs

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Abstract: This paper presents a supercapacitor-based power delivery system designed to extend the discharge duration of electric vehicles. The proposed system utilizes a dynamic series-parallel switching configuration to optimize energy efficiency under varying load demands. Simulation results demonstrate enhanced power delivery and extended energy storage compared to existing systems, supporting the growing adoption of electric vehicles.

Keywords*: Electric vehicles, energy efficiency, energy optimization, energy storage, secondary power source, supercapacitor bank*

Double gate Tunnel FET with Core-Gate Engineering: An Effective Approach to Suppress Ambipolarity

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Abstract: In the present era, the size of MOSFET is scaled down to the nanometer range to achieve lower power consumption and higher switching speed. This continual down-scaling faces difficulties in terms of short channel effects, excessive standby power, and higher subthreshold slope (SS). Tunnel FETs (TFETs) can overcome this constraint by using quantum mechanical band-to-band (BTBT) tunneling of charge carriers in the channel. Because of its low SS, low OFF-state leakage, and high Ion/Ioff ratio, TFET is an excellent contender for replacing traditional MOSFET. However, low ON current (Ion) and ambipolarity are the two main concerns in TFET technology. TFET shows this typical ambipolar behavior, which is undesirable from a circuit design point of view. So, it should be suppressed. This paper considers a new core-gate engineering in a double-gate TFET to suppress the ambipolarity without degrading the ON current. The suggested device provides a higher Ion/Iamb switching ratio without compromising the average SS. Further, the effect of varying core gate metal width, dielectric thickness, and work function upon the ambipolarity has been investigated thoroughly.

Keywords*: TFET; core-gate engineering; ambipolarity; current ratio*

Simulation of Adaptive Wavelet Packets in Spatial Domain for Signal Demodulation in Optical Frequency Domain Reflectometry

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Abstract: Adaptive wavelet packets in spatial domain have been applied for signal demodulation in optical frequency domain reflectometry (OFDR). A simulation model has been built for OFDR and the advantage of using the proposed method over the conventional short time Fourier transform method is established through simulation results.

Keywords*: Distributed fiber optic sensing; optical frequency domain reflectometry; adaptive wavelet packets*

Study on Optical Properties of Multiple Quantum Well-based InGaN/GaN Light Emitting Diode

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Abstract: The electron-optical properties like I-V characteristics, luminous power, power spectral density (PSD), and full-width half maxima (FWHM) of an InGaN/GaN multiple quantum well-based LED are analyzed using the Silvaco TCAD tool. It is shown that the anode voltage vs. anode current shows a general PN junction characteristic with a threshold voltage 4.5 V and delivers a 150mA anode current at 6.5 V. The luminous power enhances linearly with anode current and it is supported by the electron concentrations in the wells of the MQW. The results on PSD reflected that it also increases with enhanced anode voltage and shows better performance as compared to that of conventional single QW-based LED. The discussed results will be helpful in improving the internal quantum efficiency of the conventional LED/LASER structures along with unipolar laser-like QCL. A high-efficiency MQWs LED with InGaN as a well and GaN barrier is designed and analyzed.

Keywords*: Light-emitting diodes, multi-quantum well, InGaN, power spectral density.*

Comparative Study of MEMS Microheaters using distinct designs and materials for PCR applications

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Abstract: The Polymerase Chain Reaction (PCR) based chips allow the amplification of specific DNA sequences and are increasingly being used in clinical diagnosis, gene detection, etc. A uniform temperature field is essential inside the PCR chip reaction chamber. Keeping in view this requirement, microheaters using three distinct materials—Nichrome (NiCr), Gold (Au), and Silver (Ag)—were designed and analysed through FEA simulations. The microheaters were modelled with three different geometries: double spiral, meander, and serpentine. Finite-element-based simulations were carried out using COMSOL Multiphysics software to predict the thermal performance of each microheater design. The simulations reveal variations in surface temperature distributions and heat efficiency as a function of geometry and material used. Temperature plots for each design and material were generated, providing valuable insights for the selection of materials to enhance performance for use in PCR chips.

Keywords*: MEMS; Microheater; Surface temperature; Design optimization; FEA simulation; PCR application; Heat efficiency*

Understanding and Enhancing Linearity in Fin-FET Biosensors for Biomolecule Detection

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Abstract: The downscaling of MOSFET has led to different short channel effects (SCEs) such as DIBL, Mobility Degradation and Impact Ionization etc. So different modifications have been carried out in the device structure to control the SCEs. Fin-FET is one of the prominent candidates among all the engineered devices. A FinFET based biosensor is designed to measure the presence of various biomolecules. The change in device characteristics such as drain current and transconductance is studied when the nanocavity of the biosensor is filled with different biomolecules like Protein, Apomyoglobin and Gelatin etc. with different permittivity. Various voltage intercept point and intermodulation distortion has been measured to know the linearity and analog performance of the device and the suitable operating Vgs for the device

Keywords*: Fin-FET, Biosensor, Transconductance, VIP3, IMD3*

Synthesis of Graphite-Based Conductive Paint for Flexible Paper Electrode for Voltammetric Detection of Lawsone in Cosmetic Product

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Abstract: In this study, a voltammetric technique was adopted for the determination of lawsone concentration using a conductive paint-based flexible paper electrode (CP-FPE). A low-cost conductive paint was formulated that composed of graphite, chloroform, and polyacrylate, serving as the sensing material, solvent, and binder, respectively. The cyclic voltammetry was employed for sensitive detection of lawsone, with a detection potential of -0.1 ± 0.008 V against an Ag/AgCl (sataturated KCl) reference electrode in a phosphate buffer solution (PBS) at pH 6.0. The electrode exhibited a linear detection range from 5 µM to 200 µM, with a detection limit of 0.045 ppm. This proposed electrode offers several advantages, including ease of preparation, miniaturization, disposability, and biodegradability. The successful application of the developed electrode for real sample detection using the standard addition technique, with an average recovery rate of 96.07%, is a strong indication of the method's practical effectiveness.

Keywords*: Graphitic material; Napththoquinone; Conductive paint; Flexible electrode; Electrochemical technique*

Design and study of the thermoelectric performance of mini cooler box using TEC

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Abstract: The need for cooling is increasing worldwide and to reduce global warming vapour compressor pump usage should be replaced. The advent of thermoelectric cooling showed an opportunity for alternate small level cooling that is portable, has no mechanical parts, and is easily current controlled. But the efficiency level found so far is not a match for the conventional present day existing technology using vapour compressor refrigeration. This paper attempts to build a mini cooler box of volume 3.5 litres using one TEC1- 12706, 2 heat sinks with DC fans on both hot and cold sides, and a circulating water with a DC pump, and analyse its various parameters found during the experiment. The COP found is 0.7. Also, some conclusions for even results have been suggested. (Times New Roman 10, Justified). This template provides instructions for preparing the book of abstract to be published in DevIC 2021.

Keywords*: TEC, thermoelectric cooling, COP, cooler box, TE module, temperature, heat transfer (Times New Roman 10, Italics, Left Justified)*

Optimizing Triple Material Staggered Heterojunction Double Gate MOSFET (TM-SH-DGMOS) Through Advanced Gate Engineering

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Abstract: This research paper emphasises on the simulation and analysis of Triple Material Staggered Heterojunction Double Gate MOSFET (TM-SH-DG MOSFET), with a focus on their possible uses in Radio Frequency (RF) and mixed-signal Systems-On-a-Chip (SoC). Using a numerical TCAD device simulator, the study examines the device's performance characteristics, particularly in Analog/RF and linearity contexts. The research investigates how variations in gate length ratios and gate materials influence key performance metrics, underscoring the potential benefits of these transistors for specific electronic applications. The research assesses multiple performance parameters for RF/Analog and linearity performance, including Transconductance (g_m), Transconductance Generation Factor (TGF), Cut-off Frequency (Ft), Gain Bandwidth Product (GBW), and Second Order Variable Intercept Point (VIP_2), because of their better short channel effect (SCE) performance and manufacturability. The findings reveal that TM-SH-DGMOS devices exhibit promising characteristics, particularly in RF performance, when considering gate ratio variations, suggesting their competitiveness in low-power applications.

Keywords: Transconductance, Cut-off frequency, Transconductance Generation Factor, Gain Bandwidth Product, Variable Intercept point

Quasi Vertical FinFET with Step Graded Doping for Obtaining 0.037 mΩ.cm^2 ON Resistance

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Abstract: Vertical Gallium Nitride FinFET have demonstrated a great potential for better power switching based applications. This paper reports a quasi-structure with a graded doping profile in the drift region. The drift layer is split into five sub-regions and doping is done in linear and step graded manner. The devices are then compared with conventional uniformly doped device and the proposed design shows that step graded doping can reduce the ON resistance without much degradation in breakdown. The step graded drift layer doping exhibits an improved-ON current of 1.5 kA/cm^2 with a specific ON resistance of 0.037 mΩ.cm^2 and a breakdown voltage of 52 V. The proposed device shows an improved performance over conventional uniform doping in terms of ON resistance reduction.

Keywords*: FinFET, gallium nitride, graded doping, power devices, quasi-vertical, silicon carbide*

Performance Investigation on Gate Stack Dual Material Double Gate MOSFET based Biosensor

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Abstract: This work investigates the label-free detection capabilities of a Gate stack Dual Material Double-Gate MOSFET based biosensor. The biosensor design features a nanocavity specifically engineered for biomolecule adsorption. To assess its sensitivity, we employed TCAD simulations to analyze the device's response to various biomolecules with differing dielectric constants. The results demonstrate a high on-current ratio (Ion/Ioff) indicative of good switching characteristics signifying efficient gate control. Furthermore, the simulations reveal significant current changes upon biomolecule adsorption within the nanocavity, highlighting the biosensor's sensitivity to the target biomolecules. This study paves the way for further exploration junction less DG-DM MOSFET biosensors as a promising tool for label-free bio-detection.

Keywords: DM-DG MOSFET, Biosensor, Sensitivity, On-current ratio (Ion/Ioff), Higher order transconductance (Gm2, Gm3), VIP2 , VIP3 , P1dB

Enhanced Sensitivity in InAs Based Gate Stack TFET Biosensors: An In-Depth Investigation

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Abstract: This work provides a thorough analysis into the sensitivity of InAs based Gate Stack TFET (GS-TFET) biosensors. Gate stack TFET have emerged as promising candidates for biosensing applications due to their unique structural advantages and enhanced sensitivity. We develop into the operational principles of these devices, emphasizing their potential for high-performance biosensing. Through detailed simulations and experimental validations, we analyze the sensitivity parameters under various biochemical interactions. Our study explores the impact of different doping concentrations, gate dielectric materials, and operating voltages on the device performance. The results demonstrate that InAs based GS TFET biosensors exhibit superior sensitivity compared to conventional biosensors, making them highly suitable for detecting low concentrations of biomolecules. This investigation provides critical insights for optimizing Gate Stack TFET biosensors for practical applications in medical diagnostics and environmental monitoring.

Keywords: GSTFET, Biosensor, Sensitivity, Threshold Voltage,

Design And Comparison of 4x4 Bit Multipliers Utilizing CMOS 45nm And FinFET Technology

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Abstract: This paper presents a performance analysis of two 4x4 binary multipliers implemented using different architectures: an array multiplier based on carry-save adders and a ripple carry multiplier using ripple carry adders. The multipliers were simulated using Cadence in 45nm CMOS and 18nm FinFET technologies. Key metrics such as power dissipation and delay time were evaluated for each multiplier. The power dissipation of the 4x4 array multiplier is higher than that of the ripple carry multiplier by 1.3 times in CMOS 45nm, and 1.52 times in FinFET..

***Keywords**: Digital multipliers, 45nm CMOS, 18nm FinFET, ripple carry multiplier, array multiplier*

Linearity Characteristics of Gate-Stack DG-MOSFETs: A Study with Diverse Biomolecule Configurations

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Abstract: In this study, we investigate the performance of gate-stack double-gate metal-oxide-semiconductor field-effect transistors (DG-MOSFETs) in the context of their application as biosensor devices. The analysis focuses on the impact of various biomolecules, including aptes, biotin, protein, and streptavidin, on the suggested biosensor system's linearity and overall effectivenessThe study systematically evaluates the influence of these biomolecules on the analog and linearity and sensitivity parameters such as gm_2, gm3, VIP_2, VIP_3 and Id sensitivity of the Gate stack DG-MOSFET, comparing the results to establish a comprehensive performance profile. Our findings reveal that the Gate stack DG-MOSFET exhibits superior linearity compared to its symmetric counterpart. The unequal DG-MOSFET is more linear than the balanced one and the linearity of DG-MOSFET can be enhanced by a changing channel thickness, doping concentration and different gate material. The study focus on the analog and linearity parameters of the purposed biosensor.

Keywords**: **DG-MOSFET, Gate Stack, Biosensor, Linearity Analysis, Biomolecules.

Analog/RF performance and reliability investigation of nanowire junctionless MOSFETwith interface traps

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Abstract: The present piece of work emphasizes upon the analog/RF and linearity performances of nano wire junctionlss MOSFET in the presence of interfacial trapcharges. This investigation is useful in addressing thereliability issues and needed for the design of RFICs. The analog/RF and linearity performances are evaluated through figure of merits like Transconductance (Gm), cutoff / unity gain frequency (*Ft*) and third order transconductance (Gm3). ATLAS TCAD simulator is used for device simulation. The results of simulation reveal better immunity against positive trap charges as compared to negative trap charges. The device performance degrades with negative trap charge density.

***Keywords**: Jucnctionless MOSFET, Transconductance,Transconductance generation factor (TGF), unity gain Cut-off frequency(Ft), third order transconductance (Gm3)*

Polarization Engineering of the EBL to Produce Efficient AlGaN UV-C LED

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Abstract: A major challenge for III-Nitride ($Al_xGa_{1-x}N$) based ultraviolet (UV-C) light emitting diode (LED) is achieving efficient hole supply from the p-region. Herein, we try to counter the issue by employing a stair-like grading strategy in the electron blocking layer. This method enhances the hole supply by modulating the polarization charge density. Additionally, it reduces resistive losses with varying the polarization charge density. The variation in polarization charge density with a stair like grading approach leads to ~22% and ~34% improvements in the hole and electron concentrations, respectively in the target LED structure. These improvements enhance the radiative recombination (RR) rate in the active region by 1.43-times in the final LED sample. This (the reduced resistive losses, higher hole and electron concentrations, and increased RR rate) lead to a considerable improvement in the maximum internal quantum efficiency, improving it by approximately 170% in the target LED structure.

Keywords: *AlGaN, EBL, IQE, UV-C, Resistive Losses.*

High Temperature Performance Analysis of AlGaN/GaN HEMT

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Abstract: Electronic devices made with wide band gap materials are useful for High-temperature applications. GaN and its alloys have proven to be the best choice for high-power microwave applications due to their superior material properties. The excellent thermal conductivity of GaN-based High Electron Mobility Transistors (HEMTs) has attracted researchers to investigate its suitability in high-temperature applications. In this paper, we have analyzed the AlGaN/GaN HEMT device performance at different temperatures up to 200˚C through simulation using the TCAD tool Silvaco Atlas. The variation in device performance (DC and AC) was studied by considering the modification in device parameters and by applying proper device physics. This study will be helpful to the researchers in predicting the HEMT device reliability in high-temperature RF applications.

Keywords: *high-temperature; AlGaN/GaN; bandgap; power gain; current gain*

High-endurance contention-aware power optimized hybrid memory using clock gating memory

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Abstract: In the process of increasing the processor's performance heat has made it more difficult to increase frequency and thereby performance. As a solution, computer architecture has moved away from single-core chips and towards multi-core chips, sometimes called Chip Multiprocessors (CMPs). The last level cache (LLC) in a coordinated multiprocessor (CMP) design is usually SRAM and is shared by numerous processors. There is an effort to optimize power consumption in the addressing system of the low-power SRAM delay buffer circuit shown in the design proposal. An array of novel power-saving strategies are included into the suggested SRAM addressing system. As the delay buffer operates in a sequential manner, it employs a ring-counter for addressing. A C-element gated-clock approach is proposed, and the operating frequency is reduced by half through the use of double-edge-triggered (DET) flip-flops in the ring counter. Additionally, to control the clock distribution throughout the network, a new gated-clock-driver tree is used in the design. To further reduce loading and power consumption, the memory block's input and output ports also use the gated-driver-tree approach. The proposed model uses optimistic address generation and a combination of SRAM and eDRAM for read/write operations of cache memory, ultimately reducing the dynamic power consumption by 20.43% and latency by around 23.45%.

Keywords*: chip multiprocessors; static random-access; memory; double-edge-triggered; CLOCK GATING; last-level cache; Hybrid memory;*

Improvement in Toxic CO Detection Capabilities via Incorporating Pt Dopant into ZnO Nanotube based Gas Sensor Devices: An Atomistic Modeling

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Abstract: This research work analyses the improved sensing performance of platinum (Pt)-doped zinc oxide (ZnO) nanotube (NT) based sensor devices, over pristine ZnO NT, towards the detection of toxic carbon monoxide (CO). The study leverages first principle based computational approach using the Gaussian 09W and Gauss View 6.0 packages, examining them individually in two systems, where CO was being considered as the adsorbed gas for both pristine ZnO NT, and Pt-doped ZnO NT, leading to the formation of CO-adsorbed pristine ZnO NT (Type-1 system), and CO-adsorbed Pt-doped ZnO NT (Type-2 system). The interaction between them was meticulously explored through the calculation of various electronic characteristics like HOMO (the highest occupied molecular orbital), LUMO (the lowest unoccupied molecular orbital), molecular electrostatic potential (MEP), density of states (DOS), and Mulliken charge analysis. The system's semi-metallic character was verified by the computed DOS. Notably, the study found that the material's reactivity of ZnO was much increased by doping it with platinum, which produced a substantial adsorption energy (-0.73829 eV). The results indicated that the catalytic activity of the Pt atoms was responsible for the increased sensitivity towards the CO molecule identification.

Keywords*: CO adsorption; ZnO nanotube; Pt doping; Mulliken charge; DOS*

A Comprehensive Sensitivity Analysis of Adenine Nucleobase on Pristine and Platinum-Decorated ZnO Nanosheets: An Interaction Dynamics.

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Abstract: The current study compares the ability of pristine ZnO nanosheets and platinum (Pt) decorated ZnO nanosheets to sense Adenine (A) nucleobase using a first-principle computational method with Gaussian 09W and Gauss View 6.0 software. This created two systems viz. Adenine adsorbed pristine ZnO nanosheet system (system-I) and Adenine adsorbed Pt-decorated ZnO nanosheet system (system-II). The adsorption and interaction between the considered molecule and the sensing material were analyzed using various electronic characteristics such as molecular electrostatic potential (MEP), density of states (DOS), Mulliken charge analysis, HOMO, and LUMO. It was observed that the pristine ZnO nanosheet exhibited better reactivity, resulting in a strong adsorption energy (-1.784 eV) compared to the Pt-doped ZnO nanosheet with an adsorption energy of (-1.253 eV). However, the Pt-decorated ZnO nanosheet demonstrated moderate binding distance (2.0236 Å) over the pristine ZnO nanosheet (3.0301 Å).

Keywords*: Mulliken charge; Density of state (DOS); Molecular electrostatic potential (MEP)*

Customized Design and Optimization of New Materials in Silvaco TCAD Tool by Understanding Inherent Material Defining Processes and Useful Simulation Methods: An Extensive Study

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Abstract: Accurate semiconductor device modelling in technology computer-aided design (TCAD) relies on precise material and method definition. Traditional software-defined materials often fall short in representing modern materials and specific design requirements and the same goes for method definition. This study comprehensively explores material and method defining procedures in Silvaco TCAD, emphasizing critical variables for electron device simulations. It introduces material-level and region-level definition approaches, highlighting the importance of material customization and solving method settings. Detailed descriptions of material properties, including carrier lifetimes and dielectric constants, enhance understanding as well as setting the right method for solving and obtaining the desired characteristics. The motivation for this research arises from challenges encountered with software-defined materials, where simulated values often deviate from theoretical ones, and there is a lack of output data in standard methods. This paper aims to elucidate the nuanced parameters involved in material and method definition, anticipating the growing need for personalized materials in semiconductor device simulations and making the right choice for methods. The study provides a solid foundation for TCAD research and development, addressing current issues and paving the way for future innovations.

Keywords*: Material Definition, Semiconductor Device Modeling, Silvaco TCAD.*

Studies on navigational satellite visibility and signal strength of different GNSS sensor

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Abstract: This paper investigates the performance of multi-GNSS systems using Android smartphones. By comparing signal strength (SNR) and satellite availability across different devices and constellations (GPS, GLONASS, Galileo, BeiDou, and QZSS), the study highlights the capability of smartphones in capturing high-quality GNSS signals. Results show that modern smartphones, particularly those with single/dual-frequency GNSS chipsets, track nearly 50 satellites simultaneously, with BeiDou and GPS generally offering the strongest signals. Additionally, smartphone GNSS sensors demonstrated signal strength values closely matching those of high-grade receivers, underscoring their growing reliability for precise positioning in various applications.

Keywords*: GNSS; Satellite visibility; Navigation sensor; Android Smartphone; Signal to Noise*

A transient enhanced capacitor less 380mA LDO with 1.2µA quiescent current

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Abstract: This paper presents a 380 mA low-dropout (LDO) regulator that achieves an ultra-low quiescent current (IQ) of just 1.2 µA while utilizing only a 0.5 nF compensation capacitor. The LDO employs dynamic biasing to achieve a high unity gain frequency (UGF) of 10.6 MHz, ensuring robust load transient response within 10% of the output load voltage under varying load conditions. Unlike many existing designs, this LDO operates without a buffer, significantly reducing power consumption. The core of the design is a rail-to-rail operational amplifier serving as the error amplifier, consisting of two complementary differential amplifiers and a charging-discharging amplifier. This structure provides a high swing to the power MOSFET, ensuring stable output across varying load currents. Additionally, an innovative overshoot and undershoot correction circuit is introduced, enabling swift control of the transient performance with the same low IQ. The LDO is implemented using a 180 nm CMOS process, offering an efficient and compact solution for power management.

Keywords*: LDO regulator, rail to rail amplifier, adaptive dynamic biasing, low-IQ, power management integrated circuit (PMIC).*

A Low Leakage Variations, High Stability 9T SRAM Cells

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Abstract—This paper introduces an alternative NLP-9T/PLP 9T SRAM cell design that demonstrates improved stability and low leakage power variations at worst-case analysis. The suggested SRAM cells mitigate read disturbances by deactivating the access transistors within the memory cell. Moreover, the inclusion of extra PMOS read access transistors along the bit-lines helps to ensure a successful read operation with high read stability. The results indicate that the suggested PLP-9T memory cell exhibits read stability that is 1.31 times greater than 6T-SRAM, 1.05 times higher than CONV-8T, 1.27 times higher than WU-Z8T, 1.25 times higher than LIU-D0T, and 1.022 times higher than the proposed NLP-9T memory cells. Furthermore, the proposed cells in standby mode effectively limit leakage power, even under the most adverse process fluctuations. However, the suggested NLP-9T/PLP-9T design takes about 1.7 times/1.3 times more layout area than the traditional 6T-SRAM.

Keywords — *Failure probability, leakage Power, monte-carlo analysis, PVT analysis, read access transistors, robust SRAM.*

Design and Investigation of Ge Source Hetero-Dielectric L-shaped TFET for Low Power Applications

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Abstract: This study explores a novel transistor design that combines a Germanium source with an L-shaped tunnel field-effect transistor (LTFET)structure, incorporatingaHetero-Gate-Dielectric(Ge-HD-LTFET). Simulations indicate that the Ge-HD-LTFET with a Si-Ge pocket region exhibits superior performance compared to the design without the pocket. This improvement is characterized by higher I_{ON}, lowerI_{OFF}, and a significantly reduced SS.The researchers analyzed various aspects of the transistor, including current-voltage characteristics, the distribution of band-to-band tunneling (BTBT) generation rate, electric field density, and the variation of material composition (mole fraction) within the pocket region. The findings reveal that the Ge-HD-LTFET with the Si-Ge pocket achieves a higher ON current due to an increased cross-sectional area at the BTBT junction. Additionally, the implementation of the hetero-gate-dielectric effectively suppresses ambipolar current. Finally, the study investigates how changes in key device parameters influence the transistor's functionality, providing valuable insights for optimization.

Keywords: *Hetero-Gate-Dielectric, Heterojunction,ON-current (I_{ON}), OFF-current (I_{OFF}),Subthreshold swing (SS).*

Analysis of Interface Trap Position Variation in Tunnel FETs

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Abstract: This article reports insights into variation of interface trap position in p-i-n SOI TFET. The impact is measured through statistical variability of the electrical parameters, ON current, OFF current, maximum band-to-band tunneling rate, maximum electron velocity, and threshold voltage. The entire oxide-semiconductor interface is divided into two halves: the high band-to-band tunneling (BTBT) region, and the region outside high BTBT region.

Keywords*: interface traps, TCAD, standard deviation, TFET, variability, band-to-band tunneling*

Attention-COVIDNet: An Enhanced COVID-19 Classification Framework using Attention

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Abstract: The COVID-19 pandemic has socio-economically affected world health and economies, thus increasing the urgency for diagnostic procedures that are characterized by efficiency, accuracy, and cost-effectiveness. In attendance to this difficulty, we present Attention-COVIDNet as a very special deep learning framework for the automatic classification of COVID-19 from chest X-ray pictures. Some of the advanced image preprocessing techniques used by the proposed model are histogram equalization and region of interest extraction. The classification will be done with the help of an attention-based Convolutional Neural Network, which will be changing the importance given to different portions of the X-ray images dynamically. This improves distinguishment in the model for COVID-19, pneumonia, and healthy instances. Attention-COVIDNet was trained on a comprehensive dataset of chest X-ray images and reached 98.2% accuracy with an F1-score of 98.5%, hence outperforming state-of-the-art models in accuracy. Attention-COVIDNet has the potential to turn into a dependable tool to assist health care providers for the early and accurate diagnosis of COVID-19, which eventually will lead to better outcomes for patients and also in the form of better treatment of the pandemic. The findings from this study enhance the promise of Attention-COVIDNet.

Keywords— COVID-19; Attention Mechanism; Classification; Performance Metrics

Effective Webshell Detection in IoT Networks employing TF-IDF, Word2Vec and SVM

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Abstract: The Internet of Things is the giant interconnection of sensor devices that allows data sharing, intelligent identification of networked "things," and administration of these "things." With increasing pervasiveness, the gadgets in the Internet of Things are playing a very important part in improving the lives of an individual. On the other hand, wide diffusion of Internet of Things devices makes them much more vulnerable to different types of attacks emanating from the Internet, which may result in privacy breaches, data manipulation, or disastrous damage to human beings and society. The stated importance of network security for IoT systems is because one of the main threats is caused by web injection, mainly through web shells. In this paper, we use popular machine learning models for webshell detection and to build secure solutions in IoT networks. This will enable us to develop a more secure Internet of Things system. After the extraction of character-level features using both Term Frequency-Inverse Document Frequency and Word2Vec approaches, classification is done using a support vector machine. It is illustrated through simulation results that the proposed method outperforms those that are regarded as state-of-the-art.
Keywords— Web shell Attack, Machine learning, Support Vector Machine, Internet of Things, Feature Extraction

Assessment of FinFET Performance and Its Biosensing Applications:A Review.

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Abstract: In recent days, the need for nanoscale devices has increased. In this case, FinFETs have proven themselves to overcome the short channel effects caused by the traditional MOSFETs. This paper presents the review of some parametric variations in FinFETs. The TCAD simulation results were used to analyze the performance of the device. The electrical parameters of the devices have been extracted for different fin dimensions and oxide thickness.The Ion/Ioff ,Subthreshold Swing and Drain Induced Barrier Lowering are some of the parameters discussed in this review paper. The short channel effects can be minimized by replacing SiO2 with high k dielectric materials like Si3N4, Al2O3, ZrO2 and HfO2.The effects of various high k dielectric materials are also compared and reviewed. In this paper some FET based biosensing applications are also discussed.This comparative analysis will be very helpful in the development of more complex and efficient FinFET designs.

Keywords: *FinFET; TCAD; SUBTHRESHOLD SWING; DRAIN INDUCED BARRIER LOWERING; HIGH-k DIELECTRIC.*

Enhancing Safety in Automotive Systems: A Comprehensive Analysis of 77 GHz Radar Performance for Pedestrian and Vehicle Detection

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Abstract—Automotive radar technology has seen significant advancements in recent years, becoming a pivotal component in enhancing vehicle safety and preventing collisions. This study explores the efficacy of radar systems in detecting both vehicles and pedestrians, focusing on the impact of Radar Cross Section (RCS) on detection accuracy. By examining radars operating at frequencies of 24 GHz and 77 GHz, the research highlights the challenges and solutions in distinguishing between high-RCS targets like vehicles and low-RCS targets such as pedestrians.

The study demonstrates that while 77 GHz radar systems excel in long-range detection of vehicles with high RCS values, their effectiveness in detecting pedestrians is limited by the lower RCS values of these targets. To address this challenge, the research introduces enhancements in radar system configurations, including an expanded azimuth field of view and optimized resolution settings. These modifications significantly improve the detection of pedestrians and other objects that are offset from the radar's primary line of sight.

The results emphasize the need for continuous innovation in radar technology to balance long-range vehicle detection with the accurate identification of low-RCS targets. By integrating advanced radar features and refining detection algorithms, the study contributes valuable insights into developing more robust automotive safety systems. This research not only advances the understanding of radar-based collision avoidance but also lays the groundwork for future enhancements in autonomous driving technologies, ultimately aiming to create safer road environments for all users.

Key words—Automotive Radar, Pedestrian Detection, Radar Cross Section (RCS), Long Range Detection, Adaptive Cruise Control, Radar Azimuth Field of View

Fabrication, Characterization and SPICE Calibration of Dropcasted Egg Albumin Memristors

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Abstract: This article presents the fabrication and characterization of an egg albumin memristor with aluminum electrodes. Experimental I-V curve fitting is performed using a memristor model. The memristor's active region is created using the drop-cast technique, resulting in a pinched hysteresis loop that confirms its memristive characteristics. The experimental results reveal a $\boldsymbol{Ron/Roff}$ ratio of $\mathbf{0.56}$, along with the maximum and minimum current values in the order of 1 mA and 10 μA.

Keywords*: bio-memristor, pinched hysteresis, egg albumin, spice model*

Performance Evaluation of Double Gate Junctionless Accumulation Mode Stacked Gate Mosfet

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Abstract: To continue the process of miniaturization and simultaneously to overcome the issues related to short channel effects, double gate junctionless accumulation mode stacked gate (DG-JLAMSG) MOSFET is proposed in the present piece of work. The DC, analog and RF performances are investigated with varying thickness of high-k gate stacking oxide. This structure has numerous advantage in improving the transconductance generation factor, cut-off frequency, linearity .Hence a detail investigation is needed to analyze the device behavior with respect to varying structural parameters. Presently, the performances of DG-JLAMSG are studied by changing the stack oxide thickness (TOXH). A remarkable improvement in performance is observed and the device can be a better contender for the designing of system on chip applications and RFICs.

***Keywords:** Transconductance, Cut-off frequency, Transconductance Generation Factor, Gain Bandwidth Product, Variable Intercept point*

Analog and High Frequency Analysis of Dielectric Pocket Engineered (DPE) 4H-SiC Based Dual Metal (DM), Gate-Stack (GS), Surrounding Gate, FET(DPE-4H-SiC-GSDM-SGFET) for GIDL Reduction

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Abstract: Gate induced drain leakages (GIDL) is a kind of short channel effects (SCEs) that can cause device damage due to persistent gate leakage of current. It acutely impairs the device's output, predominantly in analog utilizations. To reduce this effect, an innovative construction is projected with two dielectric-pockets close to the source region & drain region. This study examines a Dielectric Pocket Engineered, 4H-SiC Based Gate-Stack, Dual-Metal, Surrounding-Gate, FET (DPE-4H-SiC-GSDM-SGFET) for surface potential, electric field (contour), and subthreshold slope on several channel lengths (L =50 nm,40 nm and 30 nm). A Gate-Stack with high-k based dielectric material, which includes Lanthanum oxide (La2O3) and Aluminum oxide (Al2O3), have been employed. The objective is to reduce Gate-Induced Drain Leakage (GIDL) in off-state condition. Critical parameters such as drain current (Ids), transconductance (gm), output conductance (gd), input capacitance (CGG) and cutoff frequency (fT) have been investigated. ATLAS 3-D simulator has been used for the simulation purpose.

***Keywords**: Gate dielectric, GIDL, Gate-Stack, 4H-SiC, Dielectric Pockets.*

Junction-less Nanowire TFET with hfo2 /sio2 stacked gate-oxide for highly sensitive biosensor

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Abstract: This paper discusses a novel junction-less nanowire tunnel field effect transistor (JL-NWTFET) with stacked HfO_2/SiO_2 oxide to design a very sensitive biosensor. With an increasing gate voltage, the high-k dielectric layer enables efficient band-to-band tunneling (BTBT) to occur, resulting to a reduced subthreshold swing (SS) and a higher on-current. A gate-all-around (GAA) structure and a dielectric modulation (DM) method are used by the JL-NWTFET to find biological compounds with DC values between K = 1 to K = 8. The device is analyzed by measuring changes in subthreshold swing (SS), transconductance (g_m), drain current (I_D), and on-current (I_{ON}). The proposed JL NWTFET biosensor is compared to conventional devices. We made the new stacked oxide JL NWTFET using high-k dielectric material (HfO_2), which shows better performance characteristics. The simulation results specify that that the proposed heterodielectric gate oxide stack-based JL NWTFET is stronger and more reliable than regular JL NWTFETs.

Keywords*: Stacked structure, hetero-Dielectric, sensitivity, biomolecules, Tunnel FET*

Effects of gate metal engineering on electrical characteristics of SOI MOSFET

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Abstract: This paper explores the influence of gate metal engineering on the performance of Silicon-on-Insulator (SOI) MOSFETs. Conventional MOSFETs are prone to SCEs, which degrade their performance with size reduction. SOI MOSFETs provide improvements over conventional designs by minimizing SCEs. This study focuses on enhancing SOI MOSFET performance by introducing Dual-Material-Gate (DMG) technology. The DMG-SOI-MOSFET demonstrates significant advantages in suppressing SCEs and increasing drive current, which is beneficial for applications such as amplifiers. This paper compares electrical characteristics of single-gate (SG) and DMG SOI MOSFETs, revealing that DMG offers superior performance.

Keywords: SOI MOSFET, DIBL, SCEs, DMG, Threshold Voltage

Predicting Tea Quality Based on Antioxidant and Polyphenol Content Using Ensemble Machine Learning Model

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Abstract: Made from Camellia sinensis, tea is highly valued for numerous health benefits and rich phytochemical makeup. This research aims to determine whether antioxidant and polyphenol levels may be used to predict the quality of tea using machine learning techniques. The main objective is to improve prediction accuracy using ensemble models that integrate the Random Forest and Decision Tree methods. The results showed the effectiveness of the ensemble model, with up to 99.89% accuracy in polyphenol and antioxidant dataset tea quality prediction. The proposed research highlights the potential of machine learning to enhance the efficiency of tea production procedures, guarantee uniformity in product quality, and propel scientific comprehension of tea's nutritional and health advantages. By utilizing cutting-edge procedures, the tea industry may improve manufacturing processes and offer consumers high-quality goods enhanced with health-promoting phytochemicals.

Keywords: *Tea Quality Prediction, Quality Control, Machine learning, Ensemble Model*

Generating Diverse Facial Expressions and Orientations from a Single Image Using Conditional Generative Adversarial Networks

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Abstract: This paper offers a unique deep-learning model for manipulating facial expressions and image orientations, leveraging the power of conditional Generative Adversarial Networks. Building upon the Pix2Pix architecture, renowned for its efficacy in image-to-image translation tasks, our model learns intricate mappings between paired images—an input face and its corresponding target image with the desired expression and orientation.
We delve into our model's architecture and training regime, emphasizing its ability to disentangle and manipulate facial attributes. Trained and evaluated the IIITM Face Data dataset, our model demonstrates promising results in generating modified facial images exhibiting the target expressions and orientations. We explore the potential applications of this technology, spanning entertainment, human-computer interaction, assistive technology, and psychology. We aim to make impactful advancements in facial image manipulation by addressing ethical considerations.

Keywords*: Deep learning model; Facial Image; GANs; IIITM Face Data*

Accuracy Enhancement in Apple Leaf Diseases Detection and Classification Using VGG16

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Abstract: In the modern world, predicting the plant diseases is an important job for several reasons which includes the early detection and intervention of loss of crop and ensures to provide heathy fruits and vegetables. This prevents the further more spread of the diseases and intimates the farmers to make strategical and managemental decisions or the necessary actions that are to be taken. The idea of using Machine learning models is that it provides various processing techniques and ensemble models that improves the accuracy and efficiency of the analysis of the diseased plant. The research uses Convolutional Neural Network (CNN) for image recognition, Visual Geometry Group (VGG) for improved performance measures. This model increases the efficiency where it consists of several convolutional layers which are fully connected. This research utilizes the apple and maize plant's dataset to visualize and categorize the plant leaf diseases. This research presents the comparison of the proposed system and all other existing models mainly to highlight the significance of the proposed model.
Keywords— Apple Leaf; VGG16; Disease detection; Diseases Classification; DenseNet

Using Machine Learning to Predict Constant Obstructive Pneumonic Infection

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Abstract: Continuing obstreperous pneumonic infection is a gathering of respiratory circumstances that hinder wind current and cause breathing troubles. COPD forecast is just conceivable in cutting edge stages. The operation known as Lung Ultrasound Surface Wave Elastography accumulates datasets. At the point when ultrasound looks at lungs with a high convergence of extravascular lung water, normal resonation relics known as B-lines happen. B-lines have a sensible relationship with how much extravascular lung water. AI strategies can moderate this by determining the event of the sickness with the most significant level of accuracy. The essential goal is to give an AI calculation that can precisely gauge the worth of the lung illness file by giving expectation brings about the type of pneumonic infection order. We accomplish the most elevated level of accuracy by assessing the presentation of directed arrangement AI calculations. In addition, we compare and discuss the performance of various ML algorithms by analyzing the supplied dataset. This investigation expects to give a grouping report, distinguish the disarray lattice, and classify the information in light of need. The outcome demonstrates the suggested ML algorithm's efficiency.

Keywords— Infection; Pathologist; Diagnosis; Machine Learning; B Lines.

A Study on Axially Graded $Si_{(1-x)}Ge_{(x)}$ Nanowire Solar Cell with Monte Carlo Simulation

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Abstract: This paper presents a study on the performance of an axially graded Ge-$Si_{(1-x)}Ge_x$-Si p-n nanowire solar cell using Monte Carlo simulation. The nanowire structure consists of a germanium (Ge) cathode, silicon (Si) anode, and a variable $Si_{(1-x)}Ge_x$ middle region. The Silvaco code incorporates quantum mechanical effects such as Fermi statistics for carrier distribution, SRH recombination for trap-assisted processes and non-equilibrium transport using the Bi-Conjugate Gradient method. The study focuses on key photovoltaic parameters, including short-circuit current density (Jsc), open-circuit voltage (Voc), maximum power (Pm), and fill factor (FF), to assess the solar cell's efficiency. Through extensive simulations with different x compositions in the middle region, it is found that the Ge-Ge-$Si_{0.5}Ge_{0.5}$-Si structure delivers the best results, offering enhanced photovoltaic performance. We also conducted a comparison of the three different solar cell structures: (a) Ge-$Si_{(0.5)}Ge_{0.5}$-Si, (b) axially graded Ge-$Si_{0.1}Ge_{0.9}$-$Si_{0.5}Ge_{0.5}$-$Si_{0.9}Ge_{0.1}$-Si, and (c) core-to-shell graded Ge-$Si_{(1-x)}Ge_x$-Si. These findings provide insights into the optimal design of graded nanowire solar cells for improved efficiency.

Keywords*: Silicon-Germanium Nanowire Solar Cells, Monte Carlo Simulation, Scattering Mechanisms, Doping Concentrations, Carrier Transport, Quantum effect*

Vivaldi antenna with reconfigurable rectangular slots

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Abstract: This study presents a Tapered Slot Antenna (TSA) that achieves reconfigurability through electronic switches like RF-MEMS, PIN diodes, and photoconductive switches. The TSA features two switchable rectangular slots, allowing dynamic adjustments to its frequency band. By incorporating diodes, a notch band is created, enabling precise tuning of the antenna's frequency response.
The antenna operates in two modes: a wide bandwidth mode covering frequencies from 3.2 GHz to 9.5 GHz and a narrow band mode spanning 8.4 GHz to 8.7 GHz. The use of PIN diodes is essential for altering both the impedance matching and the radiation pattern. Simulation results demonstrate the antenna's ability to efficiently switch between modes, showing improved performance and flexibility.
This reconfigurable design offers a versatile solution for applications requiring dynamic frequency adjustment, such as in wireless communications and radar systems, where efficient use of the spectrum and adaptability to varying conditions are crucial.

Keywords*: Pin diode, reconfigurable antenna, radiation pattern, microstrip line.*

Design of second order low pass filter using inverter-based CMOS Operational transconductance amplifier (OTA) through g_m/I_D Methodology

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Abstract: This paper introduces the design of an inverter-based CMOS operational transconductance amplifier (OTA) utilizing the g_m/I_D methodology. The approach begins by representing the inverter as an amplifier with g_m being the transconductance and I_D being the drain current when both transistors are in the saturation region. Through this methodology, performance metrics such as gain, bandwidth, and output swing are optimized to meet specific application requirements. The paper highlights an optimized version of Nauta's OTA circuit, designed with the g_m/I_D approach in a 0.18 µm CMOS technology node, and examines the design of a second-order low-pass filter using the OTA. With the 0.18 µm CMOS process, the designed second-order low-pass filter achieves a tuning ratio of 20, a total power consumption of 5.1 mW, and a 3 dB bandwidth ranging from 10 MHz to 79 MHz.

Keywords g_m/I_D, *OTA, Nauta's OTA, filter*

IoT-Driven Automated Hydroponic System for Climate-Independent Indoor Crop Cultivation

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Abstract: The goal of this work is to create an automated hydroponic system that can produce popular crops indoors without relying on the outside weather. The system is designed by evaluating several hydroponic techniques to determine which ones are most suited for automation. The fundamental component of the system is a microcontroller, which interfaces with sensors to regulate the environment and reduce the need for human interaction. An IoT platform is incorporated to store and show system data, enabling remote access via a graphical user interface. With little assistance from the user, the system maintains ideal growth conditions and sends out real-time notifications for problems like low water levels. The system's efficacy is verified through testing and IoT platform monitoring. This device not only makes farming easier both indoors and outdoors, but it also provides academics with useful data to better understand the dynamics of plant development. This technology makes it possible to grow summer crops in the winter because it doesn't depend on the weather.

Keywords*: Soil-less cultivation; hydroponics; microcontroller; automation; IoT; indoor farming*

Performance analysis of MoS2/MASnI3/WSe2 based solar cell with more than 31% efficiency

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Abstract: In recent years, Perovskite solar cells have experienced significant advancements in performance, paving the way for their commercialization. Lead-based perovskites have achieved efficiencies exceeding 25% in single junction configurations. However, concerns regarding the toxicity of lead have shifted attention towards organic-inorganic halide materials in the solar cell sector. This report focuses on the performance of MASnI3-based perovskite solar cells, highlighting the importance of numerical analysis in the design of these devices. The study employs SACPS-1d, a one-dimensional solar cell simulator, to model an optimized MASnI3-based solar cell featuring a 2D WSe2 hole transport layer (HTL) and a 2D MoS2 electron transport layer (ETL). The integration of WSe2 and MoS2 with the MASnI3 absorber layer results in an impressive power conversion efficiency (PCE) of 31.77%, with a peak current density (Jsc) of 32.952212 mA/cm² and a voltage output (Voc) of 1.1173 V. This research contributes to a deeper understanding of single-junction perovskite solar cells.

Keywords*: perovskite, solar cell, scaps-1d, masni3, pce.*

Exploring the Potential of AlGaN/GaN HEMT using TCAD Simulations for Next-Generation Biosensors

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Abstract: This article investigate the performance of AlGaN/GaN HEMT in terms of bandgap energy, polarization charge concentration, total current density, current flowlines, effect of Al content and thickness of AlGaN layer on transfer and output characteristic. All the results have been extracted using the Silvaco Atlas device simulation tool. The result showed the presence of quantum well in the energy band diagram of structure due to 2 DEG. Polarization charge concentration, total current density and current flowlines are confined to the channel only. With increase in Al content and thickness of AlGaN layer the knee point of the transfer characteristic increased and maximum drain current, drain saturation voltage of output characteristic also get increased. Due to variation in thicknesses of the different layers and Al content in barrier layer, the current parameters of the device get modified which can be used as a sensing metric for biosensors**.**
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*Keywords**: High electron mobility transistor (HEMT); Two-dimensional electron gas (2DEG); Biosensor; AlGaN/GaN; Bandgap Energy*

Advancements in operational transconductance amplifiers (OTAs) for the design, applications, and performance optimization techniques with hardware implementation

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Abstract : This research paper presents the design and simulation of a novel architecture for Multiple Path Fully Differential Operational Transconductance Amplifiers (OTAs) with a Dual Flipped Voltage Follower, specifically developed for VLSI-based signal processing applications. Utilizing advanced 50nm CMOS technology and Cadence tools, the proposed OTA architecture achieves enhanced performance and versatility in handling various signal processing tasks. Design employs multiple signal paths, which contribute to improvements in bandwidth, gain, and linearity, while also effectively minimizing common-mode noise. This multi-path approach ensures better signal integrity and reliability in high-performance applications. The integration of the Dual Flipped Voltage Follower further strengthens the OTA's stability and dynamic range, allowing it to operate seamlessly in high-speed VLSI systems. The architecture is designed to cater to the rigorous demands of modern signal processing, where precision and speed are critical. Extensive simulation studies were conducted to validate the OTA design, and the results demonstrate that the proposed approach meets or exceeds the stringent requirements of today's signal processing applications. Findings of this research contribute to the ongoing advancements in VLSI design methodologies and provide a promising solution for engineers working with nanoscale CMOS technologies. Simulation results using Cadence tools highlights effectiveness and robustness of proposed design.

Keywords*: Simulation, Cadence, Operational Amplifier, Signal, VLSI, Voltage, Transconductance, Flip, Array, OTA. CMOS, Architecture.*

Impact of Defects on the Electronic Properties of (8,3) and (7,5) Carbon Nanotube Heterojunction

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Abstract: Carbon Nanotubes (CNTs) exhibit versatile electronic properties influenced by variations in their dimensions, chirality, and the number of CNTs. When CNTs of different chiralities form a heterojunction, the interface significantly affects their electronic properties. This paper simulates circumferential, grouped, and distributed defects at the interface of (8,3) and (7,5) chiralities and analyses the corresponding Density of States (DOS) and Zero-bias Transmission with respect to energy. The comparison between the individual DOS and transmission of (8,3) and (7,5) chiralities and those of the defects generated on the interface reveals the impact of defects on energy states and transport properties. Notably, the grouped defect introduces a new energy state at -0.3 eV, facilitating electron transmission at this lower energy level, which improves performance but also affects conductivity. This paper provides a detailed analysis of interface defects between (8,3) and (7,5) chiralities, highlighting their impact on energy levels and electronic properties, with results showing certain consistencies across different defects.

Keywords*: CNT Heterojunction; (8,3) chirality; (7,5) chirality, Density of States, Zero-bias Transmission*

Impact of the Process Parameter Variation on Threshold Voltage of Short Channel Junctionless MOSFET

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Abstract: In this paper, we investigate the impact of process parameter variations on the threshold voltage or VTH of short-channel Junctionless MOSFETs (JLMOSFETs). Hence, mainly the variability of the VTH due to the key fabrication parameters—such as doping concentration, channel length, gate oxide thickness, and work function have been analyzed for the different oxide materials and the channel materials. MATLAB and SILVACO ATLAS-based simulations have been done to analyze the threshold voltage variability. Understanding these interactions is vital for optimizing the performance of JLTs and ensuring their viability for future generations of electronic devices..

Keywords*: Junctionless MOSFET, Threshold Voltage, variability, Work Function*

Design of Power-Efficient Built-in Self-Repair for Interleaved Memory Systems

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Abstract: Trillions of memory cells are fabricated into the fingertip area of a semiconductor wafer. Therefore, it is almost impossible to ensure that there will be no defects after manufacturing. Various kinds of memory faults may arise after fabrication. Hard faults like, Stuck-at faults, address decoding faults, coupling faults as well as Soft faults also degrade the performance of a memory system. Recently Built-in Self-Test (BIST) and Built-in self-repair (BISR) mechanisms have been incorporated with the memory module to make it fault-tolerant. This paper proposes a power-efficient BISR architecture for interleaved memory to retain the system's reliability and increase the throughput. The proposed architecture consists of several redundant memory banks with an on-demand power-on feature which reduces power dissipation. HDL simulation of this work has been done using AMD Vivado and the proposed architecture is also implemented on FPGA (Spartan-7).

Keywords*: Built-in Self-Repair (BISR); memory interleaving; power efficiency; Built-in Redundant Analysis (BIRA); FPGA; Redundant Memory.*

Design of Humanoid Hand with Adaptive Gripping Patterns using Vision Sensor

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Abstract: In the realm of robotics, the emulation of human like dexterity and adaptability remains a formidable challenge. This work presents the design of a 5-degree-of-freedom (5-DOF) humanoid hand capable of adaptive gripping through the integration of learning-based techniques. The system utilizes a camera sensor for real-time object detection, guiding the hand's gripping actions via a learning-driven mapping function. A learning-based technique is implemented for object recognition, enabling the hand to adapt to various dynamic scenarios. Experimental results demonstrate the effectiveness of the camera sensor in driving adaptive gripping actions. The proposed approach highlights the potential for more sophisticated and capable robotic systems, contributing to the evolving landscape of human-robot collaboration.

A First-Principle Investigation of Sc-Doped MoS_2 for Hydrogen Gas Detection

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Abstract: This study investigates the electronic and adsorption properties of MoS_2 and Sc-doped MoS_2 (Sc-MoS_2) monolayers for H_2 detection using Density Functional Theory (DFT). We calculated the adsorption energy (Ead), charge transfer (Q_T), and adsorption distance (D) to characterize the adsorption properties. To further understand the effect of H_2 gas adsorption on electronic characteristics, we evaluated the bandgap, Total Density of States (TDOS), and Projected Density of States (PDOS). With Sc doping, the bandgap of the MoS_2 reduced from 1.77 eV to 0.15 eV suggesting the improvement in the conduction property of MoS_2. The adsorption energy for H_2 on Sc-MoS_2 is -4.8 eV, stronger than that of pristine MoS_2. This study suggest that Sc-MoS_2 is a promising material for H_2 gas detection. These results highlight the potential of Sc-MoS_2 in gas sensitivity applications, particularly for detecting H_2 leakage, providing a theoretical basis for its use in sensor technology.

Keywords*: DFT, H_2 Detection, Sc-MoS_2, GGA-PBE, DFT*

A First-Principle Study to investigate Electrical and Optical Properties of Tin Oxide

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Abstract: This paper explores the electrical and optical properties of SnO2, a prominent Transparent Conducting Oxide (TCO), using Density Functional Theory (DFT). TCOs are essential for optoelectronic applications due to their unique combination of transparency and electrical conductivity. The study focuses on critical electrical properties, including the band gap (Eg), Total Density of States (TDOS), and Partial Density of States (PDOS). SnO2 exhibits a direct band gap at the Γ point, with tin (Sn) electronic states contributing significantly to the conduction band, enhancing electrical conductivity. The optical analysis, particularly of the dielectric function in the ultraviolet (UV) region, reveals substantial electron transitions from the valence to the conduction band. The material demonstrates significant optical responses across the visible, vacuum ultraviolet (VUV), and UV regions. These findings underscore SnO2 potential in photonic and optoelectronic applications, providing valuable insights for optimizing TCO-based devices and advancing transparent conductive material technology.

Keywords*: Tin oxide (SnO2), electronic properties, optical properties, DFT, GGA*

A First-Principle Investigation of Sc-Doped MoS_2 for Hydrogen Gas Detection

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Abstract: The investigation of respired breath was done to examine the potential of the P-doped WSe_2 (P-WSe2) monolayer for identifying lung cancer biomarkers. The geometric adsorption, and electronic characteristics of the P-WSe_2 monolayer, for three Volatile Organic Compounds (VOCs), namely, 2-propenal (C_3H_4O), propanal (C_3H_6O), and isoprene (C_5H_8) are investigated based on the Density Functional Theory (DFT). The Adsorption Energy (Ead) was calculated to be −0.6 eV, −0.57 eV and −1.31 eV for C_3H_4O, C_3H_6O, and C_5H_8 gas, respectively. The Density of States (DOS), binding energy, charge transfer, and desorption time at temperatures 298 K, 348 K and 398 K have been reported in this work.

Keywords*: WSe2, DFT, GGA, Sensor, VOCs, Lung cancer*

Implementation of High-K Gate Dielectric in Cylindrical SOI Schottky Barrier MOSFET for Enhanced I_{ON}/I_{OFF} Ratio

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Abstract: In this work, we propose novel device architecture titled gate stack Cylindrical SOI Schottky barrier MOSFET transistor (GS-SOI-SB-CGAA). The analog/RF characteristics of the proposed structure are extensively investigated using Silvaco, which is a well-known simulator used for three-dimensional devices. This proposed MOSFET is being compared with schottky-barrier gate all around MOSFET (SB-CGAA) and silicon-on-insulator Schottky-barrier gate all around MOSFET (SOI-SB-CGAA) to investigate the analog/RF characteristics. The GS-SOI-SB-CGAA MOSFET demonstrates improved analog/RF characteristics for off-state drain current, I_{ON}/I_{OFF} ratio, and device capacitance.

Keywords**:** *GAA MOSFET ; SOISB MOSFET ; I_{ON}/I_{OFF} ratio ; Analog/RF parameters*

Design and performance analysis of low noise amplifiers: A review

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Abstract: This article discusses the current state of low noise amplifiers (LNAs) and their crucial role in enhancing weak signals across various applications. It explores key design considerations, semiconductor technologies, and recent advancements in reducing noise figures and improving frequency performance. The article examines specific LNA architectures, emphasizing the importance of low power consumption, input-output synchronization, and high gain. Additionally, it compares different types of LNAs based on noise performance, gain, and frequency range, highlighting the evolution of technology from vacuum tubes to solid-state transistors. Emerging trends and future directions in LNA design for next-generation communication systems are also addressed.

Keywords: *Gain, noise figure, power consumption, trade-off, low noise amplifier.*

Mapping Stress/Strain in Nanoscale FinFETs: Implications for Device Design

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Abstract: This paper presents a comprehensive study on the mapping of stress and strain in FinFETs and explores its implications for device performance. The investigation focuses on the characterization of stress and strain distribution in three-dimensional FinFET structures using advanced modeling and simulation techniques. The impact of stress and strain on device parameters such as carrier mobility, threshold voltage, and overall performance is analyzed in detail. The study highlights the importance of understanding the spatial distribution of stress and strain in FinFET devices and its influence on device behavior. Insights gained from this research can help in the optimization of FinFET design and fabrication processes to enhance device performance and reliability.

Keywords*: Stress; Strain; 3D-FinFET; Device Design.*

Analysis of Stress and Strain Dynamics in Sub-7nm GAA Si- and SiGe-Channel Nanosheet FETs

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Abstract: This work underscores the importance of stress/strain engineering in nanosheet FETs and provides a detailed explanation of the stress fields within a 3-stack Si and SiGe channel nanosheet FETs. The importance of stress management in silicon and SiGe-channel nanosheet FETs and a detailed quantification of the stress fields within these devices are discussed. A 3D numerical simulation study reveals that stress/strain engineering techniques can enhance the performance of Gate-all-around (GAA) vertically stacked nanosheet field-effect transistors (NSFETs) for 7 nm technology nodes. The choice between SiGe and/or Si channels ultimately depends on the specific application requirements, with SiGe being more suited for high-performance applications and Si being preferred for applications where reliability is paramount. This work has demonstrated the advantages of using multiple nanosheet stacks in strained-SiGe NSFETs.

Keywords*: Nanosheet; SiGe; Stress and Strain; GAA; FETs.*

Junctionless Accumulation Mode Dual Gate Ferroelectric FET (JAM-DG-FE-FET) for High Cut-off Frequency Applications

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Abstract: Using TCAD Silvaco ATLAS simulator the ferro, fermi, Lombardi CVT model, Shockley-Read-Hall (SRH) recombination models, Junctionless Accumulation Mode Dual Gate Ferroelectric FET (JAM-DG-FE-FET) has been suggested and evaluated for RF/analog specifications. When comparing the JAM-DG-FE-FET configuration to the Junctionless Accumulation Mode Ferroelectric Field Effect Transistor (JAM-FE-FET) setup, key analog metrics such as g_m, A_v, g_d, and early voltage (V_{EA}) are obtained. Subsequently, the suggested apparatus undergoes frequency examination, and several crucial radiofrequency characteristics, such as f_T is noted about the Junctionless Accumulation Mode Dual Gate Ferroelectric Field Effect Transistor (JAM-DG-FE-FET). Therefore, when compared to Junctionless Accumulation Mode ferroelectric FETs (JAM-FE-FET), Dual Gate Junctionless Accumulation Mode ferroelectric FETs (JAM-DG-FE-FET) have been discovered to have improved analogue and RF performance. Therefore, it can be said that the JAM-DG-FE-FET device that is being shown here is a strong candidate for use in high-frequency systems.

Keywords*: Radio Frequency parameters; Ferroelectric;* HfO_2

Field Effect Transistor Incorporating Negative Capacitance and Nanowire Structures for the Attenuation of Gate Leakage Phenomena

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Abstract: This manuscript discusses a detailed comparative exploration of conventional nanowire field-effect transistors (NW FET) and negative-capacitance field-effect transistors (NC-NW FET) concerning gate leakage phenomena. Various pivotal parameters such as Contour Plots of Electron Velocity and Hole Concentration, Tunnelling Distance, Gate Induced Drain Leakage (GIDL), Band Diagram, Subthreshold Slope (SS), and Transconductance are analyzed at varying channel lengths. This study demonstrates a significant decrease in gate leakages from 10^{-8} A to approximately 10^{-14} A, underscoring the superior performance of NC-NW FET.

Keywords*: Ferroelectric, Gate-Induced Drain Leakage, Nanowire, Short Channel Effects.*

A Comparative Power & Delay Analysis of Full Adder Designs in 90nm CMOS and 32nm & 5nm CNFET Technologies

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Abstract— Adders are the most important building blocks for any digital system. As the transistor technology is scaling down, reliable adder operation with the least power consumption and delay is desirable. CNFET technology has proved to be effective for different digital circuits and systems. To establish the reliability of CNFET-based full adders and predict their performance metrics compared to the CMOS technologies, this paper presents a comparative power and delay analysis of full adder circuits implemented using Carbon Nanotube Field-Effect Transistors (CNFETs) of 32nm and 5nm technology nodes and Complementary Metal-Oxide-Semiconductor (CMOS) at 90nm technology node. The study aims to evaluate the performance of these technologies in terms of power consumption and propagation delay. Simulations were conducted using Cadence Virtuoso simulation tool to ensure accurate and reliable results. Our findings indicate that CNFET-based full adders demonstrate superior performance in terms of speed and power efficiency, particularly at smaller technology nodes. This comparative study provides valuable insights into the full-adder designs using CNFET and CMOS technologies, guiding future research and development in the design of high-performance digital circuits.
Keywords—Full Adder, CNFET, CMOS, Power Consumption, Propagation Delay.

New locally-active memristor for neuromorphic application

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Abstract: Due to the low energy consumption and exceptional computational efficiency, neuromorphic computing, based on artificial neurons and synapses, has garnered significant attention. The locally-active memristor (LAM) is a promising candidate for artificial neural networks, highlighting its potential applications in neuromorphic computing. This study proposes a memristor with locally-active characteristics to implement its typical behaviour in neuromorphic computing. Several numerical and theoretical analyses exhibit the behaviours of the proposed LAM model, including non-volatility, and local-activity. The validation of the proposed memristor is physically experienced through the Arduino Uno. Finally, the proposed LAM-based crossbar array is utilized as a kernel of convolutional neural network (CNN) for application in image recognition with 98.28% accuracy.

Keywords*: LAM, Arduino-Uno; neuromorphic application; image recognition; memristive crossbar*

Silicon Membranes for Microbolometers: Simulation and Fabrication Using Frontend Bulk Micromachining

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Abstract:
This paper presents a novel, simple, and cost effective approach for fabricating monolithic silicon membranes through frontend bulk micromachining for microelectromechanical (MEMS) systems. Innovative mask designs with different geometries are proposed for use as pixels in Microbolometer applications, aiming to achieve reliable and area-efficient microstructures. The design aligns rectangular openings at a 45° angle to the primary flat of the wafer, exposing only the (100) planes for wet anisotropic etching. However, these rectangular openings result in significant silicon consumption, reducing the pixel fill factor. To address this, alternative geometries are introduced to minimize area consumption in undesired directions. Simulations using Intellisuite FABSIM show that wet etching alone (Method I) results in greater silicon consumption, while a combined dry and wet etching technique (Method II) achieves an 86% reduction in footprint. A single-pixel membrane was fabricated as a proof of concept using Method I, with simulation and experimental results showing strong agreement. The resulting robust, monolithic membrane is well-suited for various sensing applications.

Keywords*: Si-Membrane, etching, MEMS, bulk micromachining*

Spoonie: Self-Stabilizing Feeding Spoon For Tremored Hands

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Abstract: Spoonie is a self-stabilizing feeding spoon designed for people who have Parkinson's disease, elderly persons, and babies who cannot hold their hands steadily during their meals. The spoon is so uniquely designed that the spoon head remains stable, thus automatically correcting for shakiness or other unwanted movements that would allow easier and classier feeding. It is powered by a microcontroller that controls servo motors in relation to real-time data from an accelerometer, ensuring the spoon head remains at a steady level, even if a user's hand is shaking or moving unpredictably. With this spoon, users are able to self-feed without any assistance, hence improving their quality of life. The self-stabilizing spoon represents a breakthrough in assistive technology that really helps people with motor control issues in solving practical dilemmas every day. Further refinements could include adjustable settings for different levels of stability so that the device is much more attuned to individual needs.

Keywords*: Self-Stabilizing; Assistive Technology; Tremor Control; Motor Disabilities; Independent Eating.*

Effect of AlGaN Thickness Variation on the Analog Performance of a Normally-off AlGaN/GaN based Double Gate MOS-HEMT Device

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Abstract: — This study investigates the influence of AlGaN layer thickness variations on the analog performance of a normally off AlGaN/GaN based double gate MOS-HEMT device. The analog metrics considered encompass the transconductance generation factor (TGF), transconductance (gm), output resistance (r0), the conduction band energy diagram and drain current (Id) with respect to the gate voltage (Vgs) and drain voltage (Vds). A meticulous analysis of the analog performance underscores that the electrical properties of the device are profoundly affected by the AlGaN layer thickness. A device with an AlGaN thickness of 20 nm demonstrates a substantial 48.96% increase in ON current when juxtaposed with devices possessing greater thicknesses. Furthermore, a thinner AlGaN layer yields an 83.56% enhancement in peak transconductance.

Keywords: *GaN/AlGaN heterojunction, Double Gate (DG), MOS-HEMT, AlGaN layer, normally-off, Analog.*

A µW Power CMOS Window Detector Circuit with Adjustable Thresholds for Low-Power Applications

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Abstract: An adjustable threshold CMOS window detector based on latch comparator is proposed here which compares between two DC threshold values. The threshold values are user adjustable. The window detector is based on a Pre-amplifier based latch comparator which is a significant part of the Analog to Digital converter (ADC). The proposed circuit is designed in SCL 180nm standard CMOS technology 1.8 V power supply. The window detector generates output with a maximum frequency of 18 MHz and 55ns delay. The proposed circuit uses a custom designed XOR gate which takes input from the comparator. The adjustable window length can be closer to supply VDD to Gnd. The total dynamic power consumption of the proposed circuit is 32µW, which is less than some of the recently reported works.
Keywords*: Window detector, Latch comparator, Pre-amplifier*

Analyzing the Analog performance of a Novel Normally OFF Double Gate MOS-HEMT due to Gate Length Variation

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Abstract: The Normally OFF Double Gate High Electron Mobility Transistor (DG-HEMT) represents a significant advancement in semiconductor technology, offering exceptional performance in high-speed and high-frequency applications. As a normally-off device, it enhances both safety and efficiency by necessitating a gate voltage to trigger conduction, thereby lowering power consumption and minimizing the risk of unintended operation. This study explores how variations in gate length (300 nm, 600 nm, and 900 nm) affect the performance of MOS-HEMTs. The results indicate that a 900 nm gate length leads to a 60.35% increase in drain current (Id) and a 99% improvement in gain, emphasizing the critical role of gate length optimization in achieving superior device control and performance. With their high electron mobility, elevated breakdown voltage, and low on-resistance, MOS-HEMTs are poised to play a crucial role in the future of fast, efficient, and reliable electronic technologies.

Keywords: *MOS-HEMT, Double Gate, gate length variation, Normally OFF device.*

Enhancing Ultrasonic-Based Distance Measurement Accuracy Through Error Correction Mechanism

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Abstract: This paper introduces a pioneering approach to ultrasonic-based distance measurement using ultrasonic sensors. Recognizing the influence of diverse weather conditions on measurement accuracy, an error correction mechanism is proposed to enhance precision. An Artificial Neural Network (ANN) model is deployed and trained on diverse weather datasets to mitigate errors effectively. The proposed model achieves an impressive 98.42.

Keywords*: Ultrasonic Distance Measurement, ANN Model, DHT11, HC-SR04*

Performance Optimization of Thin Film Micro-Patterned Piezoresistive Low Pressure Sensor

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Abstract: An array of micro-structured piezoresistive pressure sensors often becomes suitable for low-pressure environmental applications. In this work, we studied two different thin film arrays of triangular and pentagonal structures with different piezoresistive materials and structural configurations. Sensor parameters, such as Von Mises stress, resistance variation and linearity, etc., were evaluated using finite element method. The 0.5 µm height of the triangular structure achieves a higher sensitivity of 10.52 and thus shows the improved design of MEMS (Micro Electro Mechanical System) based piezoresistive pressure sensor. Different piezoresistor configurations also simulated using COMSOL Multiphysics software to obtain the optimal sensing outputs. We observed the best variation in resistance with the triangular and pentagonal array structures having a low-pressure range of 1 Pa to 10 Pa. The maximum deformation of 0.064 µm and 0.052 µm are also determined for both triangular and pentagonal array structures of 0.5 µm in height, respectively. The simulation results show that proper selection of the piezoresistor geometrical structure, shape, and dimensions allows possibilities to improve the sensor sensitivity for low-pressure applications.
***Keywords**: Piezoresistive pressure sensor; MEMS; Finite element method; Sensitivity; Optimization.*

A Fully-Customized RTL to GDS Design and Verification of Low-Power Cache Memory

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Abstract: In this paper, we have reported low-power cache memory with DFT and scan chain techniques utilizing RTL to GDS (Register-Transfer Level to Graphic Design System) implementation in the Cadence Innovus tool using 45 nm technology. In the frontend design, the gate level synthesis is carried out using the Cadence Genus tool with input files i.e., the Verilog file, design constraint, and library file which also generates the gate level netlist file. In the backend design, the physical design implementation is proposed including different intermediate levels such as synthesis, placement, routing, and timing analysis to optimize the design in terms of power, timing, and area. We have proposed a low-power cache memory including a clock gating technique to reduce the dynamic power consumption. It is estimated that the total power consumption of the proposed Low Power Cache Memory design is 20% less than the standard cache memory design. We have studied the superflow, a fully customized RTL to GDS design flow tailored for low-power cache memory, and also reported power and timing analysis. This paper emphasizes the importance of each stage in the ASIC design cycle, highlighting every phase- starting from design specification, architecture design, RTL coding,

synthesis, place and route, and verification—plays a critical role in shaping the final performance with ample opportunities for future research optimizing the design for enhanced performance.
Keywords: *Cache, ASIC, Cadence, low power, Physical design.*

Novel Modular Adder Using Thermometer Coding and One-Hot Coding for Residue Number Systems Applications

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Abstract: The goal of effective modular adder designs with thermometer coding and one-hot coding using tristate buffers is to improve modular arithmetic performance while reducing power consumption and utilizing the performance of digital circuits. Residue Number Systems (RNS) were an effective alternative solution to Positional Number Systems based on the performance. Low-power Thermometers and one-hot coding are used in embedded and Internet-of-things edge devices. Tristate buffers govern data flow in digital circuits, particularly those with high impedance states. The most significant and common operation performed on RNS components, such as forward and reverse converters and channel arithmetic units, is modular addition. When these components are coupled with a residue numbering system, the carry during addition is ignored. This method might be useful in applications where performance is improved and speed and power consumption are important aspects. The proposed modular adders, which use thermometer coding and one-hot coding, enhance latency by 33% and 30%, circuit area by 22% and 12%, and energy consumption by 23.5% and 5%, respectively.

Keywords*: Residue Number System (RNS), Thermometer Coding (TC), One-Hot Coding (OHC), Tri-State Buffers, Modular Addition, Forward Conversion, Reverse Conversion.*

Design of VTFET based biosensor utilizing Ambipolar Current in detection mechanism

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Abstract: This work presents a vertical TFET-based biomolecule biosensor which utilizes ambipolar current of the VTFET as a parameter for sensitivity measurement. Unlike conventional TFET biosensors, which captures biomolecules at the source side, the proposed biosensor is designed to capture biomolecules at the drain side. Additionally, the biomolecule receptors are positioned on an open sensing surface to capture the biomolecules as opposed to the enclosed cavity used in FET-based biosensors. The highest ambipolar current sensitivity of 4.18 × 10 5 is recorded in this work. Biomolecules vary in size and orientation and may create different biomolecule layer thickness after being attached to the receptors. A study is done to find the effect of this biomolecule layer thickness on the sensitivity of the biosensor. It is observed that sensitivity increases with increase of the biomolecule layer thickness. A 10 nm thickness of the biomolecule layer produces highest sensitivity in this work.

***Keywords**: Vertical TFET (VTFET), Heterojunctions, Band-to-Band Tunneling, Ambipolar Current Sensitivity, BTBT*

Investigating the device and circuit level performance of nanoscale double gate junctionless transistors

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Abstract: The junctionless transistors (JLT) have been evolved as a device which is free from the need to fabricate the p-n junctions in semiconductor layer. In present work, the nanoscale double gate junctionless transistors have been designed with physical gate length of 16 nm. The doping concentration and gate's work function of p-type device has been optimized to equate its threshold voltage with that of n-type JLT. The performance of both p-type and n-type JLTs have been observed and found that the devices reflect ON-current of the order of 10^{-4} A/µm, OFF-current in the range of 10^{-9} A/µm, ON/OFF current ratio of the order of 10^5.Furthermore, these devices have been used to implement an inverter circuit in Mixed-mode simulator of Silvaco technology computer aided tool (TCAD) which successfully reflects the voltage transfer characteristic. The implemented inverter successfully reflects the voltage transfer characteristics for various values of V_{dd} which enables these devices as an alternative of MOSFETs for low power circuit applications.

***Keywords**: Nanoscale, Double gate, Junctionless, Transistor, Semiconductor, TCAD*

Effect of Hole Transport Layer on Tin based Perovskite Solar Cells

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Abstract- Nnumerical analysis has been presented for different organic and inorganic hole transport layer (HTL) in Tin based perovskite solar cell. Basically Organic HTL (Spiro-OMETAD) and Inorganic HTL (Cu_2O, NiO, CsSCN) material has been used in this Tin based perovskite structure. The thickness (in µm) and electrons affinity (in eV) of the different HTL layer also varied and observed the result. As per numerical simulation perform by Scaps-1D, we can conclude that highest PCE obtain by thickness variation for NiO is 23.93and also it maintain its efficiency throughout the thickness variation of .050 µm to .350 µm thickness also we can observed that under electron affinity variation highest PCE obtained by Cu_2O (electron affinity 3.40eV) is 24.12%.So we can conclude that for ZnO as an electron transport layer we can use inorganic HTL (Cu_2O, NiO) to obtain better efficiency as well as stable efficiency(NiO) compare to organic HTL(Spiro-OMETAD).

***Keywords*: Electron transport layer, Hole transport layer, Hybrid Perovskite Solar cell**

Design Methodology and Photovoltaic Performance Analysis of $GaAs_{0.99}Bi_{0.01}$ Nanowire Solar Cell

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Abstract: III-V alloy semiconductor $GaAs_{1-x}Bi_x$ is a promising material for photovoltaic applications because of its tunable bandgap with varying mole fraction. We investigated the potential of $GaAs_{1-x}Bi_x$ alloy when implemented in nanowire homo junction solar cell having radial as well as axial doping profiles, heterojunctions with organic materials as well as carrier selective contacts in our previous works. A brief comparative analysis considering optical performance of $GaAs_{1-x}Bi_x$ solar cell (SC) implementing nanowire (NW), nanopyramid (NP) and inverted nanopyramid (INP) structure have been presented here. We considered 1% Bi mole fraction according to our previous published reports. The optical performance analysis begins with geometry optimization of all the structures with respect to generated short circuit current density (J_{sc}) considering ideal condition of unity internal quantum efficiency (IQE). The variation in generated ideal J_{sc} is justified with respect to photo absorption spectra as well as photo generation rate profile. The study reveals best result for nanowire geometry as compared to other nanostructures. We finally present the solar cell figures of merit with optimised geometrical condition. Band diagram for nanowire solar cell is also presented to obtain the open circuit voltage. NWSC structure offers a maximum PCE of ~19% for a SRH minority carrier lifetime (τ_n) of 10 ns.
***Keywords**: Nanowire solar cell, $GaAs_{1-x}Bi_x$; and Nanostructure*

Theoretical Investigation of $CsSn_{1-x}Ge_xI_3$ perovskite solar cells using Graded Bandgap Profiles

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Abstract: The continuous rise in the energy demand of the world encouraged research in the manufacture of more efficient cost-effective solar cells. Sn and Ge became a promising alternative to the toxic lead used in conventional perovskite solar cells (PSCs) to reduce environmental hazards. For this work, we studied the effect of band gap grading of $CsSnI_3$-based PSCs by adding a fraction of Ge atom to the absorber material using Vegard's law in SCAPS. We have analyzed the variation of PCE while increasing composition x in $CsSn_{1-x}Ge_xI_3$ from 0 to 1 in the interval of 0.25. It is obtained that PSC having active layer made of $CsSn_{0.75}Ge_{0.25}I_3$ having a band gap of 1.375 eV shows a better performance (PCE of 17.57%) as compared to pure planar $CsSnI_3$ (PCE of 16.05%) and $CsGeI_3$ (PCE of 14.28%) based PSCs. We have done the band gap grading studies of the perovskite layer by using the optimized grading profile. It is observed that the photovoltaic efficiency of the device increased from 16.05% for planar $CsSnI_3$ to 20.06% for high gradient double graded absorber ($CsSn_{1-x}Ge_xI_3$ /$CsSnI_3$/$CsSn_{1-x}Ge_xI_3$), 19.45 % for high Gradient Front Graded ($CsSn_{1-x}Ge_xI_3$/$CsSnI_3$) and 17.88% for high Gradient Back Graded ($CsSnI_3$/$CsSn_{1-x}Ge_xI_3$) on band gap grading.

***Keywords**: Lead free, $CsSnGeI_3$, Band gap grading, Vegard's law*

Investigation of the Recombination Processes in $FA_{0.75}Cs_{0.25}SnI_3$ based Perovskite Solar Cell: A Theoretical Framework using SCAPS-1D

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Abstract: This study deals with the recombination mechanism in the lead-free $FA_{0.75}Cs_{0.25}SnI_3$ (FACsSnI3)-based perovskite to analyzing the performance of the solar cell (SC) using the SCAPS-1D tool. First, we modelled the device with $FA_{0.75}Cs_{0.25}SnI_3$ as an absorber layer. SnO_2 and PTAA are used as the electron and hole transport layer (ETL and HTL). The recombination losses in the device, which bound the performance of PSC. Hence, the investigation of the effect of the Shockley-Read Hall, radiative, and Auger recombination on the performance of SC is crucial for enhancing the performance of the device. The ITO/SnO_2/$FACsSnI_3$/PTAA/Au PSC structure was studied and shows a PCE of 25.03 % with V_{oc} of 0.95 V, J_{sc} of 34.71 mA/cm_2, and FF of 76.28 % with the optimal absorber thickness of 0.8 µm, acceptor doping density (NA) of 10^{17} cm^{-3}, trap density 10^{15} cm^{-3}, Auger electron/hole capture coefficient ($C_{n/p}$) of 10^{-29} cm^{-6}/s and radiative recombination coefficient (B) of 10^{-11} cm^3/s. Finally, the main obstacles must be addressed to overcome the defect density (N_t) within the perovskite layer for better performance.

Keywords*: Lead-free Perovskite, Auger recombination, radiative recombination, SRH, $FA_{0.75}Cs_{0.25}SnI_3$*

On the Potential of HEMT for Millimeter-Wave Applications and Integrated Circuits for 5G Transceivers: A Review

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Abstract: Millimeter-wave amplifiers are the crucial component in 5G wireless communication systems, operating at frequencies between 24 GHz and 100 GHz. They are used to amplify weak signals, compensating forpropagation losses and ensuring reliable datatransmission. The interesting properties of HEMT such as high frequency operation, low noise figure, high powerdensity, high gain, and low power consumption, highlinearity, robustness makes them a potential contender for millimeter-wave amplifiers.

Keywords*: AlGaN; GaN; HEMT; 5G Technology.*

Analysis of Membrane Yield in Insulated Air-Patched Capacitive Transducers for High-Frequency Applications

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Abstract: This study uses Finite Element Method (FEM) to simulate a microelectromechanical system (MEMS) based Capacitive Micromachined Ultrasonic Transducer (CMUT) cell, emphasizing the effect of air patches on the device's functionality. The analysis reveals total capacitance of approximately 0.46615 pF, resonant frequency of 2.7287 MHz and maximum membrane displacement of 16.534 nm. The presence of air patch reduces the capacitance due to air's low permittivity, which influences displacement while leaving the natural frequency unaffected. The model also demonstrates a higher collapse voltage of 108.9 V, indicating enhanced robustness. The optimal performance is achieved within a bias range of 40-60 V, capable of withstanding pressures up to 3 atm. These findings provide crucial insights for designing CMUTs with air patches for ultrasonic applications.

Keywords*: MEMS; Ultrasound; CMUT; SiC; Circular diaphragm; Displacement; Membrane Yield; Collapse Voltage; COMSOL*

The Parametric Studies of a Clamped-to-Clamped Resonant Beam Accelerometer

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Abstract: In this work, an advanced MEMS based vibrating beam accelerometer has been reported. Parametric analysis is done for Clamped vibrating beam. For the vibrating beam, multiple modes of simulation have been performed. Using the FEM model, natural frequency of the vibrating beam was found to be 123 kHz. Any change in thickness has no effect on the natural frequency. Axially pressure applied to the beam has been performed and found shift in frequency. Additionally, bias analysis of the vibrating beam has been studied.

Keywords*: Electrode biasing, Natural frequency of the beam, Deformed shape, Modes of the beams, Shift in frequency.*

Predictive modeling of Nanoscale Junctionless FinFET using XGBoost

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Abstract: In recent years, computing performance has been increased and new Machine Learning (ML) algorithms has been developed for fast and accurate prediction. With increasing demand for quick estimation of semiconductor device parameters during the early stages of development, prediction using ML is essential for new technology. Tree boosting type of algorithms are highly efficient among the regression algorithms where dataset is comparatively small and nature of the dataset does not support linear regression. Dataset generated through TCAD simulation is highly time consuming and internal device physics supports non-linear nature in the dataset produced. In this paper, machine learning model using Extreme Gradient Boosting (XGBoost) algorithm has been trained with a dataset of semiconductor device, generated from TCAD simulation and is used for device performance prediction. This fast and accurate prediction method will certainly be a real alternative to TCAD in the semiconductor industries.

Keywords*: Tree regressor, XGBoost, Machine learning FinFET, TCAD simulation*

Sensitivity Investigation of Gate Stack Junctionless GaAs FinFET based NH_3 Gas Sensor

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Abstract: This work presents, designing and analysis of gate stack junctionless Gallium Arsenide FinFET (GS-JL GaAs FinFET) for ammonia (NH_3) gas sensing application using Cobalt (Co) as sensing gate electrode. To improve the sensing performance and reduce leakage current, stacking of SiO_2/HfO_2 has been used. The sensing mechanism of GS- JL GaAs FinFET NH_3 sensor is based on work function modulation of Co upon exposure to NH_3. Extensive simulations of proposed sensor have been performed using Sentaurus TCAD simulator. The presence of NH_3 is identified by observing the variation in surface potential and other sensing metrics such as threshold voltage, transfer characteristics and transconductance. Sensitivity as a function of OFF current ($S_{I_{OFF}}$), threshold voltage ($S_{V_{TH}}$) and switching ratio ($S_{I_{ON}/I_{OFF}}$) have also been investigated. Simulation outcomes show that GS-JL GaAs FinFET NH_3 sensor offers maximum $S_{I_{OFF}}$ of 4.75 x 10^3, $S_{V_{TH}}$ of 0.43 and $S_{I_{ON}/I_{OFF}}$ of 2099 at work function change of 200 meV.

Keywords*: gate stack junctionless GaAs FinFET (GS-JL GaAs FinFET,) Ammonia (NH_3) gas sensor, Sensitivity, Cobalt (Co)*

Enhanced Crop Yield Prediction by Machine Learning Techniques

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Abstract: India's economy is based primarily on agriculture. The need for agriculture has increased along with India's population growth during the previous ten years. However, climatic changes and poor irrigation is a major threat to agricultural practices in India. Many farmers practice agriculture solely based on their experience which in a way reduces productivity and effectiveness. Machine learning techniques provide effective recommendations and predictions, helping to scale the production of crops across the country effectively. There are many Machine learning-based algorithms and techniques which help us accomplish effective solutions to such problems. In this work, Random Forest algorithm proposed which predicts the crops based on weather factors and soil factors. The weather factors include Rainfall, Temperature and Humidity. The soil factors include the chemical composition of the soil such as NPK values and pH of the soil. Real-time data used for the weather conditions, which makes the model robust and scalable. The test results will show two crop names along with their yield which are best suited for the respective conditions. Random Forest Classifier used for crop name recommendation and Random Forest Regressor for crop yield prediction. These results will assist farmers to grow crops effectively and increase production of crops.

Keywords*: Agriculture; Crop yield; Real-time data; Random Fores; , Weather conditions; Soil composition; Machine Learning.*

Digital Predistortion Behavioral Modeling of Power Amplifiers: A Neural Network-Based Approach to Nonlinearity Compensation

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Abstract: This paper introduces a novel digital Predistortion (DPD) algorithm created with a neural network (NN) framework to mitigate nonlinear distortions in GaN HEMT power amplifiers(PAs). The neural network-based method is based on a polynomial model, refined to accurately represent the dynamic AM- AM and AM-PM distortions that occur when the PA processes quadrature phase-shift keying (QPSK) modulated signals. A principal characteristic of the model is the integration of distinct sub- systems for each memory node, allowing it to adjust the quantity of output nodes in accordance with the time-varying attributes of the input signal. The proposed method exhibits significant enhancements in adjacent channel power ratio (ACPR) and error vector magnitude (EVM) when compared to conventional and advanced neural network-based DPD techniques. It attains a reduction of over 7 dB in EVM and improves ACPR by 3 dB relative to the generalized memory polynomial (GMP) model, a commonly employed conventional method. Furthermore, the architecture achieves lower computational complexity than other deep learning-based DPD methods, while being approximately 1.5 times as sophisticated as the GMP approach.

***Keywords**: Digital prediddtortion (DPD), generalized memory polynomial (GMP), neural network (NN), power amplifier (PA).*

Study of Electrical Characteristics and Charge Storage Behaviour of Gold Embedded Floating Gate MOS Structure

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Abstract: Non-volatile memory(NVM) devices are of great interest because of their memory capacities in the form of charge storage, scalability and retention capabilities. A Metal-Oxide Semiconductor (MOS) structure with a tunnel oxide, control oxide and a composite gate dielectric embedded with Gold (Au) nano-crystals(nc) has been studied in this paper. This work represents a theoretical analysis of leakage current in the form of field emission or the Fowler-Nordheim (F-N) tunneling current in the designed structure. The lowering of the onset voltage in the F-N tunneling current expressed the high retention capacity or low writing voltage of the NVM structure. The proposed device structure shows a considerable memory window when the voltage sweeps from -6V to +15V back and forth. Additionally, the transfer characteristics of the nanoparticles-embedded MOS transistor have been studied well in this paper. This kind of proposed NVM structure, owing to its charge storing capacity and scalability can find immense application in the field of nonvolatile memory technology.

Optimizing Si-based DG-JL-TFET Performance through Tunable Work function Engineering

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Abstract:
The optimization of silicon-based Double-Gate Junctionless Tunnel Field-Effect Transistors (DG-JL-TFETs) offers significant advancements in semiconductor technology. This research explores the impact of tunable work function (WF) engineering on improving device performance and adaptability. By adjusting the WF of the gate material, electrostatic control over the channel is modulated, enhancing subthreshold swing (SS) and reducing leakage current. Comprehensive simulations were conducted to evaluate the effects of different WF values for both gates, yielding critical device parameters: threshold voltage (V_t) of 0.4 V, on-state current (I_{on}) of 5.7 μA, and cut-off frequencies (f_t) and (f_{max})of 156 GHz and 302 GHz, respectively. The findings indicate that strategic WF tuning can significantly increase the on-off current ratio and reduce power consumption, making DG-JL-TFETs highly suitable for low-power, high-performance applications. This optimization approach enhances the potential of DG-JL-TFETs in next-generation semiconductor devices, positioning them as promising candidates for future low-power electronics and high-frequency applications.

***Keywords**: Tunable work function; On-state Current; Unit gain Current cut-off frequency and Maximum Oscillation frequency.*

Design and implementation of low power circuits based on 5nm double gate MOSFET technology using different materials

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Abstract: This paper presents a comprehensive investigation of 5nm double gate MOSFETs (DG MOSFETs) circuits using different substrate semiconductor materials for low-power devices. A comparative analysis of characteristics of SiGe, InGaAs and GaN as substrate materials is performed. The study reveals that InGaAs offers superior performance due to its higher electron mobility, lower threshold voltage and thermal stability than other materials studied here for low-power applications. The electrical properties of DG MOSFETs on these substrates have been investigated by calculating key parameters such as threshold voltages (Vth), Ion and Ioff currents. The results show that InGaAs-based DG MOSFETs exhibit superior performance with threshold voltage, improved leakage current and Ion/Ioff ratio compared to other substrate materials. Additionally, a lower threshold voltage has been observed for InGaAs-based devices, indicating reduced power consumption. These findings demonstrate the potential of InGaAs as a preferred substrate material for low-power, high-performance DG MOSFET devices. Double gate MOSFET circuits are designed using InGaAs and power dissipation is calculated. The results show a significant reduction in power consumption and improved circuit performance compared to traditional Si-based devices. This research demonstrates the potential of InGaAs-based DG MOSFETs for low-power electronic devices, enabling the development of energy-efficient circuits for various applications.

Keywords*: double gate MOSFET, low Power, power dissipation, InGaAs, SiGe, GaN*

Comparative Analysis of Electrical Parameters for High Electron Mobility Transistors

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Abstract: The HEMT devices are explored extensively by different research groups in the last decade for analog/RF applications due to their inherent significant features such as high breakdown voltage, electron mobility, and their potential to operate at high frequency. The surface-potential, 2-DEG density, gate capacitance for HEMT is calculated in the present work. The surface potential is compared for different channel potential. Further, 2-DEG density is compared for different channel potential. The gate-capacitance are compared for gate voltage from -4 V to 4 V. The computations of g_{m2} and g_{m3} are also performed for different values of gate voltage.

Keywords*: HEMT, electric potential, channel potential, surface potential.*

Design and implementation of CML frequency divider circuit using 90nm Technology

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Abstract: The objective of this paper is to design a current mode logic (CML) frequency divider in CMOS 90nm technology. The fundamental idea behind this paper is to understand the basic operation of CML circuit using a T flip-flop-based frequency divider. Combining Current Mode Logic (CML) with T flip-flops creates a powerful solution for building high-speed frequency dividers. This introduces a frequency divider circuit that takes advantage of CML technology and the unique properties of T flip-flops to split frequencies efficiently. T flip-flops work by toggling their state with every clock pulse, effectively cutting the input frequency in half with each flip-flop stage. A frequency divider is needed in the PLL loop to allow the use of a low-frequency reference clock that is typically provided by a highly accurate off-chip crystal oscillator. Using CML in this design boosts the circuit's performance, making it faster and more energy-efficient than traditional logic circuits. CML's current steering and differential signaling help to achieve higher speeds and better handle noise, less power, less area, and low voltage making it ideal for demanding digital applications. This abstract covers how the CML-based frequency divider works, and its benefits for high-speed tasks.

Keywords*: Current mode logic (CML), PLL,CMOS,T-Flip Flops*

Kernel Based Fuzzy Simulation Model for Early Detection of Cancer to Avoid Metastasis

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Abstract: In this paper, novel cancer detection method using Kernel Based Fuzzy Simulation Model (KBFSM) represented with enhanced accuracy of 12%, considering MRI based breast cancer images. Developed framework, as suggested in this paper, Effectiveness and superiority of the suggested approach are proven by thorough testing on a variety of datasets and thorough assessment metrics, highlighting its capacity to produce accurate and nuanced segmentation results. Fuzzification and defuzzification of images using Fuzzy C means algorithm, speaks in favor of the proposed analysis, as tested over several dataset, owing to minute pixel intensity modification when associated with malignant tissues. Result is supported by histogram analysis, which paves the way of future research in the field of lung cancer using the same technique.

Keywords: *Image segmentation; Breast cancer; Fuzzy simulation; Metastasis; Defuzzification*