Monday, October 16, 2023
7:00 - 7:50 Breakfast
7:50 - 8:00 Opening Remarks/8:00 - 9:00 Keynote I
Chair: Stefano Griewot-Talocia, Politecnico di Torino
- SURFACE power delivery, the future of High-Performance Computing
  Jose A. Cobos
  Universidad Politecnica de Madrid
9:00 - 10:00 Session M-II: High Speed System Design Chairs:
  Kernal Hyun, Intel
  Junyang Tang, IBM
- M-II.1. Development of High-speed and Large-capacity 3D MRMHM: First-ever MRMHM with Dual PIMCs
  Jonghyun Kim, Jinseong Yun, Kyung Lee, Rangguo Ji, Hyang Youn, Sanghyuk Yoon, Young-Ho Kim.
  Sungchan Rho
  Samsung Electronics
  Yutaka Uematsu
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- M-II.3. PCB-level Jitter Sensitivity Measurement and Hierarchically PadN-z Based PJM Estimation for PRR on Gaud SDD
  Youngsa Keum, Jinwook Song, Seokwoo Hong, Hyunwoo Kim, Chomma Jang, Sungwoo Lim.
  Sungchan Rho, Jinan Lee, Jonghee Jeong, Kyungsuk Kim, Jonggyu Park
  Samsung Electronics
10:00 - 10:20 Coffee Break
10:20 - 12:20: Chairs: Jose Hejase, Nvida
  Session M-II. Special Session on Advances in High-speed Interconnect Signal Integrity Design, Analysis and Measurements
  Jinwook Song, Samsung Electronics
- M-II.1. Analyses of Vias-In-Par Plated Over (VPoP) and Dimpole in Fanout Routing High-Density Interconnects
  Yunyan Zhang, Junyan Tang, Xiaomian Duan, Siqian Duan, Pavel Key Papadis, Mathis Boher.
  Sungchan Rho, Chansup Daniel Cho, Doshu Kim, Doshu Kim.
- M-II.2. A New Perspective on Quasi-TEM Behavior in Microstrip Transmission Lines (Student Competition)
  Adaya Rao, Eric Bogatin, Melinda Piket-May, Mohammad Hadi
  University of Colorado, Boulder
- M-II.3. Interconnect Modelling Sensitivity Studies for High Signaling Data Rates
  Adevalde Okunde, Jose Hejase
  Nvida
- M-II.4. Package Technology Enabling for 248 Gbps Electrical Signaling
  Kunlun Gu, Daye Ye, Cenli Guo, Xizhe Qian Quan
  Intel
- M-II.5. Analysis of Differential Signal Integrity Approaches within a PCB Via Field for Crosstalk Mitigation
  Siqian Duan, Yuechen Wang, Junyan Tang, Xiaobiao Yang, Yunyan Zhang, Pavel P. Paladhi.
  Mathis Boher, Joshua C. Myers, Sungchan Rho and Daniel M. Droz

Tuesday, October 17, 2023
7:00 - 8:00 Breakfast
8:00 - 9:00 Keynote II/Chairs:
  Swagato Chakraborty, Siemens EDA
- T-II.1. Recent Progress on Signal Integrity of Practical Chiplet by the PPEM Modeling on Analysis of\n  Hanhui Ma, Tizum Tao, 1 Quanxin Chen 2 Da Li 1, Jose Schiff-Ante 1, Andreas Campell"1, "From P"1 li, "1 2
  Keyngh University
- T-II.2. University of Illinois at Urbana-Champaign
  Yuhang Dou 1, Yang Jiang 2, Ke-Li Wu 1
  1NVIDIA
- T-II.4. STAR
  The Chinese University of Hong Kong
- T-II.5. Simple Extraction of the First Resonant Frequency via Integral Equation Method
  Ricardo Tonches, Francesco Lucchini
  University of Padova
10:00 - 10:20 Coffee Break
10:20 - 12:20: Chairs: Stefano Griewot-Talocia, Politecnico di Torino
  Session T-II: Special Session on Model Order Reduction
  Jose Hejase, Nvida
- T-II.1. Wideband Complex Vertex Fitting for Modeling Time Delay Variations in Passive Photonic Filters
  Thilo Ulrich,Dirk Deschevr, Win Bogarts, Tom Duane
  Ghent University
- T-II.2. Improving Accuracy of Rational Macromodels under Realistic Loading Conditions (Student Competition)
  Antonio Carlucci, Tommaso Bradda, Stefano Griewot-Talocia
  Politecnico di Torino
  Elia Mattucci 1, Lihong Fung 2, Peter Bense 2, Daniele Romano 3, Giuilio Antonini 1
  2Istituto Italiano di Tecnologia, Pisa, 3University of Padua
- T-II.4. Max Planck Institute for Dynamics of Complex Technical Systems
  1University of L'Aquila
- T-II.5. Balancing-Based Model Reduction for Fast Power Integrity Verification (Student Competition)
  Antonio Carlucci 1, Stefan Griewot-Talocia 1, Scott Mongrue 2, Sid Kulasekarar 2, Kadaleh Rashidkhah 1
  Politecnico di Torino
- T-II.7. IBM
- T-II.8. Max Planck Institute for Dynamics of Complex Technical Systems
  1University of L'Aquila
12:00 - Sponsor Demo: Siemens
12:10 - 1:30 Lunch Break and TPC Meeting
1:30 - 2:50 Chairs: Session M-III: Special Session on Electromagnetics
  Vladimir Omatovskii, University of Manitoba
  Dinesh Vaidya, Ghost University
- M-III.1. CISP 25 Conducted Emission Simulation and Measurement Correlation of an Automotive Isolated Solid-State Relay
  Jie Chen 1, Rajan Murugan 1, John Beazley 2, Prasenaggar Kittas 1, Bryan Marshall 3, Tilen Chen 4, Alex Tiwan 2, Bibha Naya 2, Harikan Munigam 5, Joe Sivasamy 2, and Deepanjan Gope 2
  2Texas Instruments Incorporate
- M-III.2. Fast and Accurate Calculation of Mutual Inductance in the Presence of Conductive and Magnetic Media
  Dyuti Sengupta, Andreas Weisshaar
  Oregon State University
  Yuhang Dou 1, Quankun Chen 1, John Broze 1, Alex Triano
  1Texas Instruments Incorporate
- M-III.4. Quantum Computing with Industrial Spin Qubits: Scaling Challenges and the Interconnect Bottleneck
  Lester Lampert
12:30 - 1:30 Lunch Break
1:30 - 2:30 Chairs: Session T-III: Special Session on Machine Learning
  Jianjun Zhang, University of Illinois at Urbana-Champaign
- T-III.1. Fifty Years of Partial Element Equivalent Circuit (PEEC) Enhancements
  Albert Rudi
  Missouri Institute of Science and Technology
- T-III.2. Missouri Institute of Science and Technology
- T-III.3. Quantum Computing with Industrial Spin Qubits: Scaling Challenges and the Interconnect Bottleneck
  Lester Lampert
- T-III.4. IBM

Wednesday, October 18, 2023
7:00 - 8:00 Breakfast
8:00 - 9:00 Keynote III/Chairs:
  Piero Trivison, University of Trento
- W-II.1. Broadband Launch-Free Package using HDI Substrate for Radar Applications
  1Texas Instruments Incorporate
  Roni Khazaka, Bob Whitehead, Zhiling Zhou
- W-II.2. Substrate Integrated Coaxial Line Millimetrewave Components Manufactured in Standard PCB (Student Competition)
  Laura Van Messem, Arno Moorman, Olivier Catan
  Lenk Rogier, Sam Lemeny
- W-II.3. Robust and Efficient Design of On-Chip Compact Delay Units Based on Bridged Tail-Coi (Student Competition)
  Han-Ting Lin, Andris Weisshaar
  Oregon State University
- W-II.4. D-Side Flip-Chip Packaging with Wafer-Level Capacitor Bumps
  Zhibao Cao 1, Matteo Stocchi 1, Christian Wolf 2, Ken Lein 1
  1Texas Instruments Incorporate

Session W-II: Applied Machine Learning in Design and Analysis
12:20 - 2:00 Lunch Break
2:20 - 4:00 Chairs: Jose Hejase, Nvida
  Session W-II: Applied Machine Learning in Design and Analysis
  Jose Hejase, Nvida
- W-II.5. Development of High-speed and Large-capacity 3D MRMHM: First-ever MRMHM with Dual PIMCs
  Kunlun Gu, Daye Ye, Cenli Guo, Xizeh Qian Quan
  Intel
- W-II.6. Package Technology Enabling for 248 Gbps Electrical Signaling
  Kunlun Gu, Daye Ye, Cenli Guo, Xizeh Qian Quan
  Intel
- W-II.7. Analysis of Differential Signal Integrity Approaches within a PCB Via Field for Crosstalk Mitigation
  Kunlun Gu, Yuechen Wang, Junyan Tang, Xiaobiao Yang, Yunyan Zhang, Pavel P. Paladhi.
  Mathis Boher, Joshua C. Myers, Sungchan Rho and Daniel M. Droz

Session W-II: Applied Machine Learning in Design and Analysis
12:20 - 2:00 Lunch Break
2:20 - 4:00 Chairs: Jose Hejase, Nvida
  Session W-II: Applied Machine Learning in Design and Analysis
  Jose Hejase, Nvida
- W-II.8. Adapting and Training of Multi-Task Feature Learning for Partial Discharge Rejection
  Juhang Lian 1, Zhe Shui 1, Hongyan Li 2, Kai Xian 1, Yuanjun Li 2, Xiaogang Jin 2, Jinyong Hong 2, Jiwon Yoon 1, Jinyoung Kim
  Korea Advanced Institute of Science and Technology
- W-II.9. IEEE Power Group
- W-II.10. Singapore Power Group
- W-II.11. Efficient Uncertainty Quantification using Sensitivity Information in Least Squares SVM
  Karanvir S. Sidhu, Rimi Khaisaka
  McGill University
  Te-Hsin Paul 1, Paul Franxol 1, Vasimur Srinivas 2
  Mahalingum Nagaran 1, Darko Popovic 2
  1North Carolina State University
  2Qualcomm Technologies, Inc.
- W-II.13. Efficient Estimation of Power Supply Induced Jitter via Machine Learning (Student Competition)
  Ahsan Javaid 1, Ramachandran Achari 2, Jai Tripathi 2
  1Carlson University
  2Indian Institute of Technology Jodhpur
12:30 - 2:30 Lunch Break
M-V.9. A Flexible Neural Network-Based Tool for Package Second Level Interconnect Modeling
Furkan Karatoprak1, Ekin Su Sacin1, Doganay Ozser1, Ahmet C. Durgun1, Mustafa Gokce Baydogan1, Kemal Aygun1 and Tolga Memioglu1
1Middle East Technical University
2Bogcici University

M-V.10. Signal Integrity Design and Analysis of Redistribution Layer Interposer Channel with Diagonal Meshed Ground in Memory Interface of High Bandwidth Memory (Student Competition)
Jonghyun Hong, Jiwon Yoon, Hyunwoo Kim, Keeyoung Son, Seonguk Kim, Junghyun Lee, Keunwoo Kim, Joongsang Park, Seonguk Kim, Boogyo Sim, and Junghyun Kim
Korea Advanced Institute of Science and Technology (KAIST)

M-V.11. S-Parameter-Based Delay Calculations in Low-Cost Module
Robert Wenzel, Nikhita Balalari
NXP Semiconductors

M-V.12. HIGH SPEED DIGITAL SIGNALING IN PRINTED, PLANAR MICROWAVE CONNECTORS WITH MULTIPLE SIGNAL LINES (Student Competition)
Kasule Jotham, Alkim Akyurtlu, Craig Armiento
University of Massachusetts Lowell

Cagan Diyaroglu, Mohammad Taghi, Kyungjin Kim
University of Connecticut

M-V.14. Crosstalk Mitigated On-chip Interconnect Design for High-speed Network-on-Chip (NoC) of Full Wafer Scale Chip (FWSC) (Student Competition)
Jinseong Kim, Seonguk Kim, Joongsang Park, and Junghyun Kim
Korea Advanced Institute of Science and Technology (KAIST)

M-V.15. Versatile Genetic Algorithm-Bayesian Optimization (GA-BO) Bi-Level Optimization for Decompiling Capacitor Placement (Student Competition)
Hyuna Park, Haryeon Kim, Hyunwoo Kim, Joongsang Park, Seonguk Choi, Joonsang Son, Daeji Kim, Jongmin Ahn, and Joungsang Kim
Korea Advanced Institute of Science and Technology (KAIST)

M-V.16. Automated Generation and Correlation of Physics-Based Via Models with Full-Wave Simulation for an SI/PI Database
Til Hillebrecht1, Johannes Allen2, Torsten Reuschel2, Christian Schuster2
1Hamburg University of Technology (TUHH)
2University of New Brunswick