Menu

32nd Conference on Electrical Performance of Electronic Packages and Systems, Milpitas, CA - October 15-18 2023 - Final Program

Return

Final Program

Sunday, October 15, 2023

8:30 - 5:20 TutorialsChair:
Wendem Beyene, *Meta*

- **Tutorial I - Metalearning Advances in Machine Learning for Modeling of Emerging FET Devices and Interconnects below 10nm Technology Nodes (8:30-9:30)**
  Sourajeet Roy, Avirup Dasgupta
  IIT Roorkee
- **Tutorial II - Signal and Power Integrity Design for Highperformance SSD PCI Express Channel (9:30-10:30)**
  Jinwook Song
  Samsung

10:30 - 10:50 Coffee Break

- **Tutorial III - Floorplanning Methods for Die/PKG Co-Design (10:50 - 11:50)**
  Vaishnav Srinivas[1], Paul Franzon[2]
  [1]*Qualcomm*, [2]*North Caroline State University*
- **Tutorial IV - Winning the Lottery with Power Integrity Simulation ... What are the Odds (11:50 - 12:20)**
  Heidi Barnes
  Keysight

12:20 - 2:00 Lunch Break

- **Tutorial V - EM simulations of interconnects with layered media integral equations and fast algorithms (2:00 - 3:00)**
  Vladimir Ohkmatovski
  University of Manitoba
- **Tutorial VI - Design and Analysis of Hybrid DC-DC converters for Mobile Applications (3:00 - 4:00)**
  Abdullah Abdulslam
  Meta Platforms

4:00 - 4:20 Coffee Break

- **Tutorial VII - Introduction to Universal Chiplet Interconnect Express (4:20 - 5:20)**
  Joe (Zuoguo) Wu
  Intel

Monday, October 16, 2023

7:00 - 7:50 Breakfast

7:50 - 8:00 Opening Remarks8:00 - 9:00 Keynote I Chair:
Stefano Grivet-Talocia, *Politecnico di Torino*

- **SURFACE power delivery, the future of High-Performance Computing**
  Jose A. Cobos
  Universidad Politécnica de Madrid

9:00 - 10:00 Session M-I: High Speed System Design Chairs:
Kemal Aygun, *Intel*
Junyan Tang, *IBM*

- **M-I.1. Development of High-speed and Large-capacity 2U MRDIMM: First-ever MRDIMM with Dual PMICs**
  Jonghoon J. Kim, Jinseong Yun, Kyudong Lee, Rakjoo Sung, Jihye Yang, Sanghyuk Yoon, Young-Ho Lee, KyoungSuk Kim, Jeonghyeon Cho, Hoyoung Song
  Samsung Electronics
- **M-I.2. Active mode-conversion-noise Suppressor with Individual Power-supply Control for Automotive Power-over-data-line Communication**
  Yutaka Uematsu
  Hitachi Ltd
- **M-I.3. PCB-level Jitter Sensitivity Measurement and Hierarchical PDN-Z based PSIJ Estimation for PCIe Gen5 SSD**
  Youngjun Ko, Jinwook Song, Seokwoo Hong, Hyunwoo Kim, Chorom Jang, Sungwoo Jin, Sungwon Roh, Jinan Lee, Jonghee Jeong, Kyungsuk Kim, Jonggyu Park
  Samsung Electronics

10:00 - 10:20 Coffee Break

10:20 - 12:00 Chairs:
Jose Hejase, *Nvidia*
Session M-II: Special Session on Advances in High Speed Interconnect Signal Integrity Design, Analysis and Measurements
Jinwook Song, *Samsung Electronics*

- **M-II.1. Analyses of Via-In-Pad Plated Over (VIPPO) and Dogbone in Fanout Routing High-Density Interconnects**
  Yanyan Zhang, Junyan Tang, Xiaomin Duan, Srijan Datta, Pavel Roy Paladhi, Mahesh Bohra, Sungjun Chun, Daniel Dreps
  IBM
- **M-II.2. A New Perspective on Quasi-TEM Behavior in Microstrip Transmission Lines (Student Competition)**
  Aditya Rao, Eric Bogatin, Melinda Piket-May, Mohammed Hadi
  University of Colorado, Boulder
- **M-II.3. Interconnect Modelling Sensitivity Studies for High Signaling Data Rates**
  Adewale Oladeinde, Jose Hejase
  Nvidia
- **M-II.4. Package Technology Enabling for 224 Gbps Electrical Signaling**
  Kemal Aygun, Duye Ye, Cemil Geyik, Zhiguo Qian
  Intel
- **M-II.5. Analysis of Differential Stripline Routing Approaches within a PCB Via Field for Crosstalk Mitigation**
  Srijan Datta, Yuechen Wang, Junyan Tang, Xianbo Yang, Yanyan Zhang, Pavel R. Paladhi, Mahesh Bohra, Joshua C. Myers, Sungjun Chun and Daniel M. Dreps
  IBM

12:00 - 12:10 Sponsor Demo: Siemens

12:10 - 1:30 Lunch Break and TPC Meeting

1:30 - 2:50 Chairs:
Session M-III: Special Session on Electromagnetics
Vladimir Okhmatovski, *University of Manitoba*
Dries Vande Ginste, *Ghent University*

- **M-III.1. CISPR 25 Conducted Emission Simulation and Measurement Correlation of an Automotive Isolated Solid-State Relay**
  Jie Chen[1], Rajen Murugan[1], John Broze[1], Premsagar Kittur[1], Bryan Marshall[1], Tilden Chen[1], Alex Triano[1], Bibhu Nayak[2], Harikiran Muniganti [2], Joe Sivaswamy[2], and Dipanjan Gope[2]
  [1]*Texas Instruments Incorporated*

  [2]*Simyog Technology, Pvt., Ltd*
- **M-III.2. Fast and Accurate Calculation of Mutual Inductance in the Presence of Conductive and Magnetic Media**
  Dyuti Sengupta, Andreas Weisshaar
  Oregon State University
- **M-III.3. Stochastic Modeling of Microcontroller Emission**

Tuesday, October 17, 2023

7:00 - 8:00 Breakfast

8:00 - 9:00 Keynote IIChair:
Swagato Chakraborty, *Siemens EDA*

- **Fifty Years of Partial Element Equivalent Circuit (PEEC) Enhancements**
  Albert Ruehli
  Missouri Institute of Science and Technology

9:00 - 10:00 Chairs:
Session T-I: Advancements in Partial Element Equivalent Circuit
Albert Ruehli, *Missouri Institute of Science and Technology*
Swagato Chakraborty *Siemens EDA*

- **T-I.1. Recent Progress on Signal Integrity Modeling of Neuromorphic Chips by the PEEC Method**
  Hanzhi Ma[1], Tuomin Tao [1], Quankun Chen [1], Da Li [1], Jose Schutt-Aine[2], Andreas Cangellaris[3], Er-Ping Li [1]
  [1]*Zhejiang University*

  [2]*University of Illinois at Urbana-Champaign*

  [3]*NEOM University*
- **T-I.2. Physics-Intuitive Micro-Modeling Circuits (MMC) Inspired by PEEC Models for Emerging Electromagnetic Problems**
  Yuhang Dou[1], Yang Jiang[2], Ke-Li Wu[3]
  [1]*Xiamen University*

  [2]*A*STAR*

  [3]*The Chinese University of Hong Kong*
- **T-I.3. Simple Extraction of the First Resonant Frequency via Integral Equation Method**
  Riccardo Torchio, Francesco Lucchini
  Univeristy of Padova

10:00 - 10:20 Coffee Break

10:20 - 12:20 Chairs:
Stefano Grivet-Talocia, *Politecnico di Torino*
Session T-II: Special Session on Model Order Reduction
Sourajeet Roy, *IIT Roorkee*

- **T-II.1. Wideband Complex Vector Fitting for Modeling Time Delay Variations in Passive Photonic Filters**
  Thijs Ullrick, Dirk Deschrijver, Wim Bogaerts, Tom Dhaene
  Ghent University
- **T-II.2. Improving Accuracy of Rational Macromodels under Realistic Loading Conditions (Student Competition)**
  Antonio Carlucci, Tommaso Bradde, Stefano Grivet-Talocia
  Politecnico di Torino
- **T-II.3. Fast Frequency-Domain Analysis for Parametric Electromagnetic Models Using Deep Learning**
  Elia Mattucci[1], Lihong Feng[2], Peter Benner[2], Daniele Romano[3], Giulio Antonini[3]
  [1]*Rete Ferroviaria Italiana S.p.A.*

  [2]*Max Planck Institute for Dynamics of Complex Technical Systems*

  [3]*University of L'Aquila*
- **T-II.4. Balancing-Based Model Reduction for Fast Power Integrity Verification (Student Competition)**
  Antonio Carlucci[1], Stefano Grivet-Talocia[1], Scott Mongrain[2], Sid Kulasekaran[2], Kaladhar Radhakrishnan[2]
  [1]*Politecnico di Torino*

  [2]*Intel Corporation*
- **T-II.5. Causal or Not? A Definite Answer for Frequency-Response Data**
  Andria Lemus, A. Ege Engin
  San Diego State University
- **T-II.6. Lossy Transmission Line Model Based on the Generalized Method of Characteristics (Student Competition)**
  Mark Keran, Anestis Dounavis
  Western University

12:20 - 12:30 Sponsor Demo: Cadence

12:30 - 2:00 Lunch Break and EDMS Meeting

2:00 - 3:20 Chair:
Session T-III: Special Session on Machine Learning Xu Chen, *University of Illinois at Urbana-Champaign*
Lijun Jiang, *Missouri Institute of Science and Technology*

Wednesday, October 18, 2023

7:00 - 8:00 Breakfast

8:00 - 9:00 Keynote IIIChair:
Piero Triverio, *University of Toronto*

- **Quantum Computing with Industrial Spin Qubits: Scaling Challenges and the Interconnect Bottleneck**
  Lester Lampert
  Intel

9:00 - 10:20 Session W-I: RF and Advanced Packaging Chairs:
Piero Triverio, *University of Toronto*
Giacomo Bianconi, *Siemens EDA*

- **W-I.1. Broadband Launcher-in-Package using HDI Substrate for Radar Applications**
  Nikita Mahjabeen, Robert Wenzel, Tingdong Zhou
  NXP Semiconductors
- **W-I.2. Substrate Integrated Coaxial Line Millimeterwave Components Manufactured in Standard PCB (Student Competition)**
  Laura Van Messem, Arno Moerman, Olivier Caytan, Hendrik Rogier, Sam Lemey
  Ghent University
- **W-I.3. Robust and Efficient Design of On-Chip Compact Delay Units Based on Bridged T-Coil (Student Competition)**
  Han-Ting Lin, Andreas Weisshaar
  Oregon State University
- **W-I.4. D-Band Flip-Chip Packaging with Wafer-Level Cu-pillar Bumps**
  Zhibo Cao[1], Matteo Stocchi[2], Christian Wipf[1], Jens Lehmann[1], Lei Li[3], Selin Tolunay Wipf[1], Matthias Wietstruck[1], Corrado Carta[1,4], Mehmet Kaynak[5]
  [1]*IHP Microelectronics*
  [2]*Keysight Technologies*
  [3]*Cornell University*
  [4]*Technische Universitat Berlin*
  [5]*Texas Instruments*

10:20 - 10:40 Coffee Break

10:40 - 12:20 Chairs:
Vaishnav Srinivas, *Qualcomm*
Session W-II: Applied Machine Learning in Design and Analysis of Interconnects
Dan Jiao, *Purdue University*

- **W-II.1. Adaptive Gramian-Angular-Field Segmentation Integration Based Generative Adversarial Network (AGSI-GAN) for Eye Diagram Estimation of High Bandwidth Memory (HBM) Interposer (Student Competition)**
  Junghyun Lee, Seonguk Choi, Keeyoung Son, Joonsang Park, Hyunwoo Kim, Keunwoo Kim, Taein Shin, Boogyo Sim, Jonghyun Hong, Jiwon Yoon, Juneyoung Kim, Joungho Kim
  Korea Advanced Institute of Science and Technology (KAIST)
- **W-II.2. Knowledge Distillation and Multi-task Feature Learning for Partial Discharge Recognition**
  Jinsheng Ji[1], Zhou Shu[1], Hongqun Li[2], Kai Xian Lai[2], Yuanjin Zheng[1], Xudong Jiang[1]
  [1]*Nanyang Technological University*
  [2]*Singapore Power Group*
- **W-II.3. Efficient Uncertainty Quantification using Sensitivity Information in Least Squares SVM**
  Karanvir S. Sidhu, Roni Khazaka
  McGill University
- **W-II.4. System Aware Floorplanning for Chip-Package Co-design**
  Tse-Han Pan[1], Paul Franzon[1], Vaishnav Srinivas[2], Mahalingam Nagarajan[2], Darko Popovic[2]
  [1]*North Carolina State University*
  [2]*Qualcomm Technologies, Inc.*
- **W-II.5. Efficient Estimation of Power Supply Induced Jitter via Machine Learning (Student Competition)**
  Ahsan Javaid[1], Ramachandra Achar[1], Jai Tripathi[2]
  [1]*Carleton University*
  [2]*Indian Institute of Technology Jodhpur*

12:20 - 12:40 Awards and Conference Wrap-up

12:45 - 2:30 Lunch Break

Aishwarya Gavai[1,3], Jan Hansen[2], Vivek Dhoot[3] and Dipanjan Gope[1,4]
[1]*Indian Institute of Science*

[2]*Institute of Electronics, Inffeldgasse 12/I, A-8010 Graz, Austria*

[3]*Mercedes Benz Research and Development India*

[4]*Simyog Technology Pvt. Ltd.*

- **M-III.4. Analysis of Electrostatically Induced Interconnect Structures in Single-Layer Graphene via a Conservative First-Principles Modeling Technique (Student Competition)**
  Emile Vanderstraeten, Dries Vande Ginste
  Ghent University

2:50 - 3:10 Coffee Break

3:10 - 4:50 Chairs:
Session M-IV: Special Session on EDMS Packaging Benchmark
Heidi Barnes, *Keysight*
Xu Chen, *University of Illinois at Urbana-Champaign*

- **M-IV.1. Fast Electromagnetic Analysis of Multiscale Interconnect Networks using MultiAIM (Student Competition)**
  Yongzhong Li, Damian Marek, Piero Triverio
  University of Toronto
- **M-IV.2. Full Wave IBM Plasma Substrate Benchmark By Cadence Clarity**
  Simian Sun[1], Frank Zavosh[1], Zhiping Yang[2], Qin Liu[1], Suomin Cui[1], and Lijun Jiang[2,3]
  [1]*Cadence Design Systems, Inc.*

  [2]*Missouri S&T EMC Laboratory*

  [3]*The Chinese University of Hong Kong*

- **M-IV.3. Full-Wave Analysis of Interconnects in Finite Substrates with Layered Media Formulation of SVS-EFIE for 3D Composite Metal-Dielectric Structures**
  Alireza Niazi, Shucheng Zheng, Chris Nguyen, Vladimir Okhmatovski
  University of Manitoba
- **M-IV.4. Efficient Boundary Element Methodology for Analyzing Interconnects in Multilayered PCBs**
  Swagato Chakraborty, Giacomo Bianconi, Daniel de Araujo, James Pingenot
  Siemens EDA
- **M-IV.5. Integral Equation-Based Solver for the Simulation of Integrated Circuit Packages**
  Hans Schreckenbach, Santosh Janaki Raman, Andre Fecteau, Nima Chamanara, David Abraham, Randy Yee, Jonatan Aronsson
  CEMWorks, Inc.

4:50 - 5:00 Sponsor Demo: Texas Instruments

5:00 - 6:30 Sponsor Booths

5:00 - 6:30 Session M-V: Poster PresentationsChairs:
Andrew Page, *IBM*

- **M-V.1. A Comprehensive Methodology for Optimizing Power Integrity of High-Performance IC Packages**
  Wei Liu, Guang Chen, Qian Ding, Jenny Xiaohong Jiang
  Intel Corporation
- **M-V.2. Quantification of Delay and Skew Uncertainty due to Fiber Weave Effect in PCB Interconnects**
  Alex Manukovsky[1], Yuriy Shlepnev[2], Shimon Mordooch[1]
  [1]*Intel*

  [2]*Simberian Inc.*

- **M-V.3. Signal/Power Integrity Co-Simulation of Die-to-Die Interface Customized for Augmented Reality**
  Ashkan Hashemi, Koichi Yamaguchi, Bardia Bozorgzadeh, Ling Jiang, Harsha Manjunath, Mahmoud Reza Ahmadi, and Wendemgegnehu Beyene
  Meta Platforms Inc., Reality Labs
- **M-V.4. Signal and Power Integrity Design of Advanced Interface Bus (AIB) for FPGA Packages**
  Brian Wang, Guang Chen, Loke Yip Foo
  Intel Corporation
- **M-V.5. On the Phase Estimation Amplitudes in the Quantum Matrix Equation Solver**
  Xinbo Li[1], Christopher Phillips[2], Ian Jeffrey[1], Vladimir Okhmatovski[1]
  [1]*University of Manitoba*

  [2]*University of Waterloo*

- **M-V.6. Contact Resistance of 3D-Printed Interconnects to Thin-Film Metals for Advanced Packaging**
  Jacob Dawes, Alyssa Estenson, Matthew Johnston
  Oregon State University
- **M-V.7. Broadband RF Interconnects in a Multi-Layer Advanced Packaging with Si Interposer (Student Competition)**
  Sofia Mvokany, Jack Molles
  University of Colorado Boulder
- **M-V.8. Method of Exploring HVM Process Corner Cases for Loss and Impedance in High Speed Designs (Student Competition)**

- **T-III.1. Prior Knowledge Accelerated Transfer Learning (PKI-TL) for Machine Learning Assisted Uncertainty Quantification of MLGNR Interconnect Networks**
  Sourajeet Roy, Asha Kumari Jakhar, Surila Guglani, Avirup Dasgupta
  IIT Roorkee
- **T-III.2. Generative Multi-Physics Models for System Power and Thermal Analysis Using Conditional Generative Adversarial Networks**
  Priyank Kashyap[1], Chris Cheng[1], Yongjin Choi[1], Paul Franzon[2]
  [1]*Hewlett Packard Enterprise*

  [2]*North Carolina State University*

- **T-III.3. Batch Training of Gaussian Process for Up-sampling Problems in S-Parameter Predictions (Student Competition)**
  Yiliang Guo[1], Xingchen Li[1], Yifan Wang[1], Rahul Kumar[2], Madhavan Swaminathan[2]
  [1]*Pennsylvania State University*

  [2]*Georgia Institute of Technology*

- **T-III.4. Machine-Learning-Based Constrained Optimization of a Test Coupon Launch Using Inverse Modeling**
  Andrew Page, Xu Chen
  University of Illinois at Urbana-Champaign

3:20 - 3:40 Coffee Break

3:40 - 5:20 Session T-IV: Package Design and Analysis Chairs:
Yaping Zhou, *Nvidia*
Andreas Weisshaar, *Oregon State University*

- **T-IV.1. Modeling and Analysis of Simultaneous Switching Noise for Full Wafer Scale Chip Core (Student Competition)**
  Hyunwoo Kim, Seonguk Choi, Joonsang Park, Haeyeon Kim, Keeyoung Son, Junghyun Lee, Jiwon Yoon, Jonghyun Hong, Boogyo Sim, Keunwoo Kim, Taein Shin, and Joungho Kim
  Korea Advanced Institute of Science and Technology (KAIST)
- **T-IV.2. Design and Analysis of Redistribution Layer Interposer Channel Considering Signal Integrity for High Bandwidth Memory Module (Student Competition)**
  Jiwon Yoon[1], Hyunwook Park[2], Hyunwoo Kim[1], Boogyo Sim[1], Jonghyun Hong[1], Seongguk Kim[1], Keeyoung Son[1], Keunwoo Kim[1], Yigyeong Kim[3], Sujin Park[3], Youngsu Kwon[3], Joungho Kim[1]
  [1]*Korea Advanced Institute of Science and Technology (KAIST)*

  [2]*Missouri University of Science and Technology (MST)*

  [3]*Electronics and Telecommunications Research Institute (ETRI)*

- **T-IV.3. Real-Time Precision Prediction of 3-D Package Thermal Maps via Image-to-Image Translation (Student Competition)**
  Michael Joseph Smith, Seunghyun Hwang,Vinicius Cabral Do Nascimento, Qiang Qiu, Cheng-Kok Koh, Ganesh Subbarayan, Dan Jiao
  Purdue University
- **T-IV.4. Design and Analysis of an Irregular-Shaped Power Distribution Network (PDN) for High Bandwidth Memory (HBM) Interposer (Student Competition)**
  Joonsang Park[1], Seongguk Kim[1], Keeyoung Son[1], Haeyeon Kim[1], Hyunwoo Kim[1], Hyunsik Kim[2], Seonguk Choi[1], Jihun Kim[1], and Joungho Kim[1]
  [1]*Korea Advanced Institute of Science and Technology (KAIST)*

  [2]*SK Hynix Inc.*

- **T-IV.5. HBM3 PPA Performance Evaluation by TSV Model with Micro-Bump and Hybrid Bonding (Student Competition)**
  Li-Hsin Huang, Yu-Ying Cheng, Tzong-Lin Wu
  National Taiwan University

5:20 - 5:30 Sponsor Demo: Xpeedic

7:00 - 10:00 Dinner Banquet

Hyunsu Chae[1], David Z. Pan[1], Adam Klivans[1], Bhyrav Mutnury[2], Douglas Winterberg[2], Douglas E. Wallace[2], Arun Chada[2]

[1]*University of Texas at Austin*

[2]*Dell Technologies*

- **M-V.9. A Flexible Neural Network-Based Tool for Package Second Level Interconnect Modeling**
  Furkan Karatoprak[1], Ekin Su Sacin[1], Doganay Ozese[2], Ahmet C. Durgun[1], Mustafa Gokce Baydogan[2], Kemal Aygun[3],and Tolga Memioglu[3]

[1]*Middle East Technical University*

[2]*Bogazici University*

[3]*Intel Corporation*

- **M-V.10. Signal Integrity Design and Analysis of Redistribution Layer Interposer Channel with Diagonal Meshed Ground in Memory Interface of High Bandwidth Memory (Student Competition)**
  Jonghyun Hong, Jiwon Yoon, Hyunwoo Kim, Keeyoung Son, Seonguk Choi, Junghyun Lee, Keunwoo Kim, Joonsang Park, Seongguk Kim, Boogyo Sim, and Joungho Kim
  Korea Advanced Institute of Science and Technology (KAIST)
- **M-V.11. S-Parameter-Based Delay Calculations in Low-Cost Module**
  Robert Wenzel, Nikhita Baladari
  NXP Semiconductors
- **M-V.12. HIGH SPEED DIGITAL SIGNALING IN PRINTED, PLANAR MICROWAVE CONNECTORS WITH MULTIPLE SIGNAL LINES (Student Competition)**
  Kasule Jotham, Alkim Akyurtlu, Craig Armiento
  University of Massachusestts Lowell
- **M-V.13. A Computational Framework on Pinhole Damage in Ultrathin Inorganic Barriers for Flexible Electronics Encapsulation**
  Cagan Diyaroglu, Mohammad Taghi, Kyungjin Kim
  University of Connecticut
- **M-V.14. Crosstalk Mitigated On-chip Interconnect Design for High-speed Network-on-Chip (NoC) of Full Wafer Scale Chip (FWSC) (Student Competition)**
  Juneyoung Kim, Seonguk Choi, Seongguk Kim, Jihun Kim, Boogyo Sim, Junghyun Lee, Taein Shin, Hyunwoo Kim, Jonghyun Hong, Haeyeon Kim, Joonsang Park and Joungho Kim
  Korea Advanced Institute of Science and Technology (KAIST)
- **M-V.15. Versatile Genetic Algorithm-Bayesian Optimization(GA-BO) Bi-Level Optimization for Decoupling Capacitor Placement (Student Competition)**
  Hyunah Park, Haeyeon Kim, Hyunwoo Kim, Joonsang Park, Seonguk Choi, Jihun Kim, Keeyoung Son, Haeseok Suh, Taesoo Kim, Jungmin Ahn and Joungho Kim
  Korea Advanced Institute of Science and Technology (KAIST)
- **M-V.16. Automated Generation and Correlation of Physics-Based Via Models with Full-Wave Simulation for an SI/PI Database**
  Til Hillebrecht[1], Johannes Alfert[1], Torsten Reuschel[2], Christian Schuster[1]

[1]*Hamburg University of Technology (TUHH)*

[2]*University of New Brunswick*