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Two-day Hybrid Bonding Symposium

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Theme: **Enabling Hybrid Bonding Commercialization**

16-17 January 2025 **Silicon Valley** at SEMI Headquarters, Milpitas, CA USA

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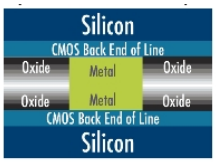

Hybrid Bonding has emerged as the technology of choice in the semiconductor industry for ultra-fine-pitch interconnection. With significant benefits for interconnect density and device performance, it will become widely adopted for a broad range of high-performance semiconductor devices in the years to come. The success of Hybrid Bonding technology for high-volume manufacturing depends critically on the process technology as well as materials and equipment. Design, performance characterization, thermal management and reliability are also important considerations to enable applications in various areas.

The following **Advance Program** lists the speakers and talks to be presented:

Speaker Name	Presentation Title
Hybrid Bonding Processes and Materials	
Guilian Gao, Adeia	Hybrid Bonding Process Technology
Anne Jourdain, imec	Deep Pitch Scaling of Wafer-to-wafer and Die-to-wafer Cu/SiCN Hybrid Bonding
Viorel Dragoi, EVG	Permanent and Temporary Wafer Bonding
Jonathan Abdilla, BESI	Die to Wafer Hybrid Bonding for Direct Copper Interconnection
Jinho An, Applied Materials	HBM Multi-Die Stacking Challenges with D2W Hybrid Bonding
Wei-Lan Chiu, ITRI	Low-Temp and Fine-Pitch Wafer-to-Wafer Hybrid Bonding using Nanotwinned and Nanocrystalline Copper for Advanced Packaging
Ilseok Son, TEL	Wafer Bonding Challenges and the Resolution of Paths
Andrea Chacko, Brewer Science	Materials for Hybrid Bonding
Masaya Jukei, Toray Industries	Investigation of Materials/Processes for Polymer-Based Hybrid Bonding
Takafumi Fukushima, Tohoku Univ	Materials and Processing for Fine-pitch CtW Hybrid Bonding
Kuan-Neng Chen, NYCU	Hybrid Bonding Innovations: Ultra-Low Temp Cu-Cu Bonding Based Passivation Technology and HRDL Platform Development for RDL Interposer Applications
Hybrid Bonding Applications	
Masaya Nagata, Sony	Advanced 3D Stacking Process with Hybrid Bonding Technology for CMOS Image Sensors
Raghav Sreenivasan, Amat	Advances in W2W Hybrid and Fusion Bonding for Device Inflections in Logic and Memory
Stephane Moreau, CEA-Leti	How Did the "Hybrid Bonding" Technology become Reliable?
Brandon Wang, Synopsys	Enabling Advanced Chiplet Based Design
Charles Woychik, NHanced Semi	Onshoring Advanced Packaging in the United States
Hybrid Bonding Metrology	
Monita Pau, Onto Innovation	Process Control for Hybrid Bonding Applications
Wenbing Yun, Sigray	Advanced 3D Imaging Technologies for 3D IC Packages
Peter Hoffrogge, PVA TePLa	Acoustic Inline Metrology for Hybrid Bonding
Julius Hållstedt, Excellum AB	Metrology for Hybrid Bonds, Microbumps and TSVs in Advanced Packaging – Are X-ray Methods Up to the Task?
Ryohei Fujita, Nagoya Univ	Non-Contact Measurement of Thermal Contact Resistance using Lock-in Thermography
Puneet Gupta, UCLA	Yield Modeling for Hybrid Bonding

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"Hybrid Bonding Overview" (6 pages) ==>

Hybrid Bonding: Pioneering Innovations and Pathways to Future Semiconductor Integration

Kuan-Neng Chen, Fellow, IEEE
Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
E-mail: knchen@nycu.edu.tw

***Abstract*—**Hybrid bonding technology has emerged as a critical enabler for three-dimensional integration circuits (3D IC) and advanced packaging for semiconductor integration, offering significant advantages in high-density interconnects and system miniaturization. By addressing the limitations of traditional interconnect approaches, hybrid bonding enables the development of next-generation circuits and systems. This review paper explores the evolution of hybrid bonding technology, beginning with its historical development, followed by recent advancements, current status, key challenges, and future potential, with particular emphasis on low temperature bonding.

Development Trajectory

Hybrid bonding is a technology used to stack two structures, such as chips, wafers, and substrates, each consisting of metal and surrounding dielectric materials. After the hybrid bonding process, the metals bond to each other, and the dielectric materials attach seamlessly as well. Hybrid bonding is considered one of the ultimate technologies in 3D IC integration. However, before the advent of hybrid bonding, Cu-to-Cu bonding was first introduced to achieve the concept of 3D IC integration. Between 1999 and 2002, Reif's group at MIT proposed a wafer-level 3D integration scheme that included the use of a handling wafer (Si carrier wafer), grinding technology, and Cu-to-Cu direct bonding, as shown in Figure 1 [1]. The Cu structures to be bonded were composed of Cu pads, similar to the Cu bumps and Cu pillars used today.

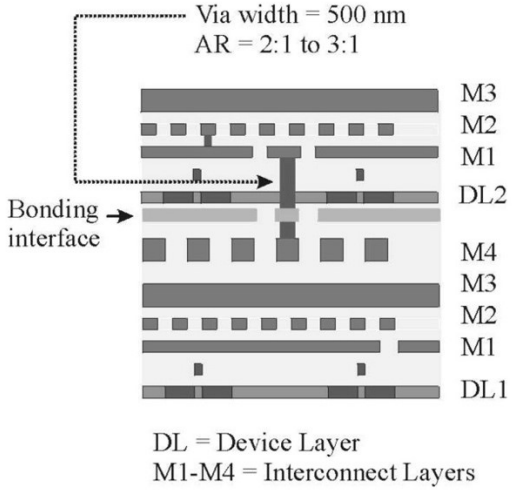

Fig. 1. An example of 3D Integration [1]

At that time, to prevent thermal damage to the devices on both wafers, the upper temperature limit for Cu-to-Cu bonding was set at 400°C, which aligns with the CMOS thermal budget. In 2001, K. N. Chen from Reif's group demonstrated that Cu-to-Cu bonding could be successfully performed at 400°C, with the original bonding interface disappearing, proving the feasibility of this technology [2]. As examples shown in Figure 2 [3], the thermal compression bonding condition was 400°C and 400 mbar for 30 min and then annealed at 400°C for 30 min in N_2 ambient atmosphere. This 400°C bonding temperature was later adopted in current hybrid bonding processes. Between 2000 and 2005, K. N. Chen published extensive research on the morphology evolution, bonding strength, bonding parameter guidelines, and electrical characteristics of Cu-to-Cu bonding [3-6]. The contact resistance of Cu-to-Cu bonded structure was found to be on the order of $1x10^{-8}$ Ω−cm^2. In 2006, K. N. Chen at IBM summarized and published comprehensive results on Cu-to-Cu bonding, covering aspects such as structure design and pattern considerations [7].

In the original Cu-to-Cu bonding scheme, there was no material surrounding the Cu, raising concerns about the reliability of the bonded Cu, such as potential corrosion and insufficient bond strength. Using underfill to fill the gap between the two substrates could be a potential solution; however, this approach is challenging due to the small gap, typically just a few micrometers, created by the height of the Cu bond pads. Moreover, this method is only feasible for chip-level bonding and is not suitable for wafer-level bonding.

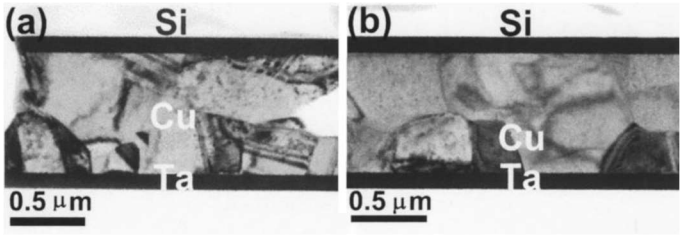

Fig. 2. Various images of the Cu-to-Cu bonded layer after 30 min bonding [3]

To address these challenges, it was intuitive to incorporate surrounding dielectric materials before Cu-to-Cu bonding. Suitable dielectric candidates include silicon dioxide (SiO_2) or polymers. The ideal bonding scenario involves

achieving simultaneous Cu-to-Cu and dielectric-to-dielectric bonding. In 2005, Gutmann and Lu's group at RPI successfully demonstrated 200mm wafer-level Cu/BCB (benzocyclobutene) thermal compression bonding using a force of 10,000 N at 250°C for 30 min, followed by ramping to 350°C for another 30 min, as shown in Figure 3 [8]. In their later 2005 publication, they named this technology "Hybrid Bonding" [9]. Both the Cu-to-Cu and BCB-to-BCB bonding interfaces exhibited excellent contact, with the contact resistance of the Cu-to-Cu bonded structure measured at approximately 1×10^{-7} Ω−cm².

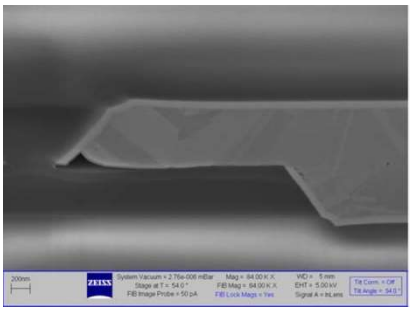

Fig. 3. The first demonstration of Cu/BCB hybrid bonding [8]

Since then, researchers have focused on developing reliable hybrid bonding techniques based on Cu/Polymer and Cu/SiO_2 formats. To leverage the compliance advantages of polymers, IBM scientists introduced a 'Lock-and-Key' hybrid bonding structure, where Cu pads/pillars on the top wafer act as the 'Lock,' while polymers (polyimide) on the bottom wafer feature larger holes, serving as the 'Key' to accommodate the Cu pads/pillars. Figure 4 shows that this 300mm wafer-level bonding scheme was successfully demonstrated, with W TSVs (tungsten through-silicon vias) revealed from the bonded and thinned top wafers [10]. Furthermore, K. N. Chen at NCTU and his former colleagues at IBM successfully demonstrated a 300mm wafer-level Cu/SiO_2 hybrid bonding based on the Lock-and-Key scheme, including reliability assessments [11-12]. As shown in Figure 5, the thermal compression bonding was performed at 400°C for 1 hour under a 10,000 N force in a 2×10^{-4} torr environment.

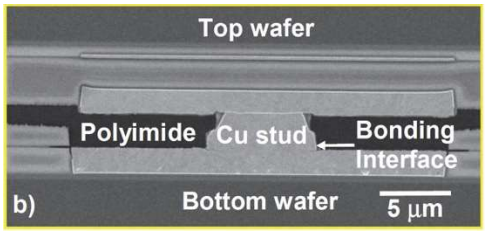

Fig. 4. Demonstration of Cu/Polymer hybrid bonding using Lock-n-Key technique [10]

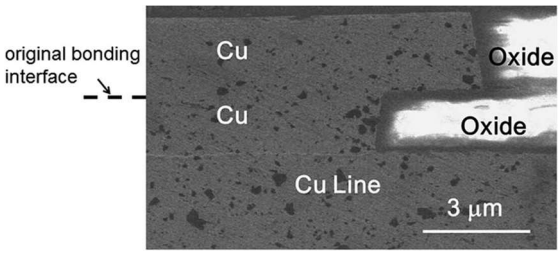

Fig. 5. Demonstration of Cu/SiO_2 hybrid bonding [12]

When considering thermal compression Cu/SiO_2 hybrid bonding, it is ideal to use the damascene Cu directly as the bonding medium. However, the Cu bond pad surface typically becomes recessed after the damascene process, up to 50 nm depending on pad dimensions. As shown in Fig. 6, the Cu is dished approximately 20 nm below the oxide level [13]. Even this small recess results in sub-optimal topography for Cu bonding, as the hard oxide surfaces make contact first, hindering Cu contact at the center of the bond pad. Therefore, developing hybrid bonding using the damascene Cu structure presents a significant challenge, which has been raised about 20 years ago.

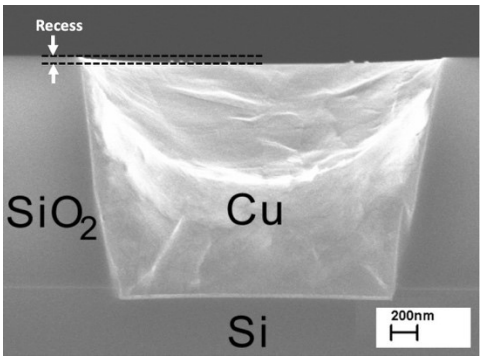

Fig. 6. SiO_2/Cu patterned surface after standard damascene process [13]

Interestingly, the unique characteristics of damascene Cu led researchers to develop another hybrid bonding technology known as 'Direct Bond Interconnect (DBI)'. Although DBI did not initially use the word of 'hybrid bonding', it captured the essential concept: Two wafers or dies with recessed Cu pads surrounded by SiO_2 were first bonded through oxide-to-oxide bonding at room temperature. During the subsequent anneal process, usually at the temperature for Cu-to-Cu bonding, e.g., 400°C, the coefficient of thermal expansion (CTE) of Cu, being much larger than that of SiO_2, caused the gap/recess/dishing of Cu to fill, resulting in the compression and bonding of the Cu pads, as illustrated in Figure 7 [14]. Notably, no bonding pressure and vacuum environment are required during the anneal for Cu-to-Cu bonding, making large batch processing feasible. Additionally, oxide-to-oxide bonding can be performed at room temperature, which is a much shorter process compared to thermal compression bonding.

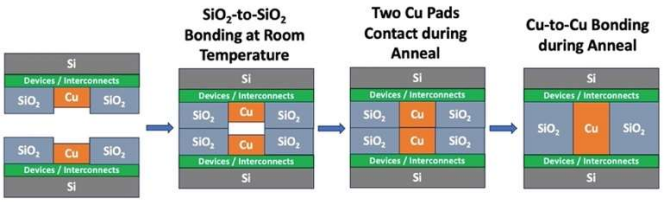

Fig. 7 Schematic diagram of hybrid bonding process based on DBI concept

Current Status

With the advantages mentioned above, DBI—which later became known as hybrid bonding—quickly captured industry-wide attention and was applied to real products. The first commercial demonstration of hybrid bonding was in CMOS image sensors (CIS). This technology enables CIS to achieve smaller pixel sizes and higher pixel densities, resulting in higher resolution sensors without increasing the overall sensor size. Additionally, hybrid bonding reduces the interconnect distance between the sensor and the logic layer by enabling finer pitch connections. This shorter distance minimizes parasitic capacitance, leading to lower power consumption and reduced noise, thereby improving signal-to-noise ratio (SNR) and image quality, particularly in low-light conditions. An example of CIS using hybrid bonding is shown in Fig. 8 [14].

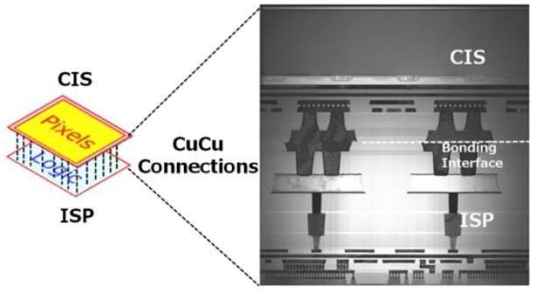

Fig. 8. Cross-sectional view of stacked CIS with hybrid bonding [14]

In contrast, logic and memory stacking applications involve more complex architectures, denser interconnections, and higher performance demands, making the hybrid bonding process more challenging and raising concerns regarding yield and cost. However, with the growing demand for high-performance computing, AI, and heterogeneous integration, traditional interconnect designs, packaging techniques, power efficiency, and logic-memory integration are approaching their limits. Logic and memory stacking using hybrid bonding provides a promising solution to address these challenges. Various platforms and applications have been proposed and are currently being explored to push the boundaries of performance and efficiency [15-17].

In the context of the DBI hybrid bonding mechanism, it is crucial to control the coplanarity of Cu bond pads, including the degree of Cu recess. This factor is closely related to the coefficient of thermal expansion (CTE) mismatch between Cu and SiO_2, as well as the bonding temperature and bonding duration, all of which contribute to achieving strong hybrid bonding results. In this regard, chemical mechanical polishing (CMP) plays a pivotal role. The single or multiple CMP process steps must effectively control the Cu pad recess within acceptable limits, both locally and across the entire chip or wafer, to ensure successful hybrid bonding in subsequent processes.

Just like other industry-wide efforts, the research team at imec has been actively working on hybrid bonding. Unlike the DBI approach, which utilizes SiO_2-to-SiO_2 bonding, imec has adopted SiCN, a well-known Cu-BEOL interconnect material, due to its exceptional smoothness (0.1 nm post-CMP) and high SiCN-to-SiCN bonding energy. Recently, E. Beyne from imec successfully demonstrated wafer-level hybrid bonding with a 400-nm pitch and Cu pad dimensions of 200 nm, as shown in Fig. 9 [18]. These fine-pitch hybrid bonding results highlight the feasibility of high-density interconnect applications through 3D IC integration for future technologies.

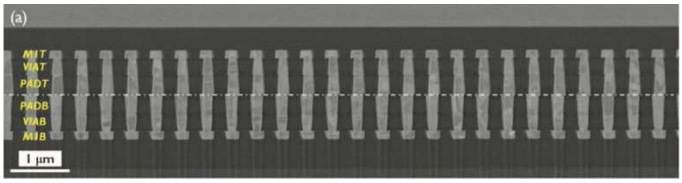

Fig. 9 400nm pitch (200nm pad diameter) hybrid bond pads interconnect [18]

Requirements and Future Trend

Several factors are key to successful hybrid bonding. Surface cleanliness, or 'particle control', and flatness are both of the most critical. For both DBI and thermal compression hybrid bonding using SiO_2, oxide-to-oxide bonding requires extremely flat and clean surfaces, as SiO_2 is a relatively hard material. Any large surface roughness and particles present will obstruct surface contact during bonding, leading to degraded bonding quality. In Cu/polymer hybrid bonding, although polymers are more forgiving of particles, excessively large particles can still complicate the bonding process and introduce reliability and stress concerns.

Since hybrid bonding is typically associated with advanced technology nodes used in high-performance computing (HPC) and high-bandwidth memory (HBM) applications, it is anticipated that multiple chip stacking with high yield and reliability will become a standard scenario. However, due to the involvement of multiple thinned chips and the increase in temperature during the hybrid bonding process, significant stress and warpage can be induced in the bonded system. This poses challenges for subsequent processing and packaging steps. Furthermore, when temperature-sensitive chips with low thermal budgets must be integrated, achieving hybrid bonding within these temperature

constraints becomes a critical challenge. One solution is to develop a low temperature hybrid bonding technology.

Furthermore, the selection of materials for hybrid bonding, particularly dielectrics, plays a crucial role in determining the appropriate bonding method, such as DBI or thermal compression bonding. In addition to SiCN's successful demonstration for hybrid bonding, various polymers have been proposed not only to meet the fundamental requirements but also to reduce bonding temperature and processing time. Moreover, alternative Cu-based materials are frequently discussed as potential replacements for conventional Cu to enable lower temperature bonding.

Finally, a sophisticated hybrid bonding facility is undoubtedly a critical factor in achieving successful bonding outcomes. In addition to a clean bonding environment, the surface condition and particle control during hybrid bonding are highly dependent on the capabilities of the bonding equipment. Moreover, alignment accuracy is essential for determining the bond pitch and size in hybrid bonding. For future logic and memory stacking applications, sub-micron misalignment has become a fundamental requirement due to the high-density interconnect designs. Therefore, the performance and precision of the hybrid bonding tool are of paramount importance.

Recent Advancements

As bonding temperature is closely related to stress, warpage, and device performance, although the 400°C bonding temperature developed by K. N. Chen in 2001 meets the CMOS thermal budget, developing lower temperature bonding technologies remains crucial. One key reason that Cu-to-Cu bonding typically requires temperatures of 300-400°C is due to the presence of Cu oxides on the surface, which hinder the interdiffusion of Cu atoms from the two substrates. A sufficiently high temperature is therefore necessary to provide the Cu atoms with enough energy to promote interdiffusion and grain growth.

K. N. Chen at NYCU (formerly NCTU) successfully demonstrated a low temperature Cu-to-Cu bonding technique using passivation metals. Cu oxide formation can be avoided by depositing a very thin (~10 nm) metal passivation layer on top of the Cu layer prior to bonding [19]. As shown in Fig. 10, when certain metals are used as passivation, during the bonding process, Cu atoms have a tendency to diffuse through the thin passivation layer and reach the bonding interface. At this point, since the Cu atoms from both substrates are oxide-free, they can easily form a bonded structure. Interestingly, this phenomenon occurs only with specific metals (e.g., Au, Ag, Pd, and Ti). Furthermore, it has been demonstrated that the diffusion path occurs through the grain boundaries of the passivation layer, and both the thickness and surface roughness of the passivation are critical factors for bonding success.

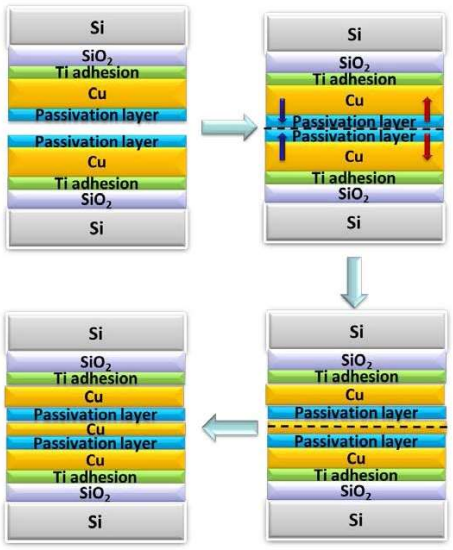

Fig. 10. Schematic of Cu-to-Cu bonding with metal passivation [19]

In the Cu-to-Cu bonding platform using metal passivation, with proper control of the passivation thickness and surface roughness, bonding temperatures as low as 40°C have been achieved, followed by post-bond annealing [20]. In general, successful Cu-to-Cu bonding using metal passivation has been demonstrated at both wafer-to-wafer and chip-to-wafer scales, with bonding temperatures below 150°C. As shown in Fig. 11, the excellent reliability characteristics and electrical performance of Cu/SiO_2 hybrid bonding using metal passivation further validate the feasibility of low-temperature bonding for future 3D IC and advanced packaging applications [21].

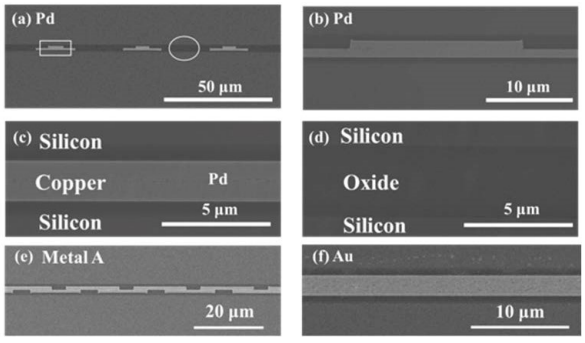

Fig. 11. Cu/SiO_2 hybrid bonding with various metal passivation [21]

CONCLUSIONS

Over the past twenty years, hybrid bonding has enabled significant advancements in three-dimensional integrated circuits (3D IC) and advanced packaging. With developments in Cu-to-Cu bonding and DBI bonding, the technology has expanded to include both wafer-to-wafer and chip-to-wafer

formats, marking a journey of continuous innovation. Hybrid bonding continues to push the boundaries of system miniaturization, performance, and efficiency. Key advancements, such as low temperature hybrid bonding and fine-pitch interconnections, have addressed many challenges and met the stringent requirements of advanced semiconductor systems. Looking ahead, the development of materials, bonding and CMP equipment, and bonding methodologies will be critical in overcoming remaining challenges, such as cost, yield, low warpage, and stress management in multi-chip stacking. By addressing these critical issues, hybrid bonding will play a significant role in shaping the next generation of high density, low power, and highly reliable semiconductor devices.

ACKNOWLEDGMENT

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