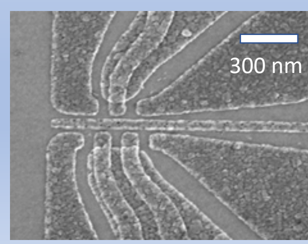
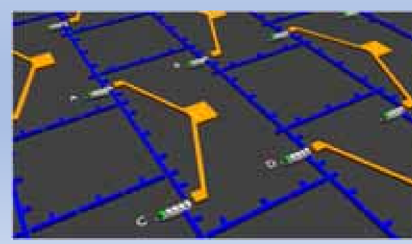
UNIVERSITY OF WATERLOO

IQC Institute for Quantum Computing

Network Architecture for Silicon Quantum Computing

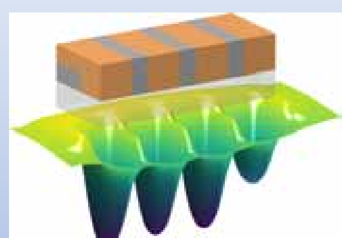
Jonathan Baugh
IEEE Santa Clara QC workshop, Oct. 24, 2023





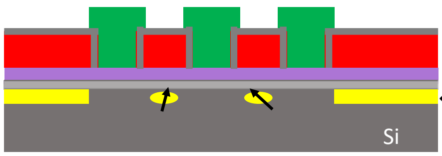
Outline

- Introduction
- Architecture
- Experimental devices
- Spin qubit simulator
- Conclusions



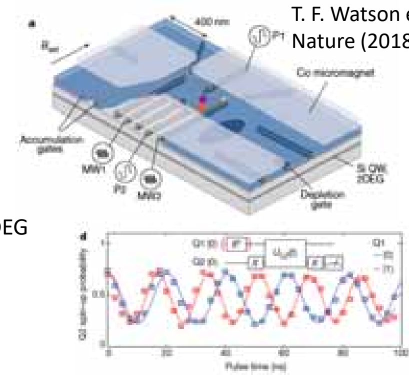
Spin qubits: Silicon MOSFET

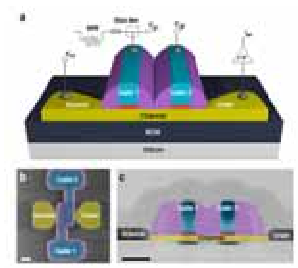
Silicon MOS quantum dots



Side view

T. F. Watson et al, Nature (2018)





CEA-LETI

- Electron and hole spins in ^{28}Si MOS (or SiGe) are promising qubits
- Leverage decades of investment/knowledge in silicon; co-integration of classical/quantum circuits; small qubit footprint
- higher T operation (~2-4 K) relative to superconducting qubits (<0.1 K)

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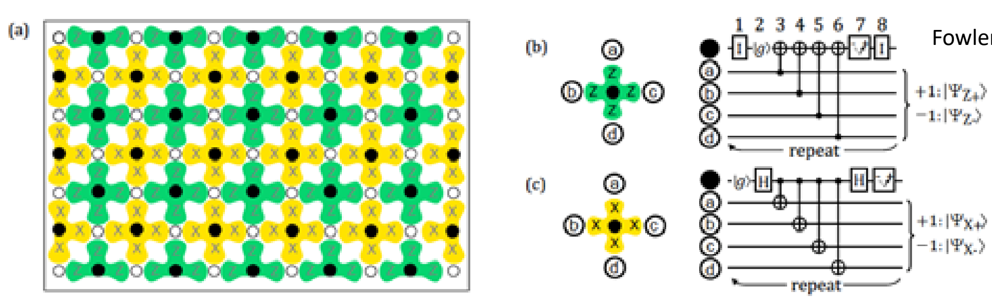
Large-scale QC: quantum error correction

Surface Codes



Fowler et al, 2012

- One of the highest error thresholds of any code (close to 1%)
- 2D topology; size adjustable to actual error rates (no concatenation)
- Requires repeated measurements and feed-forward corrections

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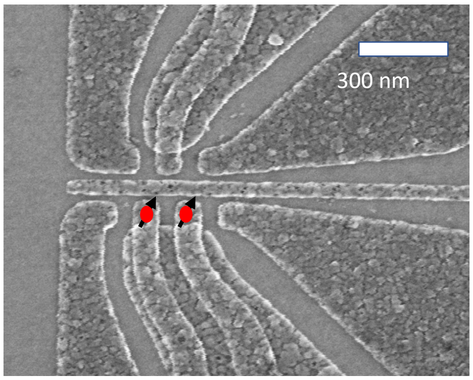
How do we scale quantum dot spin qubits?

Si MOS electron spin qubits



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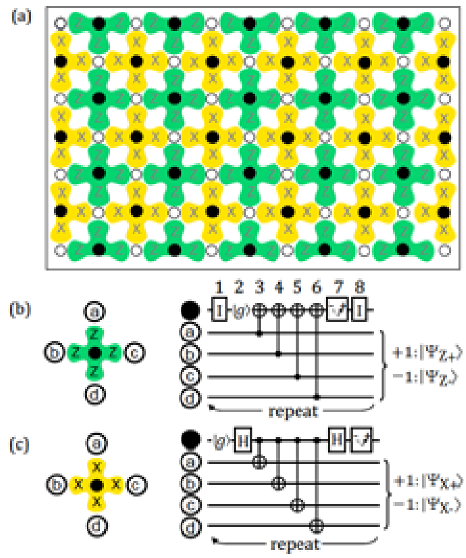

To factor a 2000 bit RSA number, Fowler et al (2012) estimate **~100 million physical qubits**, 27 hours (T_{meas} = 100 ns)

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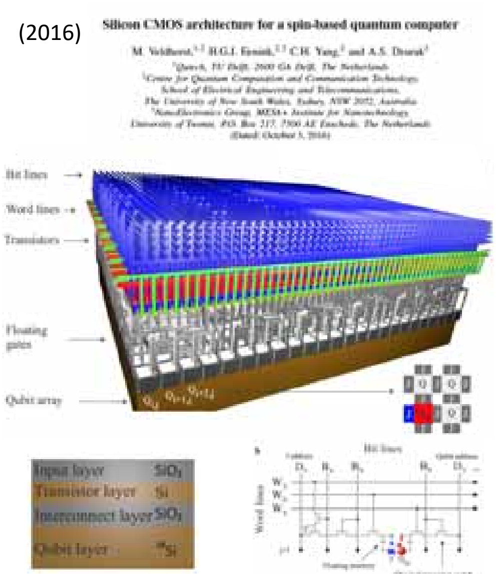
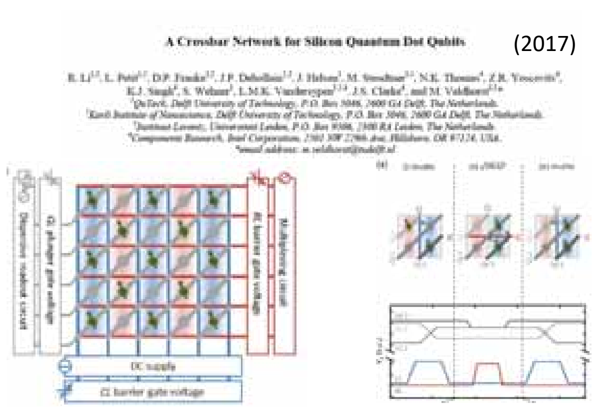
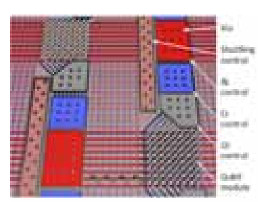
Proposed architectures

(2016)



(2017)





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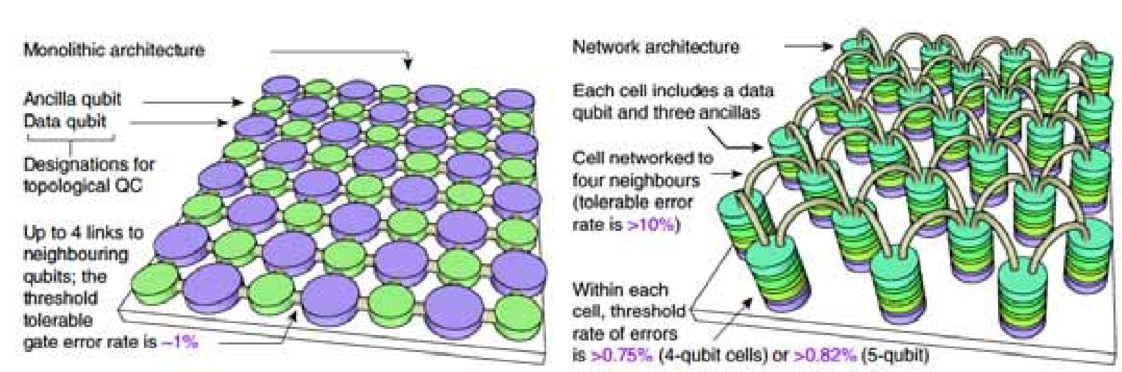
Distributed network approach



Nickerson, Li and Benjamin, *Nat. Comm.* (2013)

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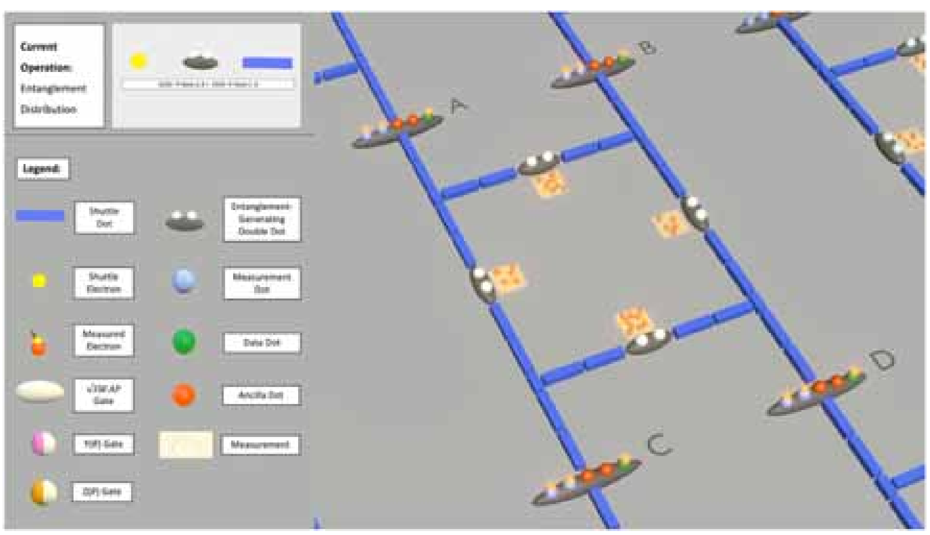
Node-network for silicon spin qubits

Institute for Quantum Computing



B. Buonacorsi et al, *Quantum Science and Technology* **4**, 025003 (2019).

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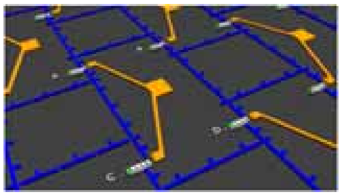
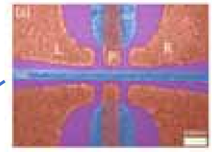
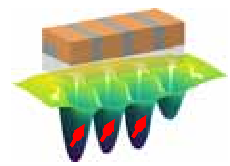
Focus areas of our research

Distributed network architecture

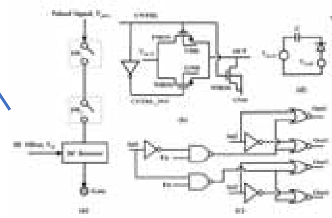




Experiment (MOS QDs)



Spin qubit simulator
(Python based)



Scalable control circuits &
cryo-CMOS

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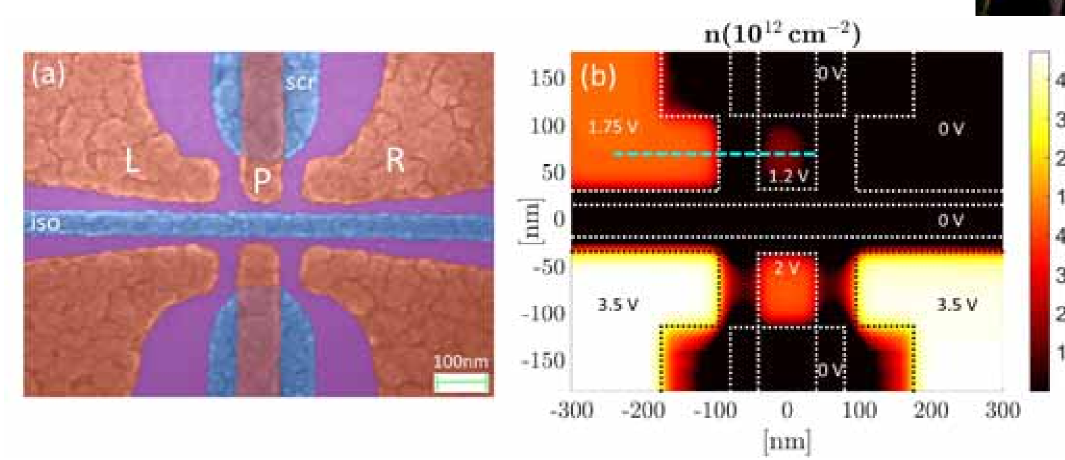
Experiment: MOS dots



E. B. Ramirez et al, “Few-electrode design for silicon MOS quantum dots”, *Semicond. Sci. Technol.* **35** 015002 (2020)

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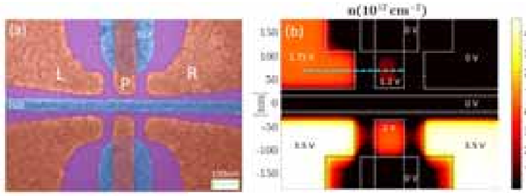
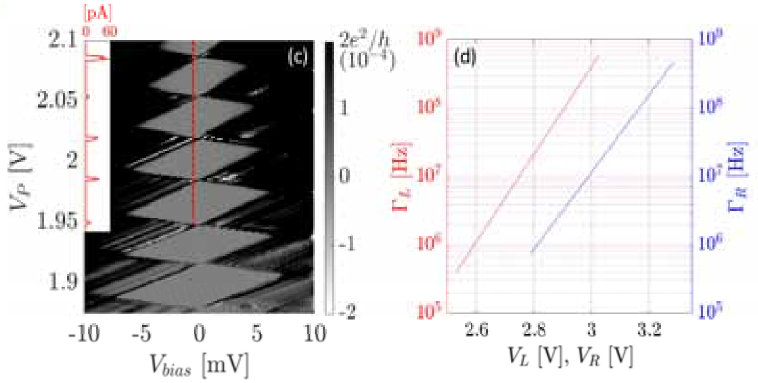
Control of tunnel rate



- MOS device with no explicit barrier gates
- Tunnel rates still tunable over ~8 orders



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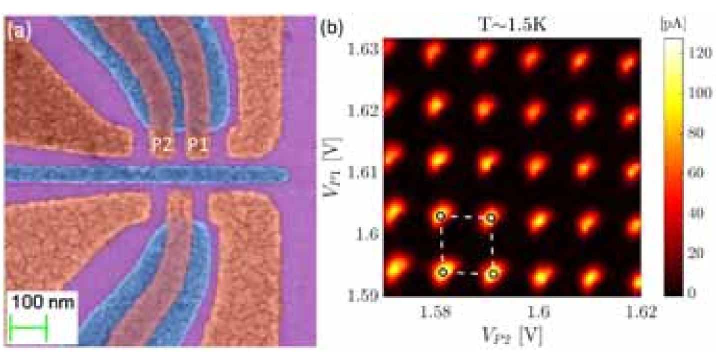
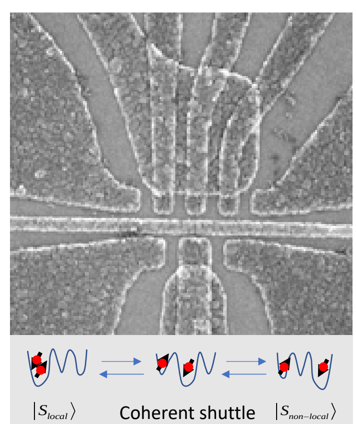
Linear QD arrays

Double dot



$$\begin{array}{c} \\ D1 \\ D2 \end{array} \begin{array}{c} \begin{array}{cc} D1 & D2 \end{array} \\ \begin{pmatrix} 16.9 \pm 0.6 & 0.8 \pm 0.4 \\ 0.8 \pm 0.2 & 17.5 \pm 0.2 \end{pmatrix} \end{array} \text{aF}$$

Triple dot



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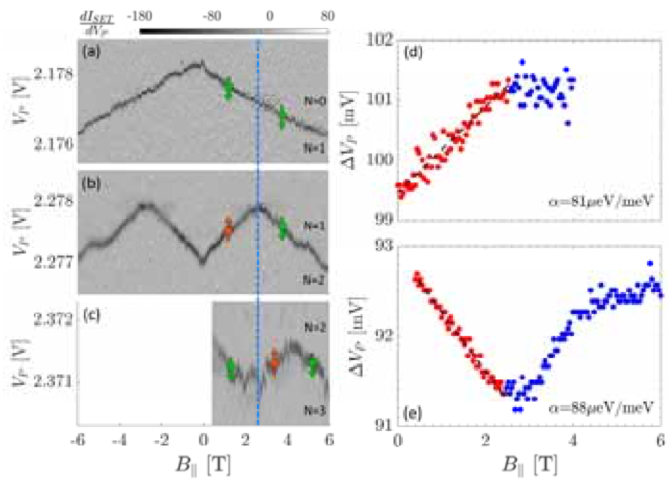
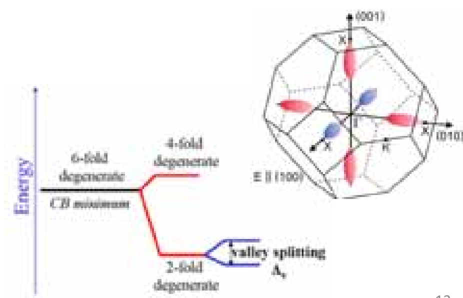
Magneto-spectroscopy and valley states



- ❑ Spin filling of first 3 electrons
- ❑ Crossover at 2.5 T due to excited valley state, 290 μeV gap for this device



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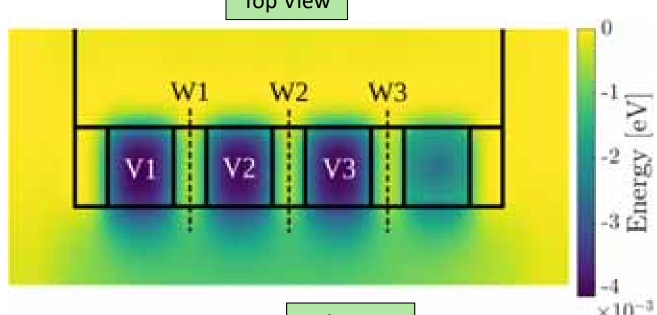
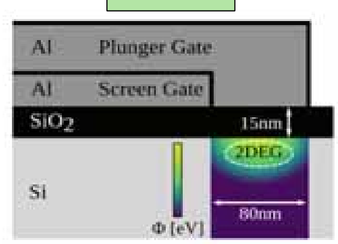
Quantum dot simulation

- Electrostatically-defined Quantum Dots (QDs)
  - Plunger gates = V1,V2,…
  - Tunnel gates = W1, W2,…
- Addressing/Manipulating Qubits
  - *g*-factor modulation (Stark effect)
  - Heisenberg exchange coupling
  - Electron spin resonance (ESR)

Top View



Side View



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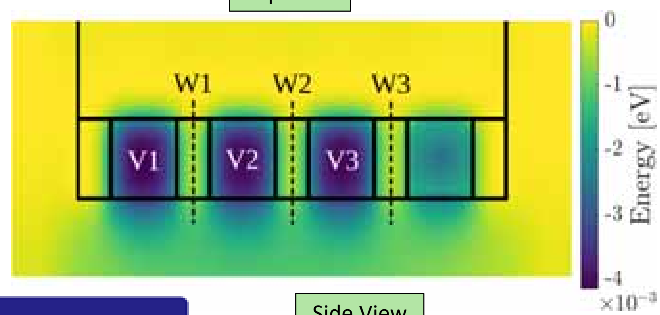
QuDiPy (quantum dot simulations in python)

- Solve 3D Poisson equation
  - NextNano++ (S. Birner et al., 2007)
- Determine effective parameters (spin Hamiltonian)
- Apply optimal control methods

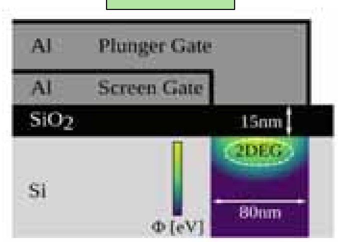
Top View



N-qubit Hamiltonian (rotating frame)

$$H(t) = \mu_B \sum_{j=1}^{N}\left\{\frac{g_j(t)-g_0}{2}B_0 Z_j + B_{RF}(t)\left[\cos\phi(t)\, X_j + \sin\phi(t)\, Y_j\right]\right\} + \sum_{j=1}^{N-1}\frac{J_{j,j+1}(t)}{4}\vec{\sigma}_j\cdot\vec{\sigma}_{j+1}$$

Side View



Map effective parameter controls back to experimental controls, $\vec{V}(t), \vec{B}_{RF}(t)$

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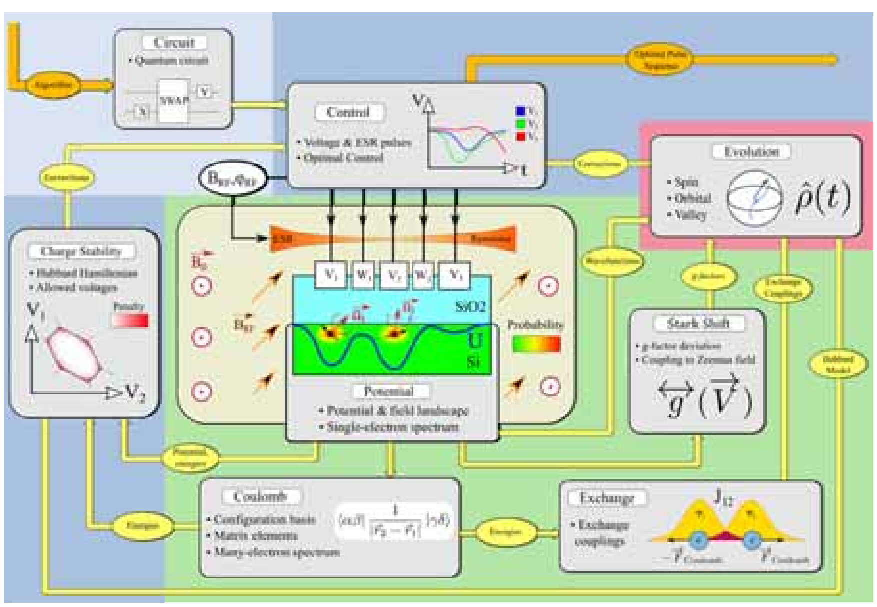
Simulator Modules

Circuit

Control



Spin Evolution

Dot Array

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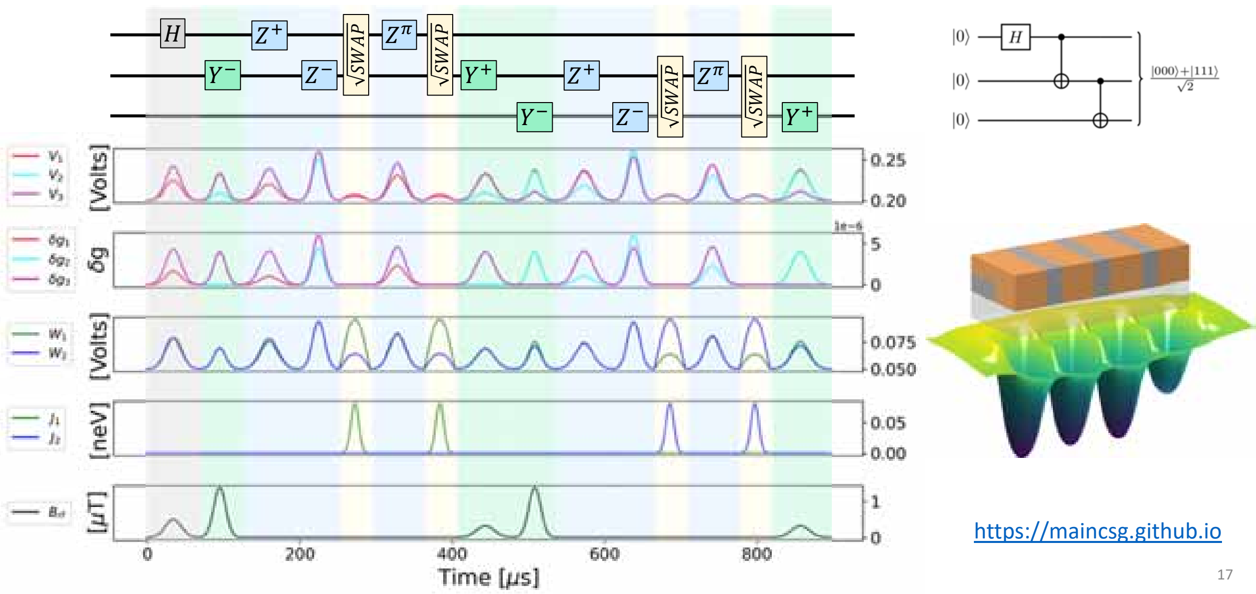
Control pulse engineering and simulation



https://maincsg.github.io

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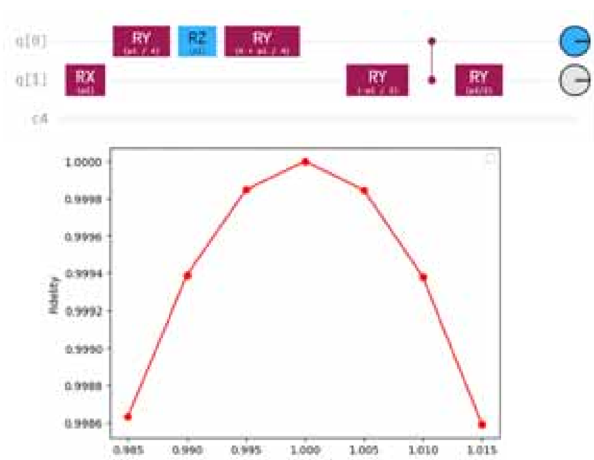
Utility of simulations

- Effects of pulse errors
  - miscalibration
  - noise (1/f, 2-level fluctuator, etc)
- Robust control
  - include decoherence (T_1, T_2)
  - optimize device geometry
- Compare different optimal control methods



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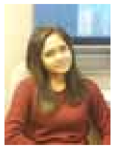
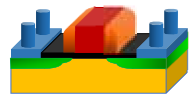
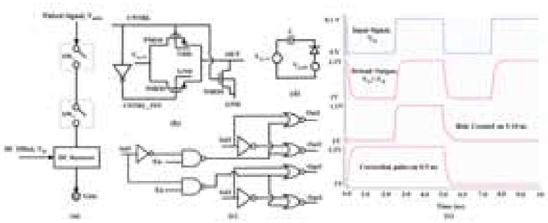
Prof. Lan Wei

Control circuits and cryo-CMOS

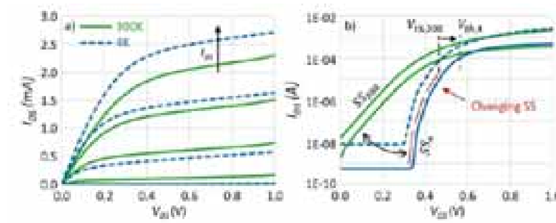




@ low T



R. Absar et al., Scalable Addressing Circuits for a Surface Code Silicon-based Quantum Computer, TechRxiv pre-print (2023)



Hazem Elgabra (2023). Cryogenic CMOS Compact Modeling for Cryo-Electronic Applications. http://hdl.handle.net/10012/19966

Summary

- ☐ Distributed network architecture for silicon QC
- ☐ Small linear qubit arrays, space for wiring, co-integration
- ☐ Simplified MOS QD (shuttling, charge sensing)
- ☐ Realistic multi-qubit simulation

1. B. Buonacorsi et al, *Quantum Science and Technology* **4**, 025003 (2019).
2. E. B. Ramirez et al, *Semicond. Sci. Technol.* **35** 015002 (2020).
3. QuDiPy - https://maincsg.github.io
4. R. Absar et al., Scalable Addressing Circuits for a Surface Code Silicon-based Quantum Computer, *TechRxiv* pre-print (2023)

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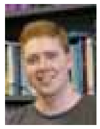
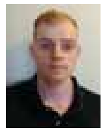
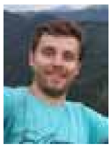

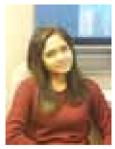

Acknowledgements

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