equal 1

Workshop on Quantum Computing: Devices, Cryogenic Electronics & Packaging

A 22nm FD-SOI CMOS Scalable Quantum Processor SoC with Fully Integrated Control Electronics at 3.5K

Dr. Imran Bashir
VP of Analog Engineering, Equal1 Labs Inc.
Oct 24th, 2023

equal 1

My odyssey into Quantum Computing

- PhD in EE – UT-Dallas (2014)
- 20+ years in semiconductor industry
- Wireless connectivity & cellular, image sensing ICs
- Joined a Quantum Computing Startup Equal1 Labs in 2019
- Just saying “Sky is blue” is not enough for me, I need to understand why is it so.
- Enrolled in Quantum Technology program at SJSU

equal 1

Outline

- *Introduction*
- Quantum Physics for Engineers in a Hurry!
- Quantum Controller Architectures
- Cryogenic Electronics (Equal1)
  - Pattern Generator
  - Pulse Generator
  - Quantum Reference Bias Generation & Capacitive DACs
  - Detector Chain
- Conclusions

equal 1

What does it take to build a Quantum Computer?

https://www.npr.org/

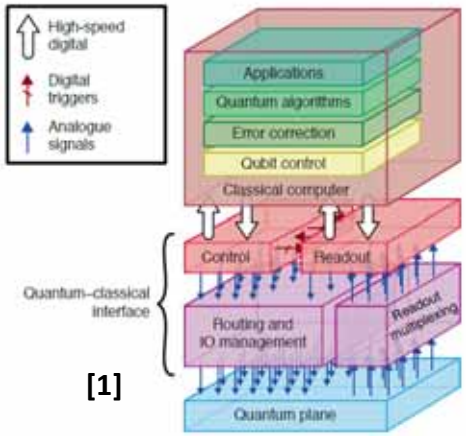
Apollo11 workforce comprised of over 400,000 engineers of the following disciplines:

- Aerospace
- Electrical
- Mechanical
- Systems
- Software
- Structural
- Propulsion
- Thermal
- Materials
- Environmental

• Mechanical	Cryocooler, compressor, chiller, vacuum pump, piped Helium
• Systems/Hardware	Instrumentation, cable plant, cryogenic sensors, amplifiers
• Software	Automation, calibration, computation
• Physicist	Qubit Substrate
Add Chart Recently…	
• Electrical (IC)	Cryogenic Controller IC

equal 1

Quantum Computer Stack



[1]

Innovations & Trends	This Workshop
Quantum + AI, Error Correction & Encoding, State Classifiers, Efficient Transpilers	Dr. Kundra, Dr. Kim, Dr. Spendier, Dr. Haidar
Low power & high fidelity qubit drive and read out architecture	This talk, Dr. Babie, Dr. Otten, Dr. Lee, Dr. Galicia, Castriotta
High density multiplexing at mK, 2.5D / 3D packaging	Dr. Schreckenberg, Dr. Das, Dr. Smith
Superconductor, semiconductor, photonics, trapped ions	Dr. Tennant, Dr. Zumbuhl, Dr. Baugh, Dr. Zalba, Dr. Tran, Dr. Steiner

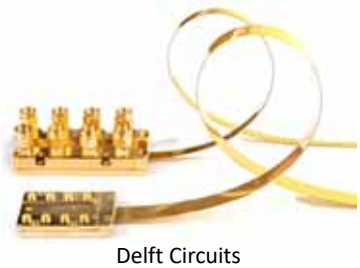
equal 1

Other Innovation Areas

Cryocoolers
- High cooling power at mK
- Quick turn and sample loading
- Fully integrated sensors & controls

Maybell Quantum

Cabling
- High density flexible cabling supporting wide bandwidth and low thermal load

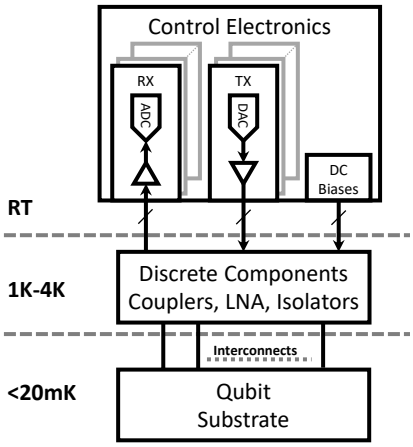


Delft Circuits

equal 1

The Era Before Integrated Cryogenic Electronics

- Main electrical components of a Quantum Computer
  - Quantum Processor where qubits are located
  - Classical Controller:
    - Driving circuits: Generate waveforms to induce quantum operations
    - Read out circuits: read the state of qubit using SET, RF reflectometry (drain or gate)
  - Other: Couplers, amplifiers, attenuators, circulators, resonators
- Is this the best architecture to support 1M qubits? What are the limits?



equal 1

A Little Detour into Thermodynamics

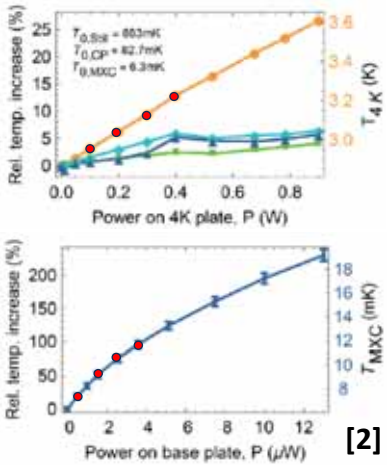
- Passive Heat Loads

$$\Delta P_i = \frac{\partial P_i}{\partial T_i}\Delta T_i$$

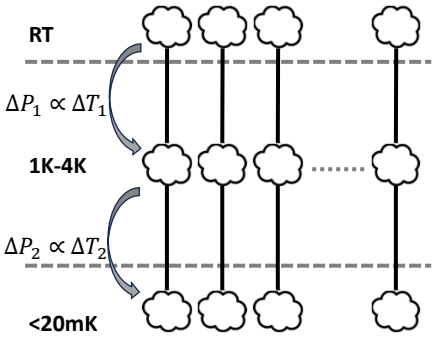
- Active Heat Loads

$$P = I^2 R$$

- Radiative Loads
  - Ignored for lower temperature stages



[2]



equal 1

A Little Detour into Thermodynamics

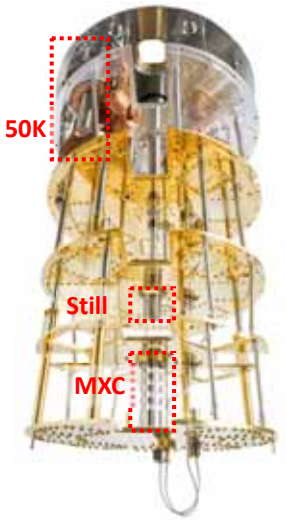
Thermal budget (P_{lim}) limits the amount of cabling and electronics that can be integrated at a given stage in the cryocooler.

$P_{dis,i} = P_{passive,i} + P_{IC,i} + P_{active,i}$ *@ the i-th stage*

$P_{lim,i} < P_{dis,i}$ *@ the i-th stage*

Stage name	Temperature (K)	Cooling power (W)	Cable length (mm)
50K	35	30 (at 45 K)	200
4K	2.85	1.5 (at 4.2 K)	290
Still	882×10^{-3}	40×10^{-3} (at 1.2 K)	250
CP	82×10^{-3}	200×10^{-6} (at 140 mK)	170
MXC	6×10^{-3}	19×10^{-6} (at 20 mK)	140

[2]

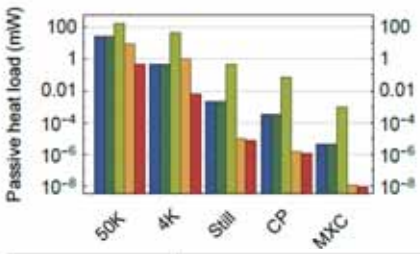


Source: bluefors.com

equal 1

Integration Strategies and Challenges

- Considering passive loads ONLY
  - 30k mW/45mW ~ 666 cables @ 50K
  - 1500 mW/1mW ~ 1500 cables @ 4K
  - 20 µW/0.013µW ~ 1538 cables @ MXC
- *Not enough for 1M qubits*
- *How do you fit that many cables in the cryocooler?*
- *What about the discrete components and their active load?*



Preferred for RF Signals

UT85-SS-SS

UT85-NbTi

[2]

UT85-SPCW

TwP AWG35 Cu-NbTi

TwP AWG36 PhBr-NbTi

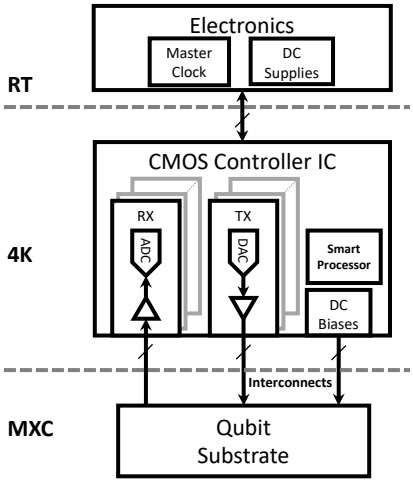
Preferred for DC Signals

		50K	4K	Still	CP	MXC
Drive line UT085 SS-SS	Measured HL	45(23) mW	1.0(2) mW	4(3) µW	0.4(2)µW	0.013(6)µW
	Predicted HL	24-27 mW	0.4-1.7 mW	1.9-2.1 µW	0.33-0.43 µW	0.004 µW
Flux line UT085 SS-SS	Measured HL	56(27) mW	1.2(2) mW	2(1) µW	0.29(3) µW	0.025(5) µW
	Predicted HL	24-27 mW	0.4-1.7 mW	1.9-2.1 µW	0.30 µW	0.027-0.131 µW
Output line UT085 NbTi	Measured HL	-	-	-	0.29(12) µW	0.020(16) µW
	Predicted HL	-	-	-	0.29-0.39 µW	0.012-0.023 µW

equal 1

The Era of Integrated Cryogenic Electronics

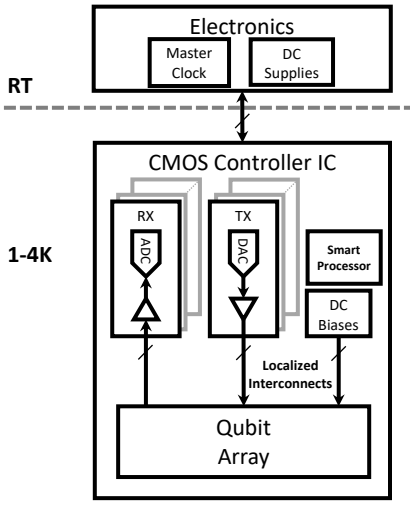
- Move main functions of signal generation/detection to/from the quantum processor to 4K. Only a few clock & bias channels needed from RT electronics.
- Pros:
  - Simplified cable plant from RT to 4K
  - Reasonable compromise for both qubit substrate and controller IC
  - Qubit substrate is located at MXC to achieve optimum quantum metrics in best technology option
  - Cryogenic controller is located at 4K → reasonable high cooling power → more TX/RX channels designed in commercial CMOS. Risk of carrier freeze out mitigated.
- Challenges:
  - IO passive load constraint at MXC not addressed
  - Solution: Packaging & multiplexing schemes → Dr. Schreckenberg, Dr. Das & Dr. Smith talks tomorrow!



equal 1

An Alternative: Monolithic Integration of Qubits and Control Electronics

- Qubits and localized control electronics on the same die
- Pros:
  - Seamless control of electronics for qubit operations
  - Low parasitics → large signal bandwidths
  - IO bottleneck addressed with dense localized routing
- Challenges:
  - 'Hot Qubits'
  - Qubit substrate designed in commercial CMOS technology
  - Heating effects



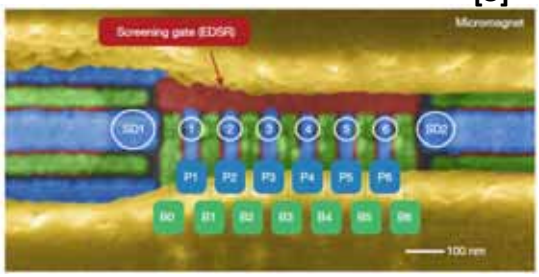
equal 1

Engineered Process vs. Foundry Process

Engineered Process

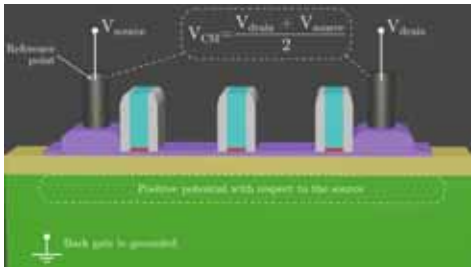
- Molecular Beam Epitaxy for crystal growth
- E-Beam based patterning
- Custom recipe & flexible design rules
- Fine pitch between barriers and plungers
- Integrated micro-magnets

[3]



Commercial Foundry Process

- Czochralski (CZ) Method for crystal growth
- Photolithography / EUV
- Fixed recipe & design rules
- Barrier/plungers pitch defined by process spec
- No integrated micro-magnets



equal 1

Outline

- Introduction
- *Quantum Physics for Engineers in a Hurry!*
- Quantum Controller Architectures
- Cryogenic Electronics (Equal1)
  - Pattern Generator
  - Pulse Generator
  - Quantum Reference Bias Generation & Capacitive DACs
  - Detector Chain
- Conclusions

equal 1

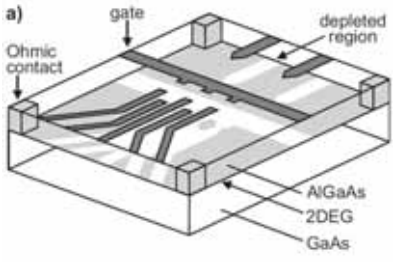
Quantum Physics for Engineers in a Hurry!

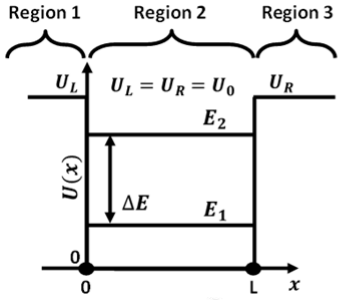
- Critical concepts for Silicon qubits
  - Quantum Dots
  - Charge Sensors
  - Quantum Dot with a DC Magnetic Field (Zeeman Effect)
  - Measurement Method
  - Larmor Precession
  - Quantum Dot with an AC Magnetic Field (Rabi Oscillation)

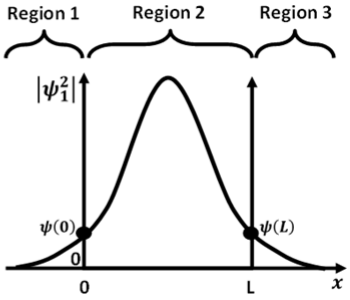
equal 1

Quantum Dots (Particle in a Box)

An elementary treatment of Quantum Dot reveals discrete energy levels and the criterion for charge confinement.







Solve 1-D Time Independent Schrodinger Eqn. over x

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi}{dx^2} + U(x)\psi(x) = E\psi(x) \Rightarrow$$

$U(x)$ = Potential Energy $\psi(x)$ = Wave Function

E = System Energy

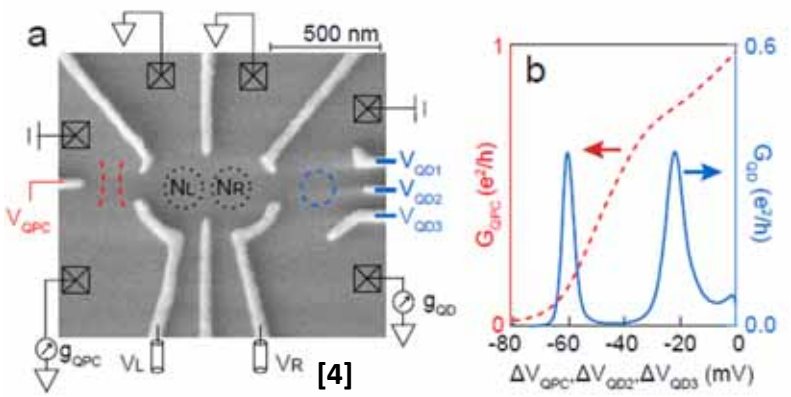
For $U_0 \to \infty$, the solution results in discrete energy levels E_n.

$$E_n = \frac{n^2\pi^2\hbar^2}{2m^*L^2}, \qquad n = 1,2,3,\cdots$$

equal 1

Charge Sensors

A charge sensor is sensitive to the number of charge carriers in the neighboring quantum dots. The curves in figure 'b' shift as a function of occupancy state in quantum dots.

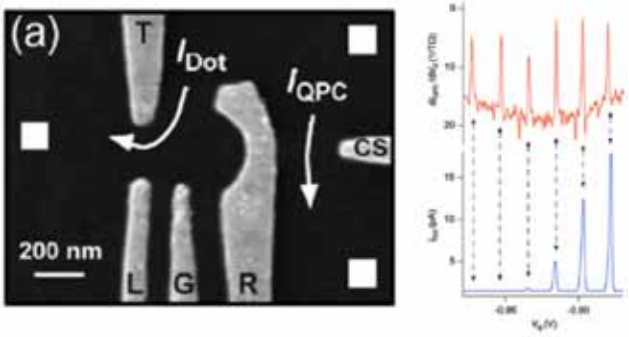


[4]

equal 1

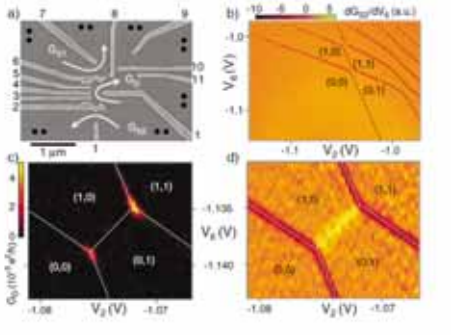
Charge Sensors

A charge sensor shows more features regarding the occupancy state in its transport current compared to a direct current measurement of the quantum dot.



Si Hetrostructure with 1 QD and 1 QPC structure (left); Measurement from QPC sensor (top/red) & QD tunnel current (bottom/blue).

[5]



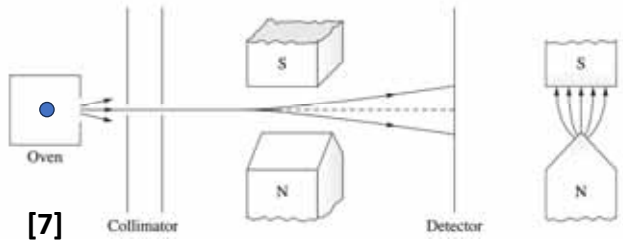
Measurements on DQD with transport current (lower left) and QPC charge sensor (top and bottom right).

[6]

equal 1

Stern-Gerlach Experiment

- Performed in 1922 by Otto Stern and Walther Gerlach
- Proved quantization of *spin angular momentum $\vec{S}$ and energy $\hat{E}$*



[7]

$$\vec{B} = B_o\vec{z}$$
$$\hat{E} = -\vec{\mu}\cdot\vec{B}$$
$$\vec{\mu} = -g\cdot\frac{e}{2m_e}\vec{S}$$
$$\vec{F} = \nabla(\mu\cdot\overrightarrow{B})$$
$$\vec{S} = \widehat{S_x}\vec{x} + \widehat{S_y}\vec{y} + \widehat{S_z}\vec{z}$$
$$S_z = \frac{\hbar}{2}\cdot\begin{pmatrix}1 & 0\\ 0 & -1\end{pmatrix}$$

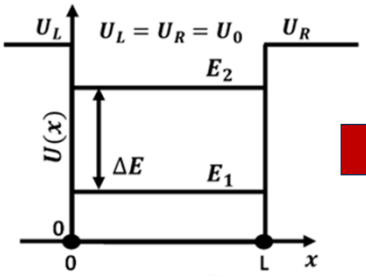
$\vec{B}$ *Magnetic Field*
μ Magnetic Moment
g Gyromagnetic ratio
$\vec{F}$ Force causing deflection
$\vec{S}$ Spin angular momentum

equal 1

Quantum Dot with a DC Magnetic Field

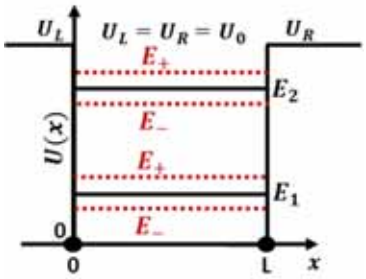
$$\vec{B} = B_o\vec{z}$$
$$\hat{H} = -\vec{\mu}\cdot\vec{B}$$
$$\vec{\mu} = -g\cdot\frac{e}{2m_e}\vec{S}$$
$$\vec{S} = \widehat{S_x}\vec{x} + \widehat{S_y}\vec{y} + \widehat{S_z}\vec{z}$$
$$\hat{H} = \frac{\hbar\omega_o}{2}\cdot\begin{pmatrix}1 & 0\\ 0 & -1\end{pmatrix}$$
$$\omega_o = \frac{e\cdot B_o}{m_e}$$
$$H|\uparrow\rangle = E_+|\uparrow\rangle$$
$$H|\downarrow\rangle = E_-|\downarrow\rangle$$
$$E_+ = +\frac{\hbar\omega_o}{2};\ E_- = -\frac{\hbar\omega_o}{2}$$

$\vec{B} = 0$



$$E_n = \frac{n^2\pi^2\hbar^2}{2m^*L^2}, n = 1,2,3,\cdots$$

$\vec{B} = B_o\vec{z}$

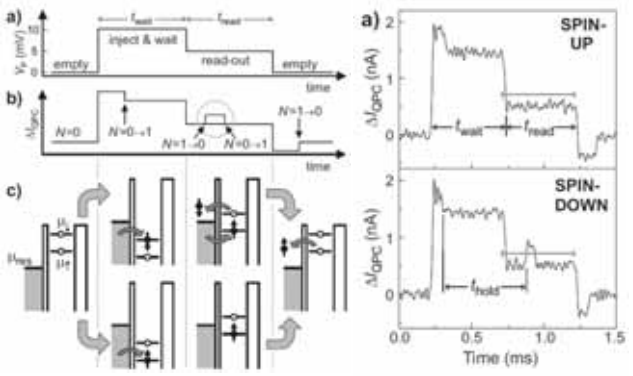


Each discrete energy level splits into E_+ & E_- aka Zeeman split

equal 1

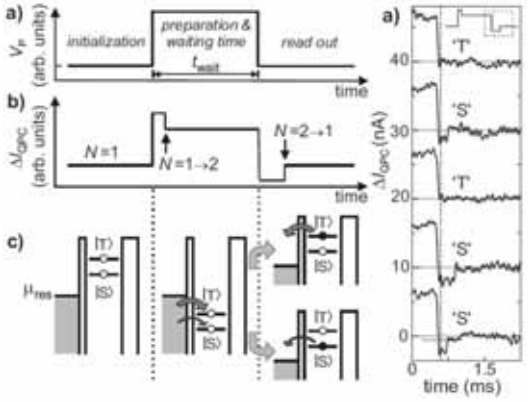
Measurement Method

Energy Selective Readout (Spin to charge conversion)
The information is encoded in the electron spin which is detected as a change in tunneling current.



[8]

Tunnel Rate Selective Readout
The information is encoded in the tunneling rate of the charge carrier as it travels back into the reservoir.



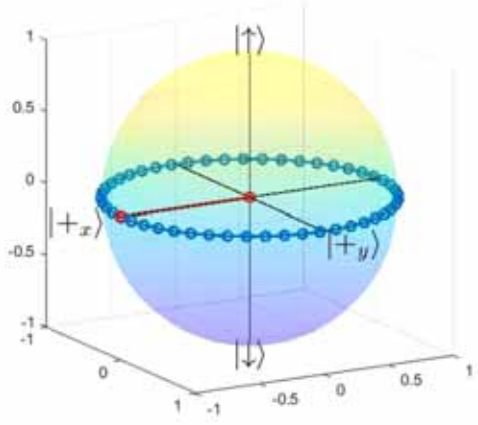
equal 1

Larmor Precession

$$\vec{B} = B_o\vec{z}$$
$$\widehat{H} = -\mu \cdot \vec{B}$$
$$\widehat{H} = \frac{\hbar\omega_o}{2} \cdot \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$
$$\omega_o = \frac{e \cdot B_o}{m_e}$$
$$|\psi(0)\rangle = \cos\frac{\theta}{2}|\uparrow\rangle + e^{i\phi}\sin\frac{\theta}{2}|\uparrow\rangle$$
$$|\psi(t)\rangle = e^{\frac{-i\omega_o t}{2}}\left(\cos\frac{\theta}{2}|\uparrow\rangle + e^{i(\phi+\omega_o t)}\sin\frac{\theta}{2}|\downarrow\rangle\right)$$
$$P_{+x} = |\langle +_x|\psi(t)\rangle|^2 = \frac{1}{2}\cdot[1+\sin\theta\cos(\phi+\omega_o t)]$$
$$E_+ = +\frac{\hbar\omega_o}{2};\ E_- = -\frac{\hbar\omega_o}{2};\ \omega_o = \frac{\Delta E}{\hbar}$$

ω_o is the Larmor Frequency
Increasing B_o → Increasing ΔE & ω_o

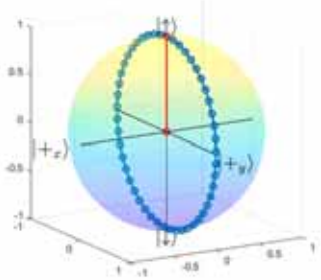
The trajectory of $|\psi(t)\rangle$ on the bloch sphere is the Larmor Precession.

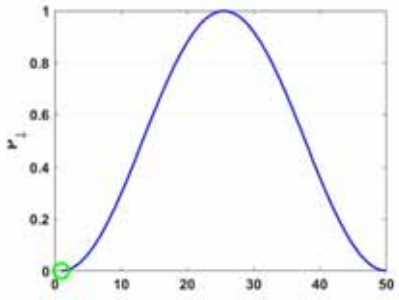


equal 1

Quantum Dot with an AC Magnetic Field (Rabi Oscillation)

The trajectory of $|\psi(t)\rangle$ on the bloch sphere due to excitation signal. The complete trajectory will also include Larmor precession (fast oscillations).





Excitation Signal

$$\vec{B} = B_o\vec{z} + \boxed{B_1 \cos\omega t\, \vec{x}} \;;\; B_1 \ll B_o$$

$$\hat{H} = -\mu \cdot B$$

$$\hat{H} = \frac{\hbar}{2} \cdot \begin{pmatrix} \omega_o & \omega_1 e^{-i\omega t} \\ \omega_1 e^{i\omega t} & -\omega_o \end{pmatrix} \leftarrow \textit{Time Dependent!}$$

Using rotation frame approximation & perturbation theory

$$\hat{H} = \frac{\hbar}{2} \cdot \begin{pmatrix} -\Delta\omega & \omega_1 \\ \omega_1 & \Delta\omega \end{pmatrix} \leftarrow \textit{Time Independent!}$$

$$\omega_o = \frac{e \cdot B_o}{m_e};\; \omega_1 = \frac{e \cdot B_1}{m_e};\; \Delta\omega = \omega - \omega_o$$

$$|\psi(0)\rangle = \cos\frac{\theta}{2}|\uparrow\rangle + e^{i\phi}\sin\frac{\theta}{2}|\uparrow\rangle$$

$$|\psi(t)\rangle \approx e^{\frac{-i(\phi+\omega_o t)}{2}}\left(\cos\left(\frac{\theta+\omega_1 t}{2}\right)|\uparrow\rangle + e^{-i(\phi+\omega_o t)}\sin\left(\frac{\theta+\omega_1 t}{2}\right)|\downarrow\rangle\right)$$

$$P_\downarrow = |\langle\downarrow|\psi(t)\rangle|^2 = \frac{\omega_1^2}{\Delta\omega^2+\omega_1^2}\sin^2\left(\frac{\sqrt{\Delta\omega^2+\omega_1^2}}{2}t\right)$$

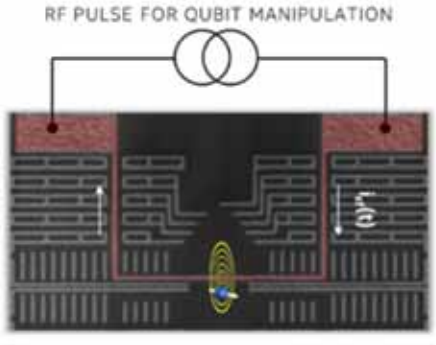
ω_o is the Larmor Frequency & ω_1 is the Rabi Frequency
Increasing excitation amplitude B_1 → Increasing ω_1

equal 1

Modes of Qubit Excitation

ESR

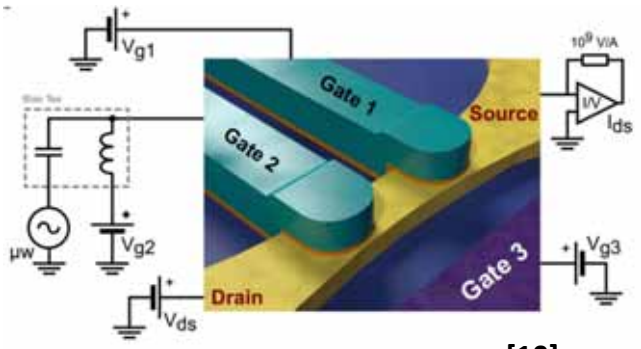
RF current through a loop conductor generates EM field in the vicinity of the quantum while the gradient from the static magnetic field determines the qubit addressability.



[9] Zwerver (Intel)

EDSR

RF voltage on gate conductor (open load) generates E field in the vicinity of the quantum while the gradient from the static magnetic field determines the qubit addressability.



[10]

equal 1

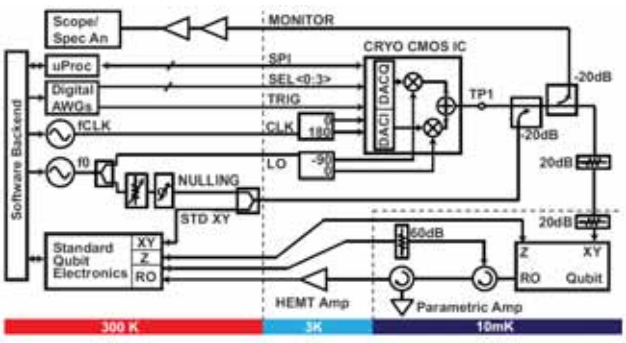
Outline

- Introduction
- Quantum Physics for Engineers in a Hurry!
- *Quantum Controller Architectures*
- Cryogenic Electronics (Equal1)
  - Pattern Generator
  - Pulse Generator
  - Quantum Reference Bias Generation & Capacitive DACs
  - Detector Chain
- Conclusions

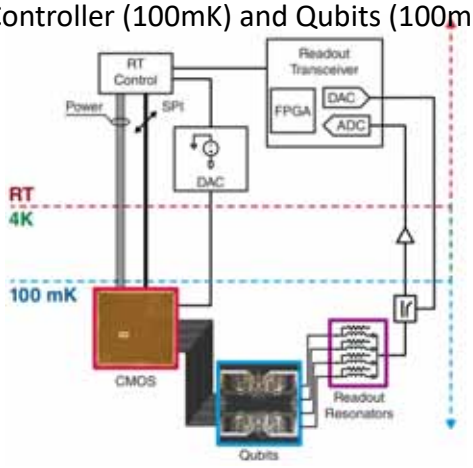
equal 1

Quantum Controller Architectures

Bardin et. al **[11], UCSB, Google**
Controller (3K) and Qubits (10mK)



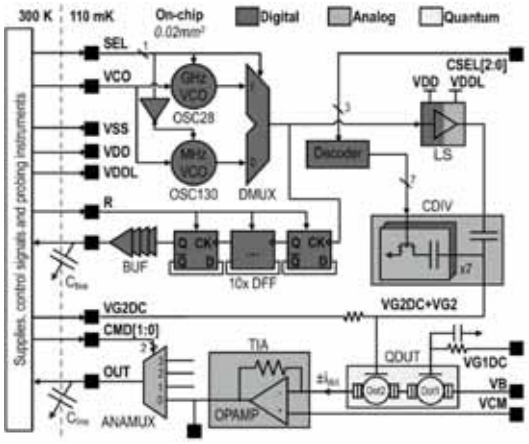
Pauka et. al **[12], Sydney NSW, Microsoft**
Controller (100mK) and Qubits (100mK)



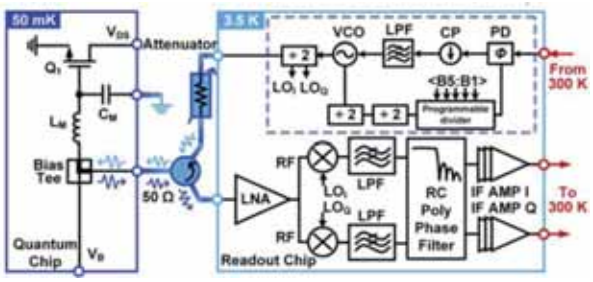
equal 1

Quantum Controller Architectures

Guevel et. al **[13] Cea Leti**
Controller + Qubits (110mK)



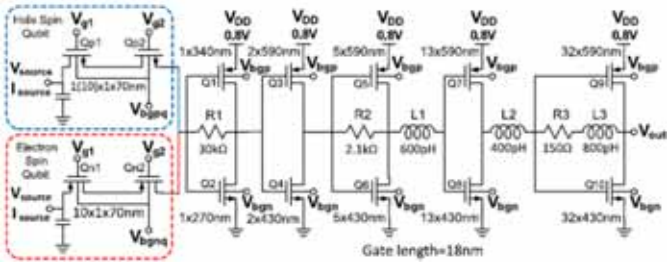
Ruffino et. al **[14], EPFL**
Controller (3.5K) + Qubits (50mK)



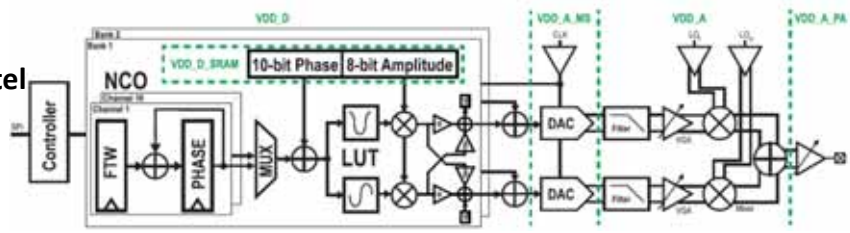
equal 1

Quantum Controller Architectures

Gong et. al **[15], U of Toronto**
Detector & Qubits (4K)



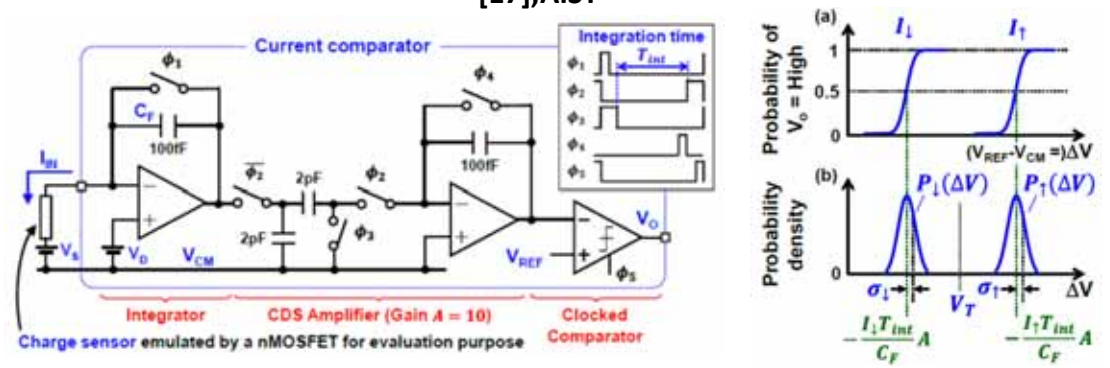
Van Dijk et. al **[16], TU Delft, Intel**
Controller (4K)



equal 1

Quantum Controller Architectures

[17],AIST



equal 1

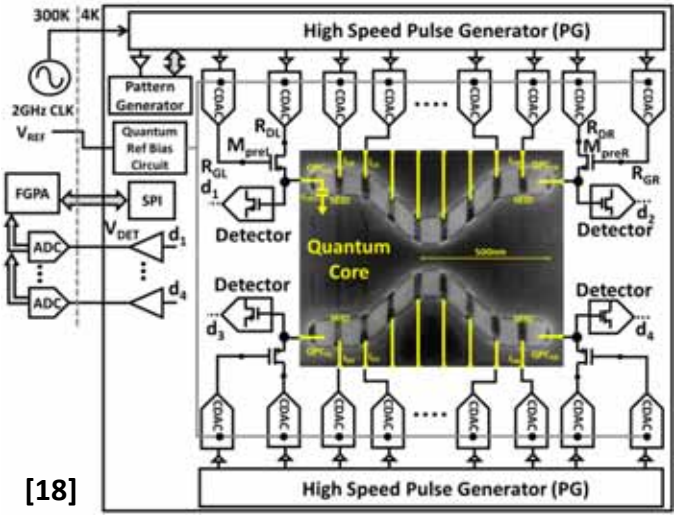
Outline

- Introduction
- Quantum Physics for Engineers in a Hurry!
- Quantum Controller Architectures
- *Cryogenic Electronics (Equal1)*
  - Pattern Generator
  - Pulse Generator
  - Quantum Reference Bias Generation & Capacitive DACs
  - Detector Chain
- Conclusions

equal 1

The Quantum Processor Unit (QPU)

- Fully integrated Quantum Processor Unit comprising a Quantum Core co-located with control + detection circuitry
  - Qubits: 6 (min); 240 (max)
  - Up-to 32 CDAC injectors
  - Up-to 8 detectors
  - High Speed Pulse Generator with 8 concurrent pulse synthesizing blocks
  - Quantum Reference Bias Circuit generates all biases for the quantum structure from a single input reference
  - Pattern Generator as command-and-control for all electronics in the QPU

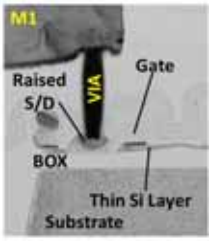


[18]

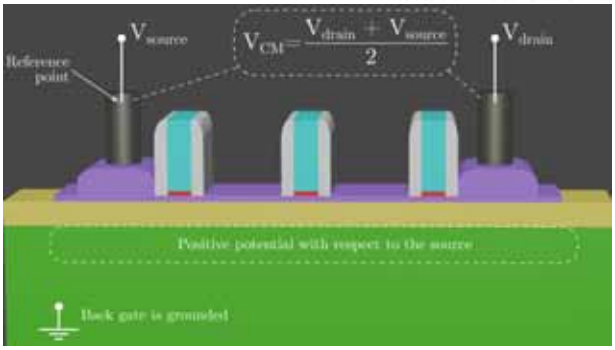
equal 1

Quantum Structure

- Fabricated in 22nm CMOS FDSOI Process from GlobalFoundries
- Lateral confinement dimensions ~70 x 70 nm^2, separation ~ 20 nm barrier
- Effective confinement in thin intrinsic Si layer (4nm)
- Channel electric field control by gates and common mode voltage

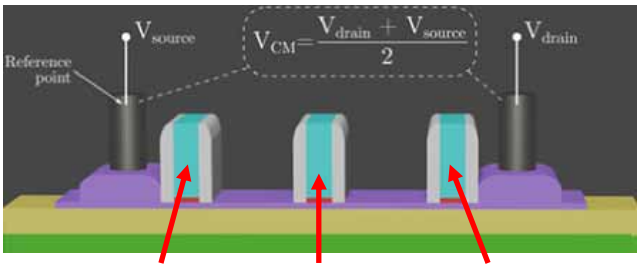


[18]



Quantum Structure Biasing

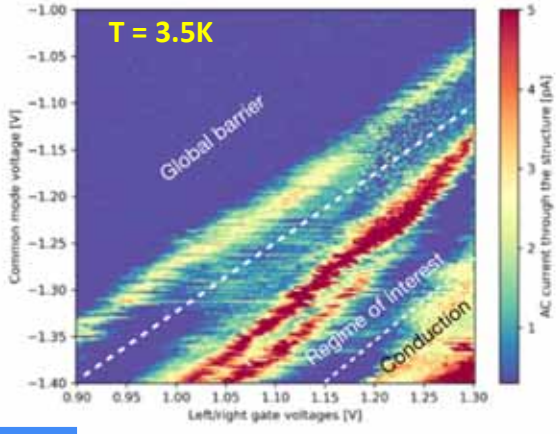
As a result, the common mode works as a single global plunger.

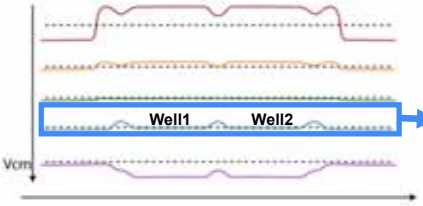


Left Gate Voltage

Middle Gate Voltage

Right Gate Voltage





Dual Quantum Dot Mode with small tunneling barrier

Quantum Structure Modeling in QTCAD

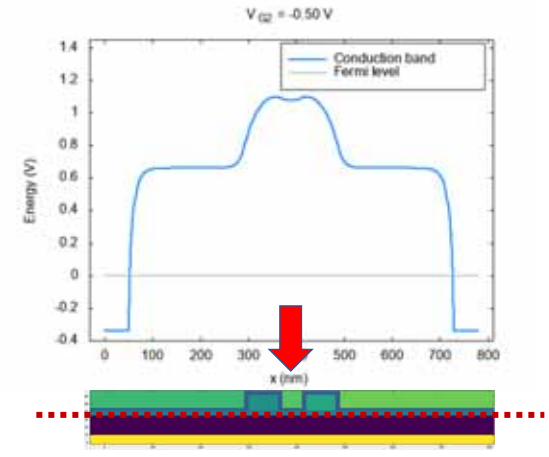
(Tool developed by Nanoacademic Technologies)

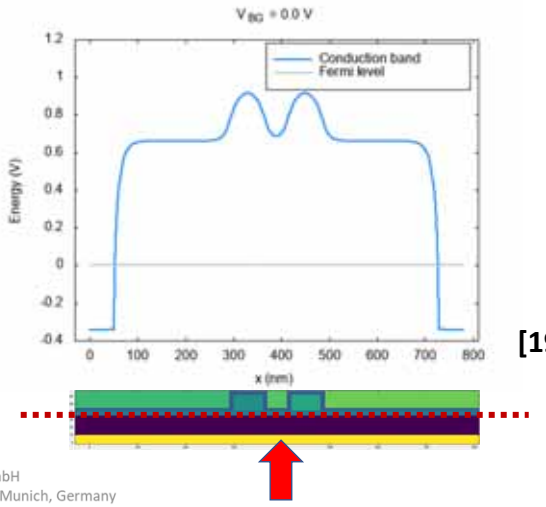
nextnano
Software for semiconductor nanodevices

NANOACADEMIC TECHNOLOGIES

P lggdh#Wrs#Jdwh

Edfn#Jdwh

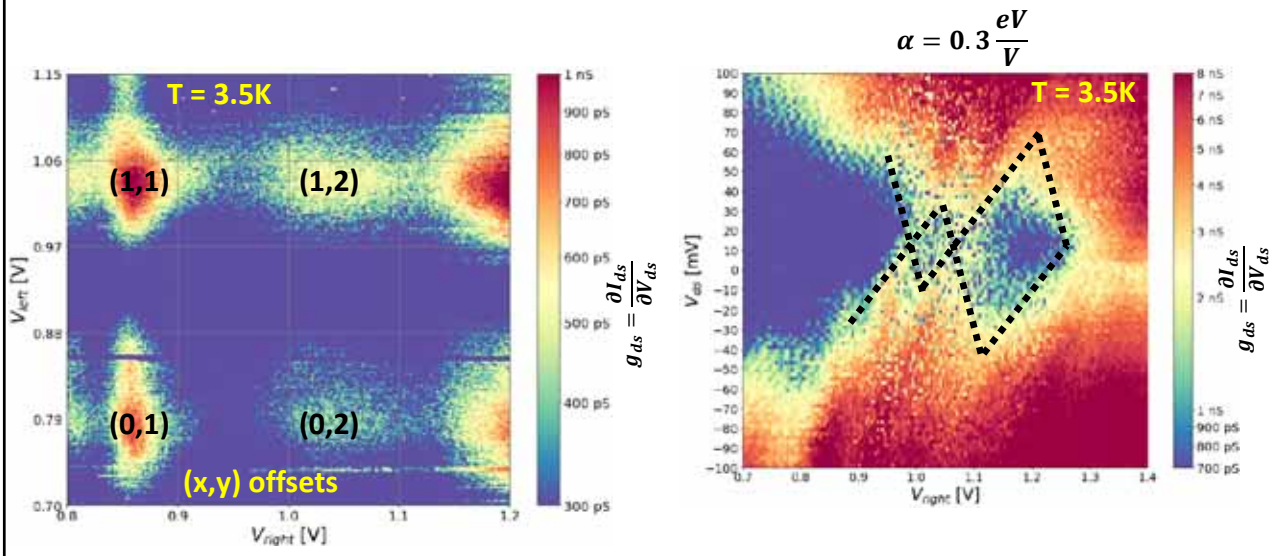




[19]

nextnano GmbH
Konrad-Zuse-Platz 8, 81829 Munich, Germany

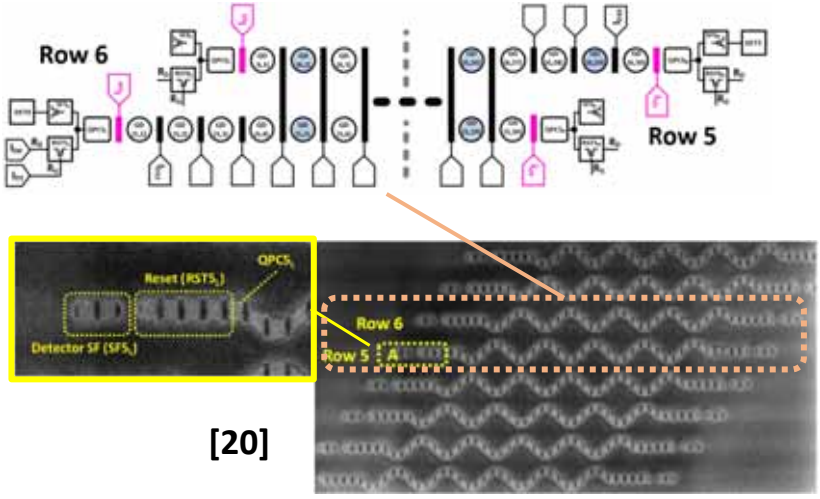
Quantum structure Charge Stability



equal 1

Integrated Quantum SoC

- 240 Quantum Dots
- 30x8 2D Array
- 32 CDACs driving gates
- 8 Detectors at the edge of each row
- Use ‘electron shuttling’ and measure at the edge of structure
- More on ‘electron shuttling’ from Rene Otten

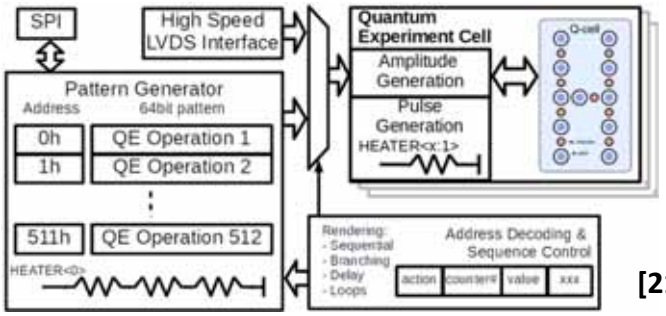


[20]

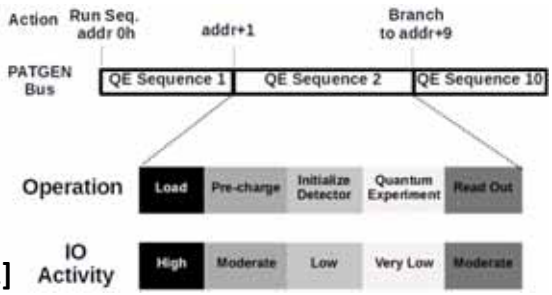
equal 1

Pattern Generator (PATGEN)

- PATGEN drives the 64-bit bus to control all CDACs, detectors & bias generation circuits
- Sequence is pre-loaded before the quantum experiment
- Various execution options: loops, branch etc.



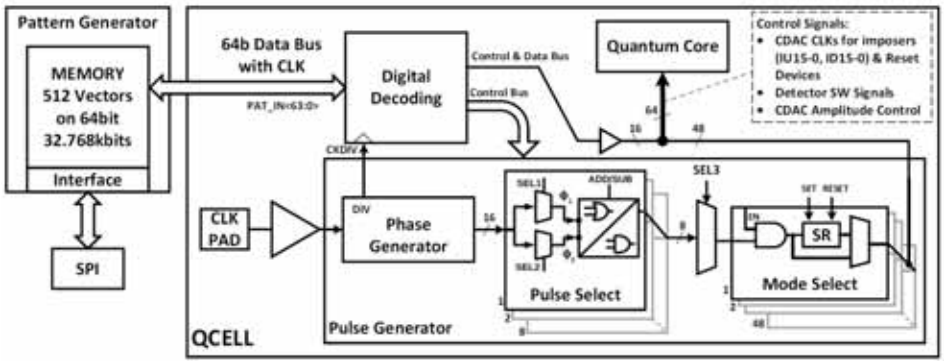
[21]



equal 1

Pulse Generator

- PATGEN drives the 64-bit bus to control all CDACs, detectors & bias generation circuits
- The pre-loaded sequence can be executed in various modes: loops, branch etc.
- Pulse Generator sub blocks:
  - 8-stage Johnson counter; Stage 1: AND/OR gate; Stage 2: Propagate / SR Latch

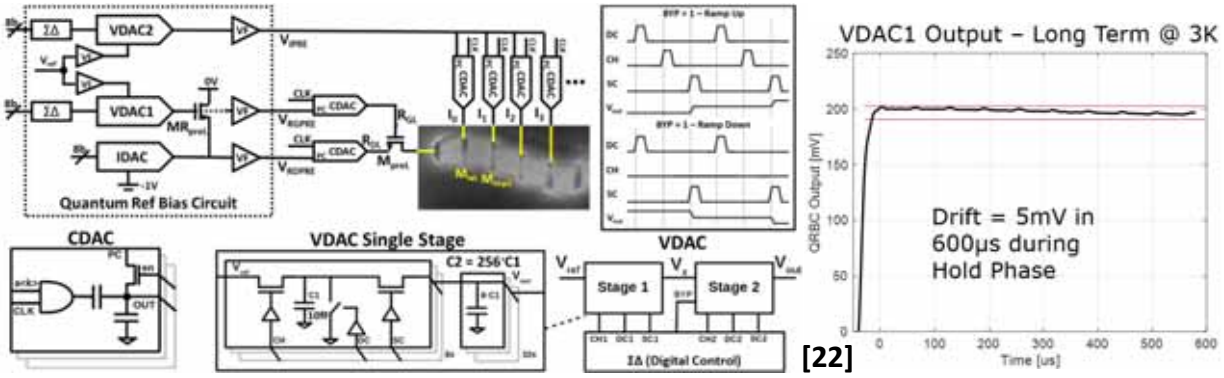


38

equal 1

Quantum Reference Bias Generation

- VDAC1 and VDAC2 generates pre-charge for M_{pre} gate (R_{GL}) and all imposers from a single reference V_{ref}
- A replica pre-charge device MR_{pre} and 8-b IDAC generates M_{pre} source bias (R_{DL})
- The digital ΣΔ drives the switch capacitor network and ceases shortly before the quantum experiment

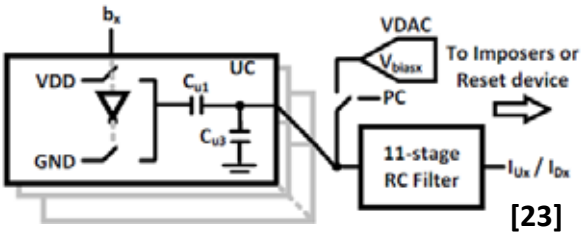


[22]

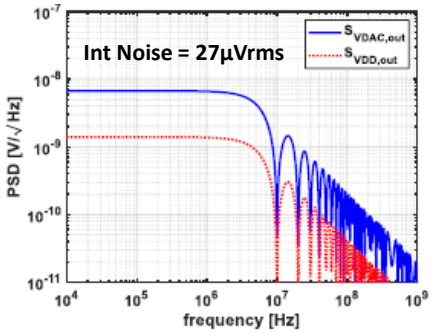
equal 1

Capacitive DAC (CDAC)

- 8-b binary weighted switch capacitor array; range 0-70mV
- Pre-charge bias provided by VDAC or external supply
- Clock gating with input data to reduce dynamic power; No DC current
- 11-stage RC filter to remove fast transients



[23]

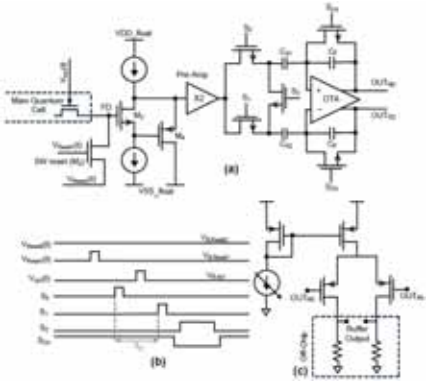


40

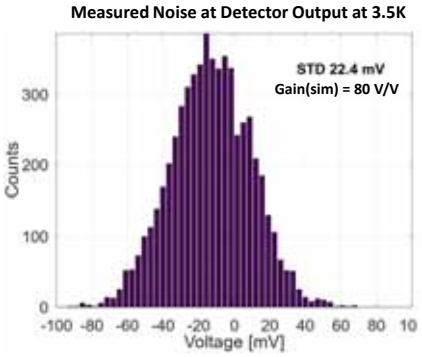
equal 1

Detector Chain

- Detector Chain Stages: Source follower, Pre-Amp, CDS, Output Buffer
- Snap shot of QPC voltage stored on Cs1 and Cs2 before and after QE
- Output buffer is class A stage connected to off-chip loads and ADC interface circuit; I_{dd} = 650uA



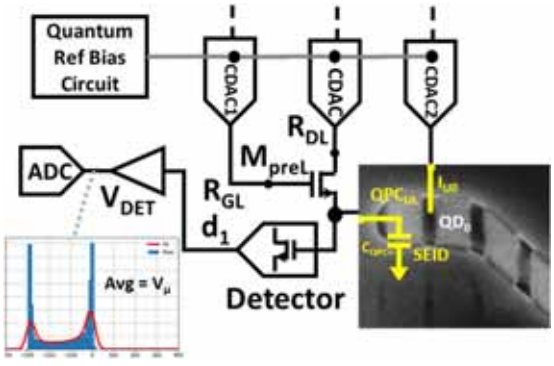
[23]



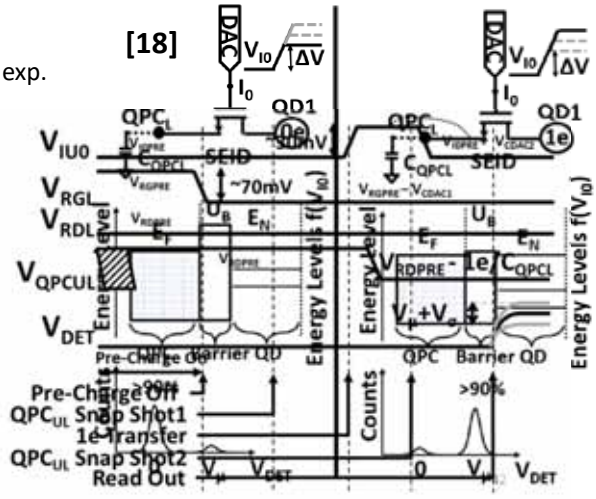
equal 1

Quantum Core Stimulus
M_{pre} Biasing & Single Electron Transfer

V_{RDL} controls potential energy profile in QD_0
V_{RGL} controls M_{preL} gate which is reduced during quantum exp.
V_{IU0} controls coulomb blockade



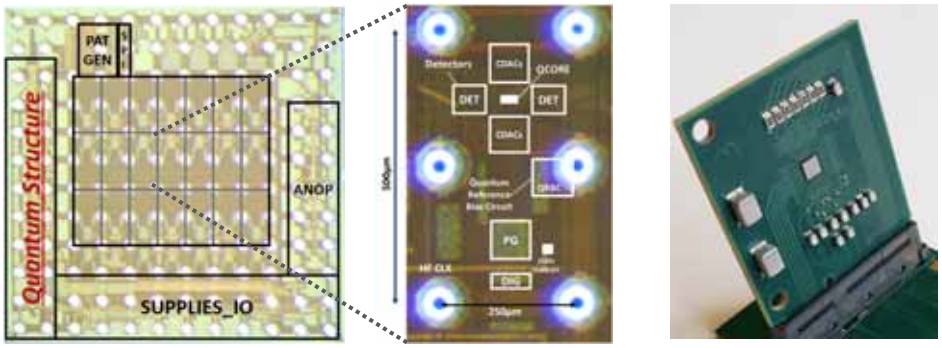
[18]



equal 1

IC Micrograph and Cryo-system

- 3x3mm^2 SoC fabricated in GF 22nm CMOS FD-SOI process in flip chip package
- 28 Quantum Experiment Cells
- Backside of Flip-chip Si makes contact with cold finger inside the cryocooler



equal 1

Putting it all together…

- Desktop size quantum computer comprising compressor, 2-stage GM cryocooler, vacuum pump, motherboard & airside PCB
- DC bias on flex lines & RF Signals on coax
- < 2-ft (internal) cabling
- 200mW cooling power
- 3.3K Base Temperature
- 1.5kW power consumption (110V / 16A Single Phase)

Block	Units per Core	Area (W x H)	Power	Power
		Per Unit	Per Unit	Total
CDACs	40	3.5µm x 45µm	0.27 mW	ǂ0.27 mW
Detectors	8	40µm x 25µm	1 mW	8 mW
VDACs	1	85µm x 84µm	0.23 mW	0.23 mW
PG	1	93µm x 144µm	1 mW	1 mW
Total			2.5 mW	10 mW

ǂ Depends on Quantum Experiment

Signal	Count
Supplies	3
Biases	†2-4
Analog IO	16
Digital IO	7
RFIO	1
Total	29-31

†2 with VDAC

equal 1

Conclusions

- Discussion on key innovation areas in Quantum Computing
- Thermal engineering and impact on system design
- Evolution of quantum computer architecture and the era of cryogenic electronics
- Review of key concepts from Quantum Mechanics and Physics
- Survey of Quantum Controller Architectures

…more importantly

- *It's takes a village to build a quantum computer. You need to be "Jack of all trades, master of none!"*

equal 1

Acknowledgments

Questions?

equal 1

References

1. S. J. Pauka et al., “A cryogenic CMOS chip for generating control signals for multiple qubits,” *Nature Electronics* 4, 64-70 (2021).
2. Krinner, S. et al. Engineering cryogenic setups for 100-qubit scale superconducting circuit systems. Arxiv: 1806.07862v1 (2018).
3. Philips, S.G.J., Mądzik, M.T., Amitonov, S.V. *et al.* Universal control of a six-qubit quantum processor in silicon. *Nature* 609, 919–924 (2022). https://doi.org/10.1038/s41586-022-05117-x
4. Vigneau et al., “Probing quantum devices with radio-frequency reflectometry,” arXiv:2202.10516
5. Appl. Phys. Lett. 91, 213103 2007
6. Physical review VOLUME 93, NUMBER 18, 2004
7. https://sites.esm.psu.edu/~vfm5153/IQM/chapter1.html
8. Hanson, Ronald, et al. "Spins in few-electron quantum dots." *Reviews of modern physics* 79.4 (2007): 1217.
9. Zwerver, Qubits made by advanced semiconductor manufacturing arXiv:2101.12650
10. Corna, A., Bourdet, L., Maurand, R. *et al.* Electrically driven electron spin resonance mediated by spin–valley–orbit coupling in a silicon quantum dot. *npj Quantum Inf* 4, 6 (2018). https://doi.org/10.1038/s41534-018-0059-1

equal 1

References

11. Bardin, J. C. et al. Design and Characterization of a 20-nm Bulk-CMOS Cryogenic Quantum Controller. Solid-State Circuits 54, 3043–3060 (2019).
12. S. J. Pauka et al., “A cryogenic CMOS chip for generating control signals for multiple qubits,” *Nature Electronics* 4, 64-70 (2021).
13. Guevel, L. L. et al. A 110mK 295µW 28nm FDSOI CMOS quantum integrated circuit with a 2.8GHz excitation and nA current sensing of an on-chip double quantum dot. In ISSCC, ses. 19.2, 306–308 (2020).
14. A. Ruffino, Y. Peng, T. -Y. Yang, J. Michniewicz, M. F. Gonzalez-Zalba and E. Charbon, "13.2 A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots," ISSCC 2021, San Francisco, CA, USA, 2021, pp. 210-212, doi: 10.1109/ISSCC42613.2021.9365758.
15. M. J. Gong et al., "Design Considerations for Spin Readout Amplifiers in Monolithically Integrated Semiconductor Quantum Processors," RFIC 2019, Boston, MA, USA, 2019, pp. 111-114, doi: 10.1109/RFIC.2019.8701847.
16. J. P. G. Van Dijk et al., "A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons," in IEEE JSSC, vol. 55, no. 11, pp. 2930-2946, Nov. 2020, doi: 10.1109/JSSC.2020.3024678.
17. H. Fuketa, et. al, “A Cryogenic CMOS Current Comparator for Spin Qubit Readout Achieving Fast Readout Time and High Current Resolution,” in Symp. VLSI Technology, pp. 234–235, 2023.
18. I. Bashir et al., "A Single-Electron Injection Device for CMOS Charge Qubits Implemented in 22-nm FD-SOI," *in IEEE Solid-State Circuits Letters*, vol. 3, pp. 206-209, 2020, doi: 10.1109/LSSC.2020.3010822.
19. F. Beaudoin et al., APL 120, 264001 (2022)

equal 1

References

20. I. Bashir et. Al, “Monolithic Integration of Quantum Resonant Tunneling Gate on a 22nm FD-SOI CMOS Process”; arXiv:2112.04586
21. I. Bashir et al., "A mixed-signal control core for a fully integrated semiconductor quantum computer system-on-chip," *Proc. of IEEE European Solid-State Circuits Conf. (ESSCIRC),* vol. A2L-C4, pp. 14, 2019.
22. I. Bashir et al., "Bias Generation and Calibration of CMOS Charge Qubits at 3.5 Kelvin in 22-nm FDSOI," ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 47-50, doi: 10.1109/ESSCIRC53450.2021.9567784.
23. A. Esmailiyan et al., "A Fully Integrated DAC for CMOS Position-Based Charge Qubits with Single-Electron Detector Loopback Testing," *in IEEE Solid-State Circuits Letters*, DOI: 10.1109/LSSC.2020.3018707.