Cryo-CMOS Transceivers for Control and Readout of Semiconductor Spin Qubits

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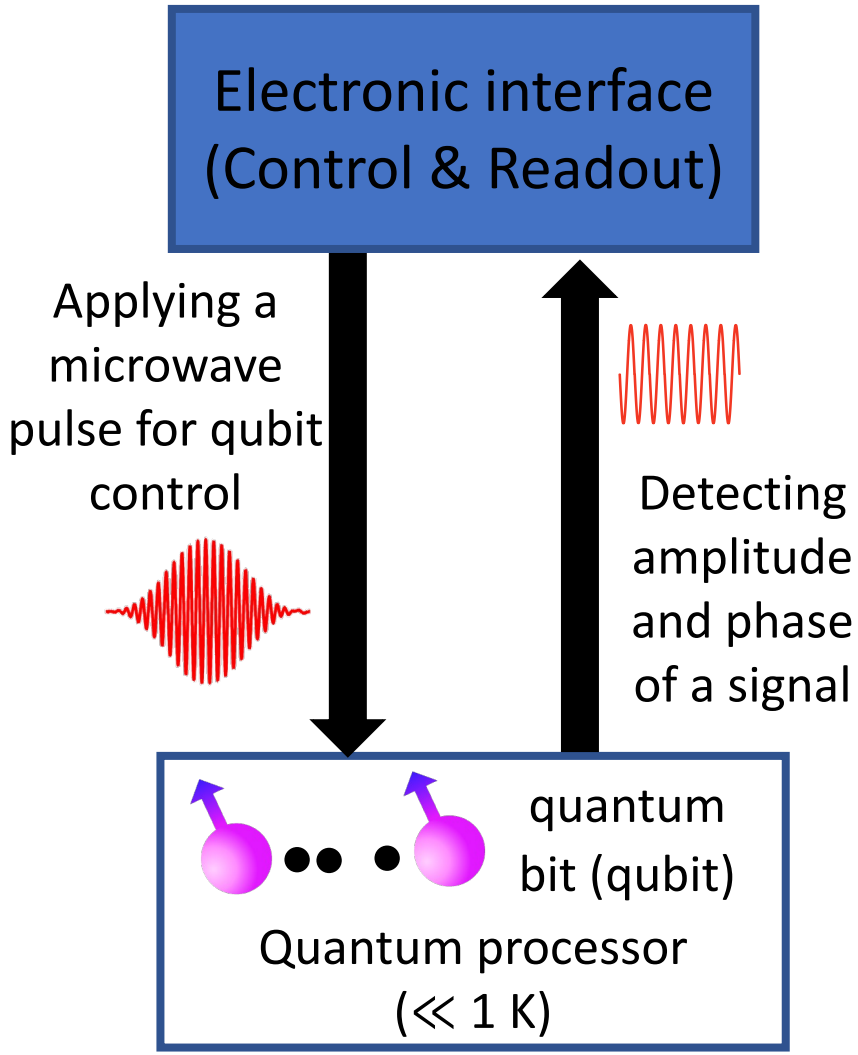
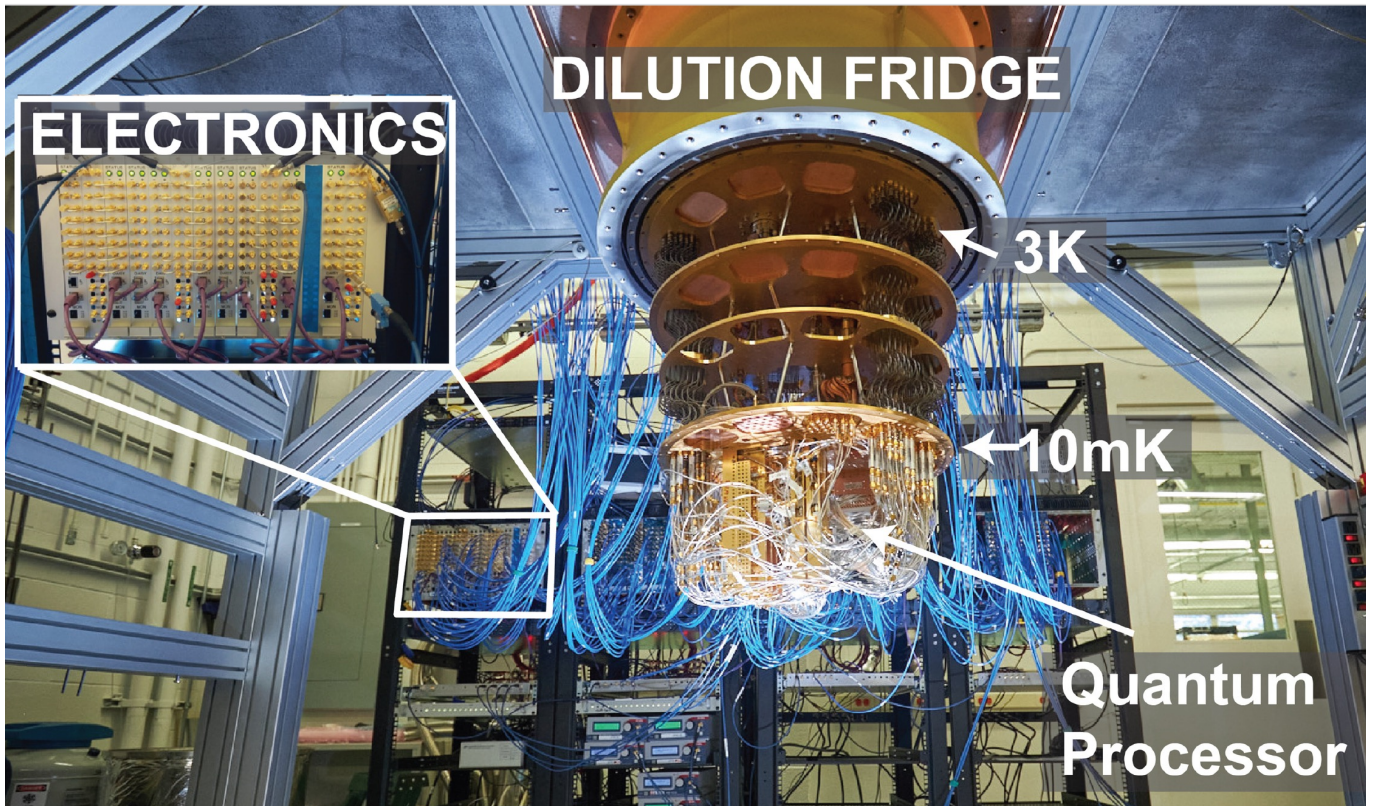
Outline

- Need for cryogenic electronics for scalable quantum computers
  - Associated challenges
- Introducing control and readout principles for spin qubits
- Cryo-CMOS controller for spin qubits
  - Behavior of active and passive CMOS devices at cryogenic temperatures
  - Required circuit and system specification
  - Controller architecture and circuit implementation
  - Electrical characterization
  - Experiments with qubits (single- and two-qubit operations)
- Gate-based readout for spin qubits
  - Receiver architecture and implementation
  - Electrical characterization
  - Experiments with qubits
- Conclusions

General Block Diagram of a Quantum Computer

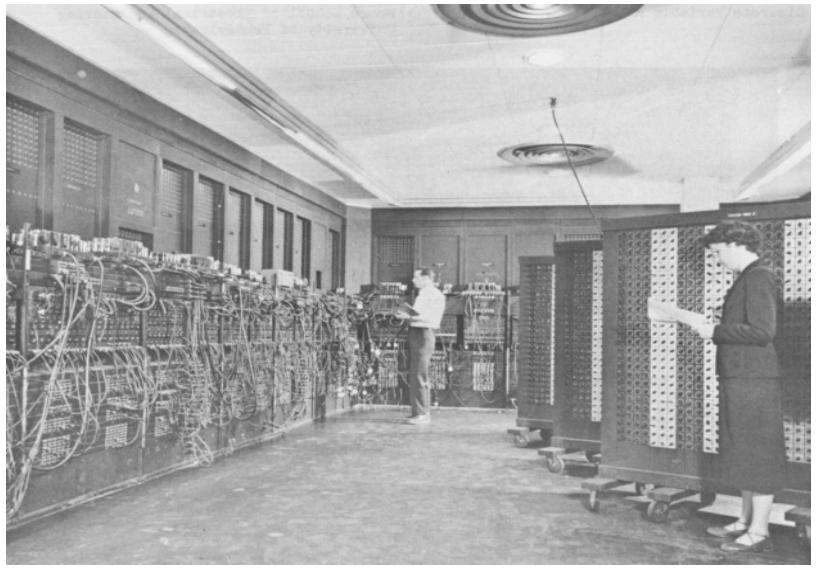




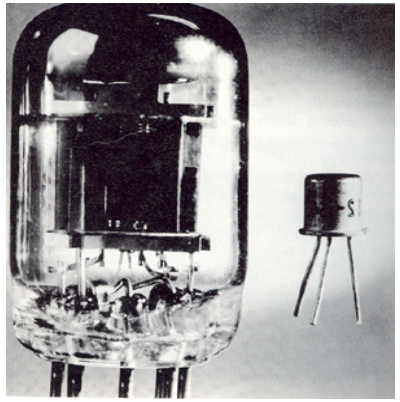
[J. Bardin, ISSCC'23]

What Can We Learn from History?

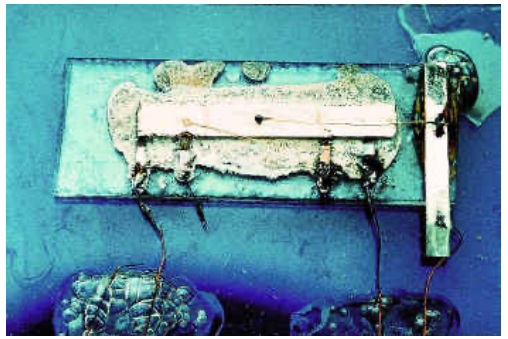
- Miniaturization – Vacuum tube to transistors
- Integration – Transistor to Integrated Circuit



ENIAC
(Vacuum tube)



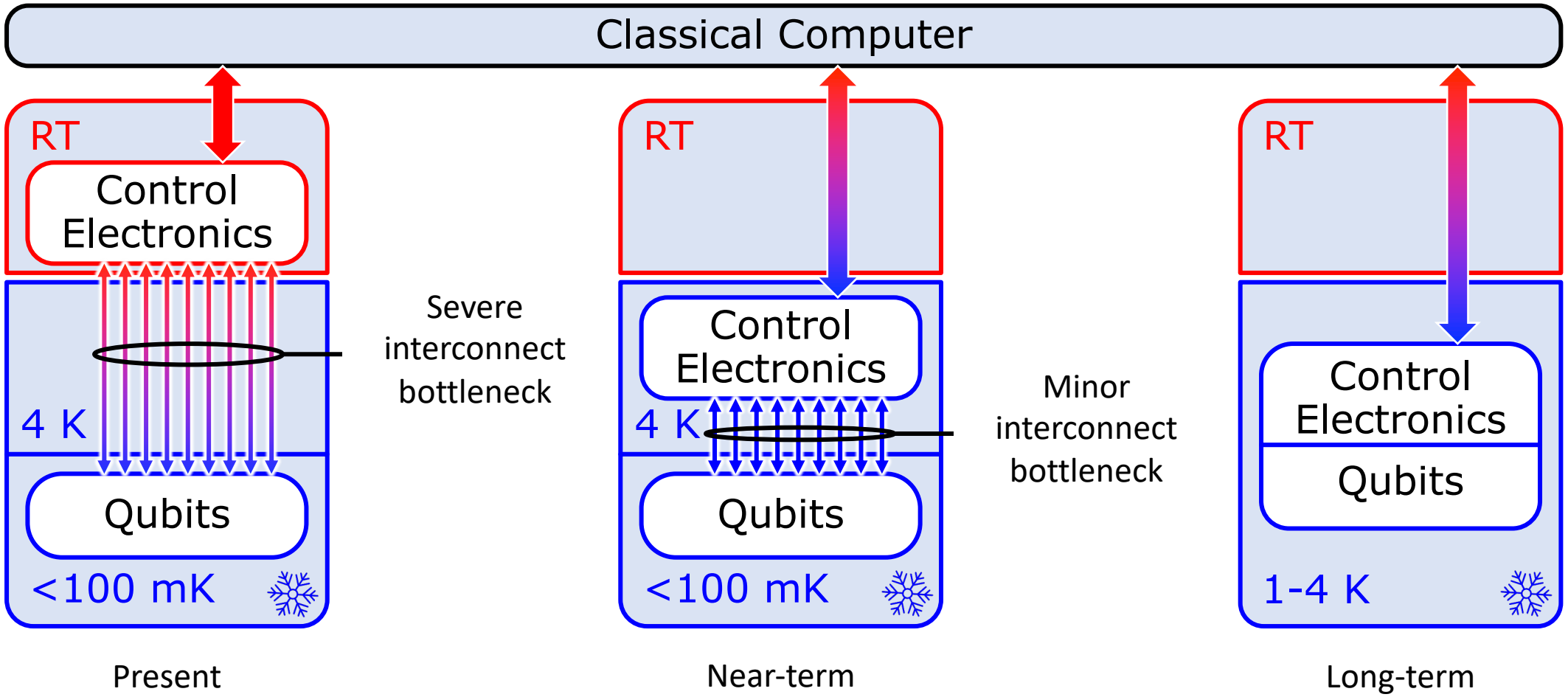
Transistor



Integrated Circuit

Silicon-based
computers

Need for cryogenic electronics



Challenges

- **What kinds of functionalities are needed for qubit control and readout?**

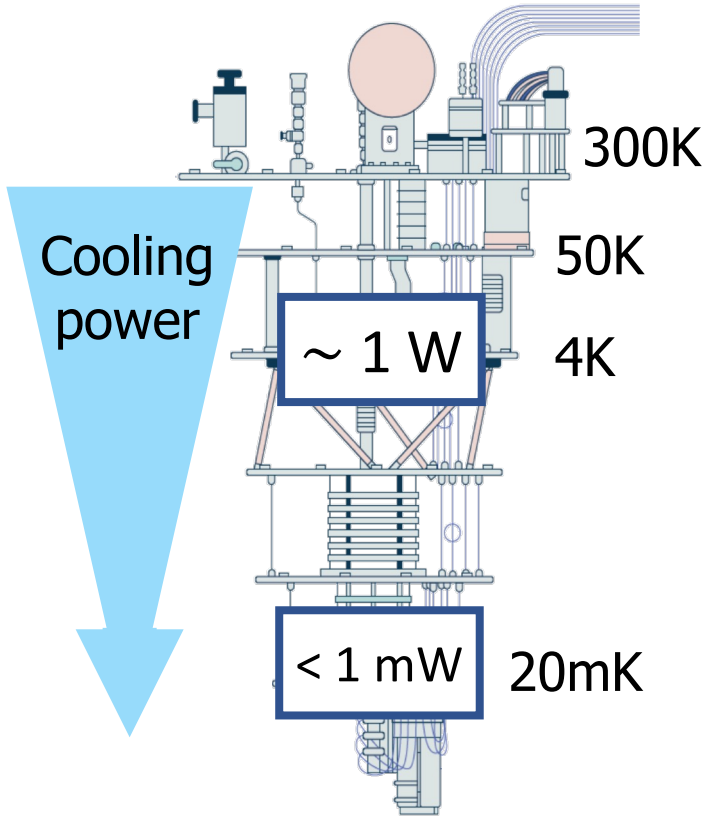
- **System & circuit specifications?**
  - Linearity, noise, jitter,…

- **Cryogenic technology?**
  - How does commercial CMOS perform at 4K? Transistor model?

- **Demanding spec with limited power consumption?**

- **Cryogenic measurements?**

- **Measurements with Qubits?**



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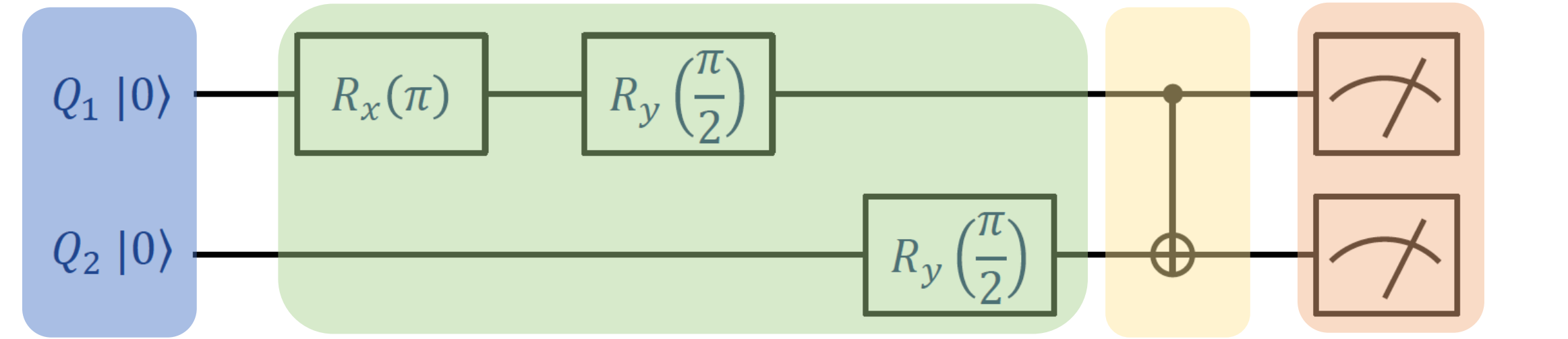
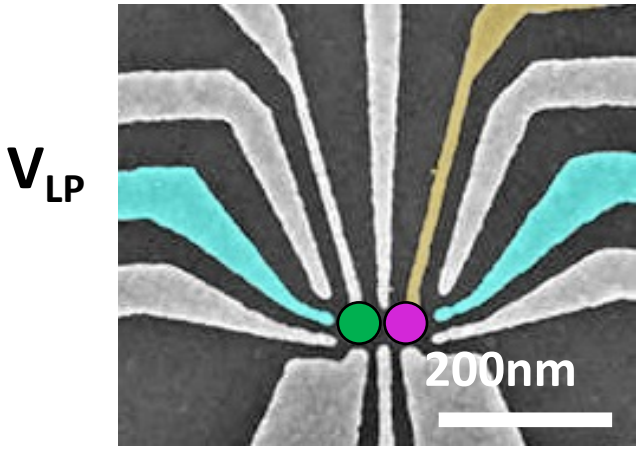
Required Functionalities for running a Quantum Algorithm

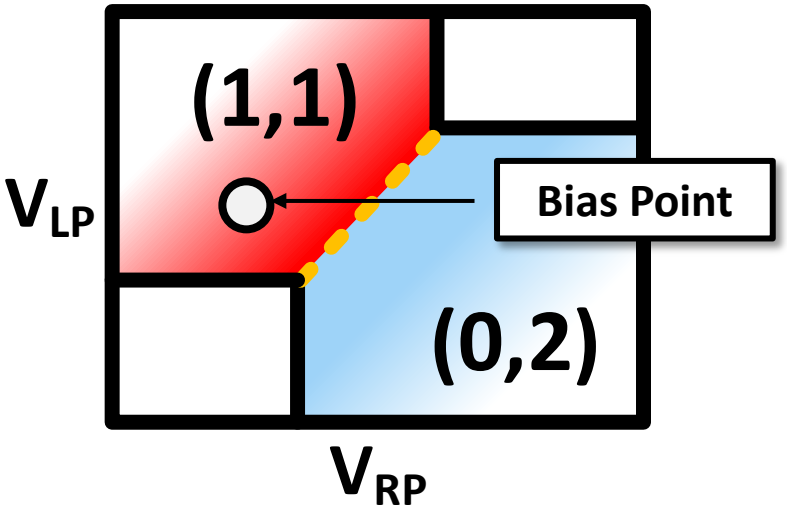


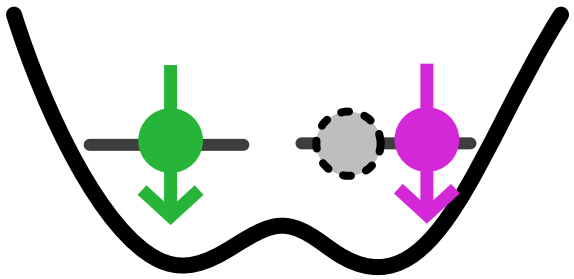
Spin Qubit Operation– Initialization

Double Quantum Dot (DQD)



Stability Diagram



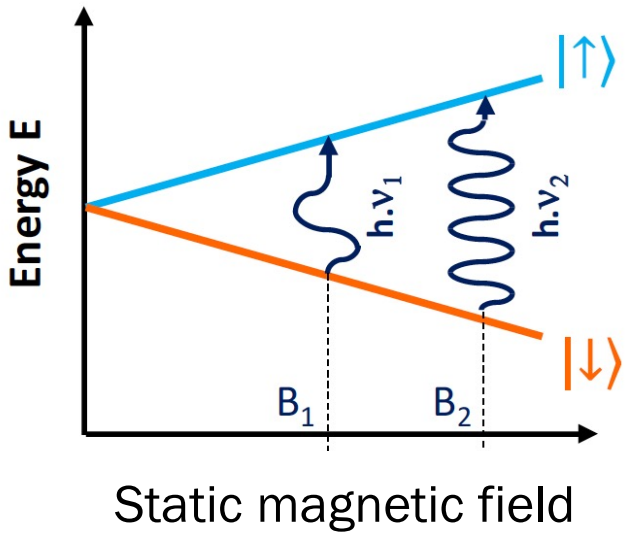


Initialize

- Behavior of double quantum dot → dependent on the voltage of the plunger gates (V_{LP}, V_{RP})
- **(N_L,N_R)** → Electron population on the left and right dots

[B. Prabowo, ISSCC'21]

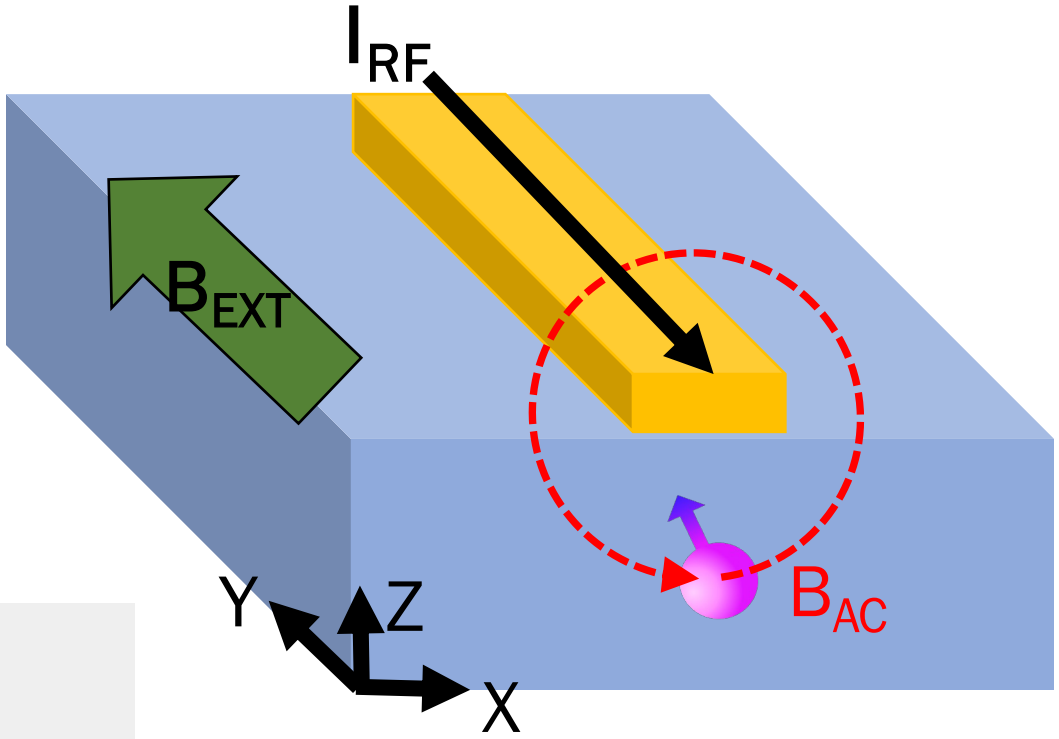
Single-Qubit Operation

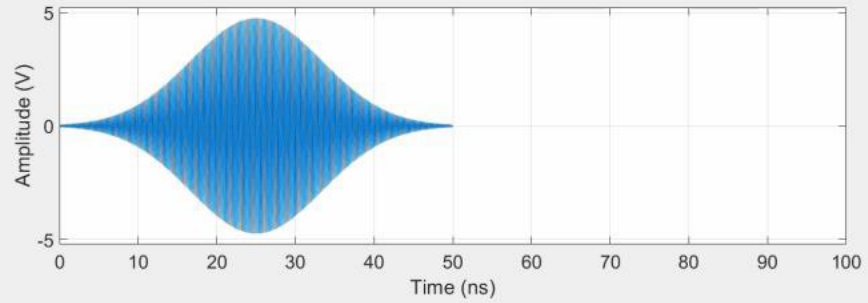


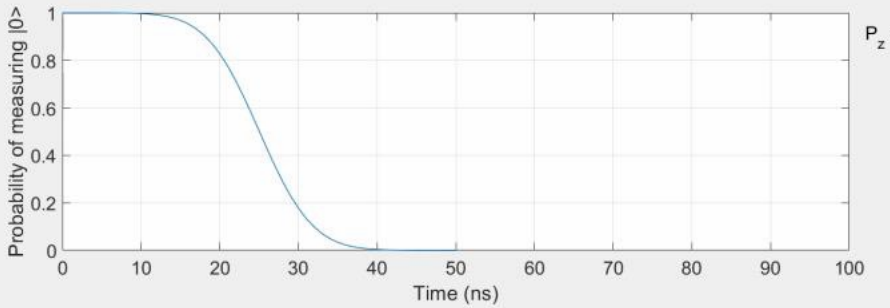
$$\begin{cases} E = \gamma_e h B \\ E = h \cdot f \end{cases} \rightarrow f = \gamma_e \cdot B$$

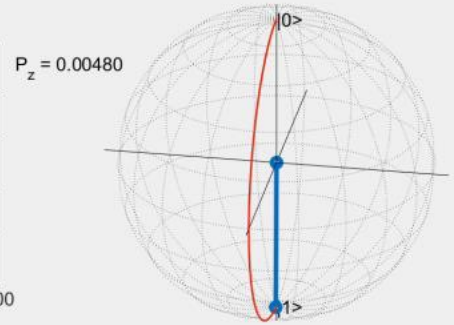
Plank constant

Geometric ratio of electron, 28GHz/Tesla

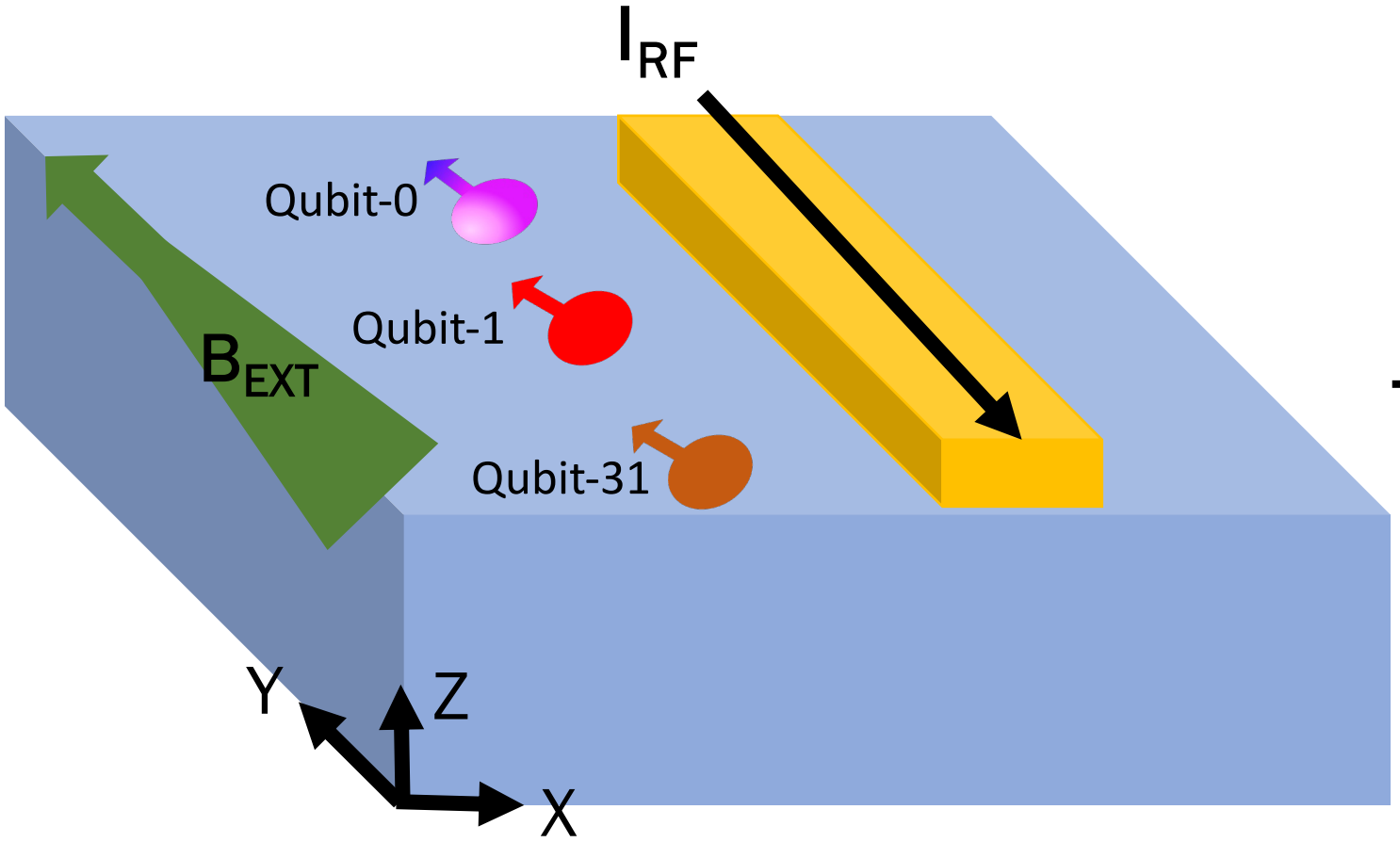


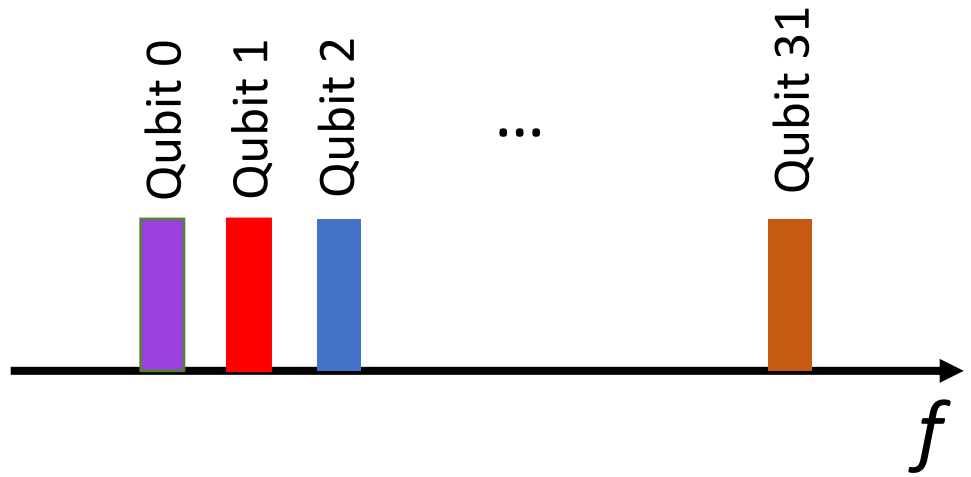




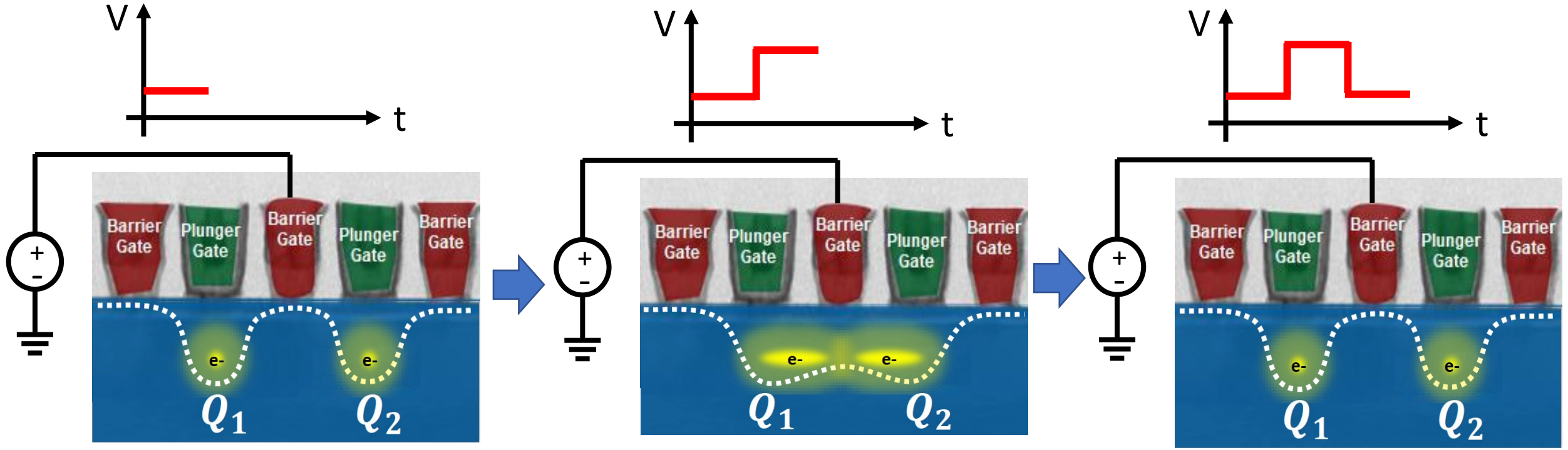


Frequency Multiplexing Technique for Qubit Control





Two-Qubit Gate

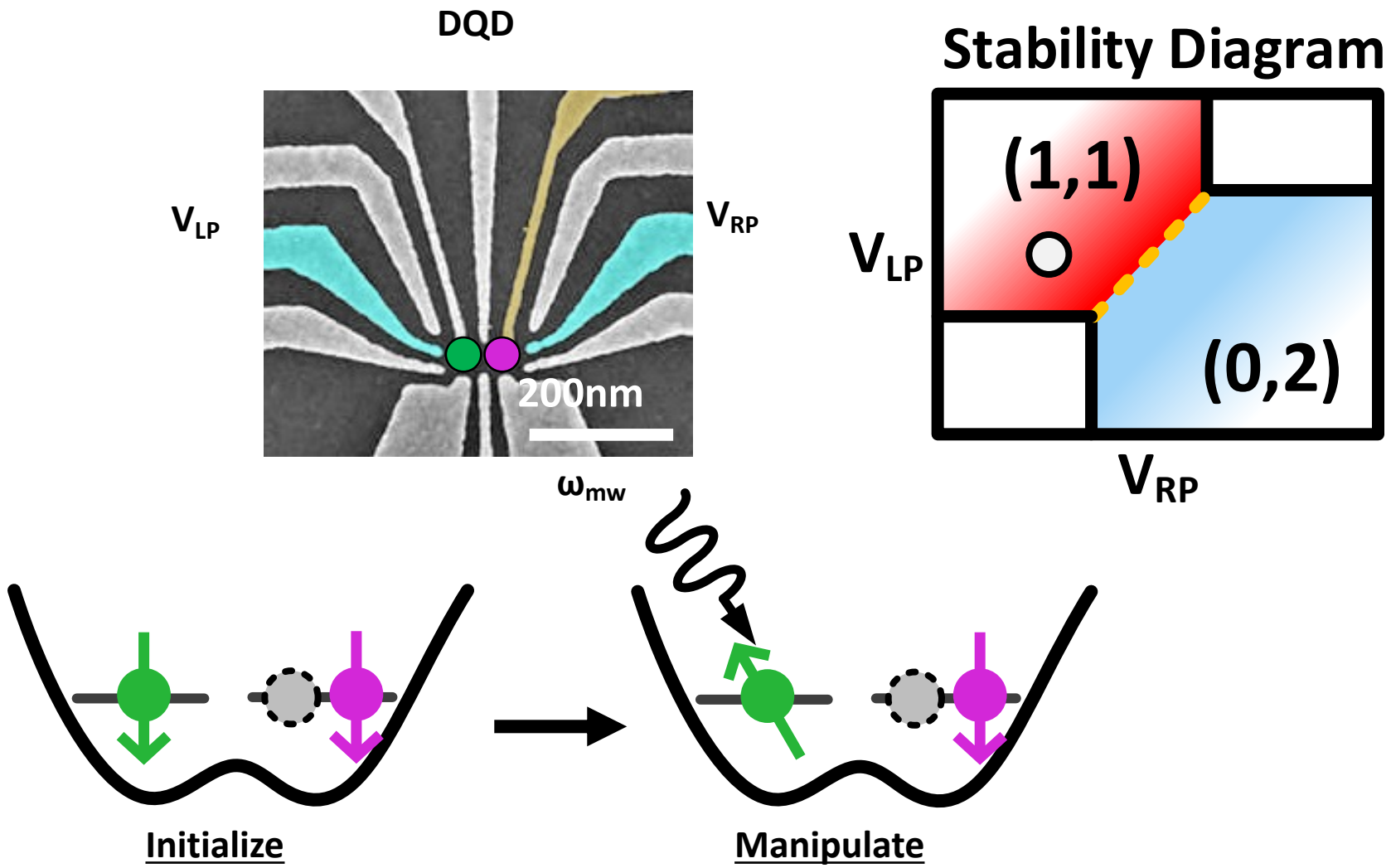


- No interaction between qubits
- Suitable for single-qubit operation

- Enabling qubit-1 and qubit-2 interaction by applying a voltage pulse on barrier gate
- Controlled-Not (CNOT)→ XOR

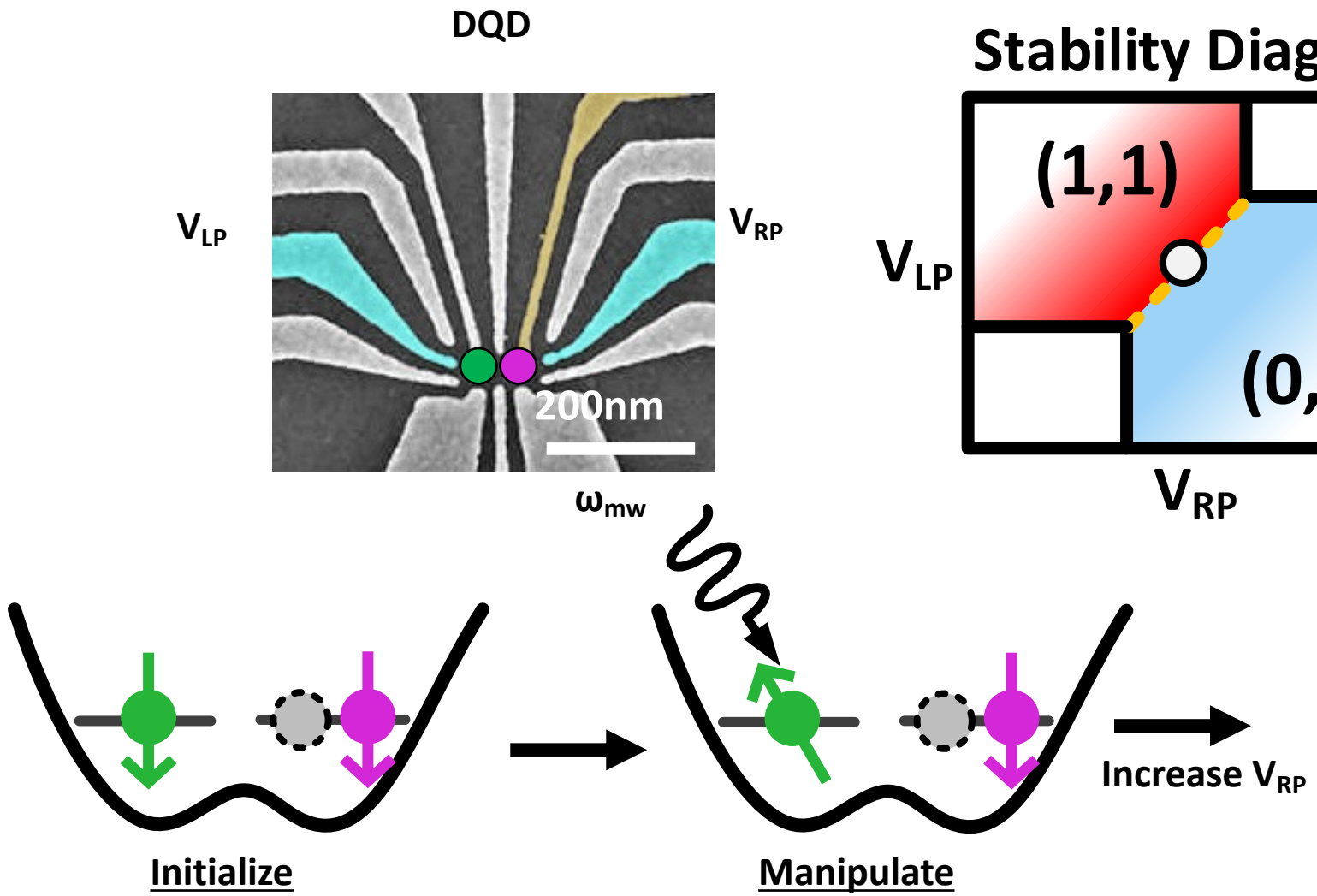
$$\begin{cases} Q_1 = |0\rangle \rightarrow Q_2 \text{ unchanged} \\ Q_1 = |1\rangle \rightarrow Q_2 \text{ flipped} \end{cases}$$

Spin Qubit Operation– Manipulation



[B. Prabowo, ISSCC'21]

Spin Qubit Operation– Readout



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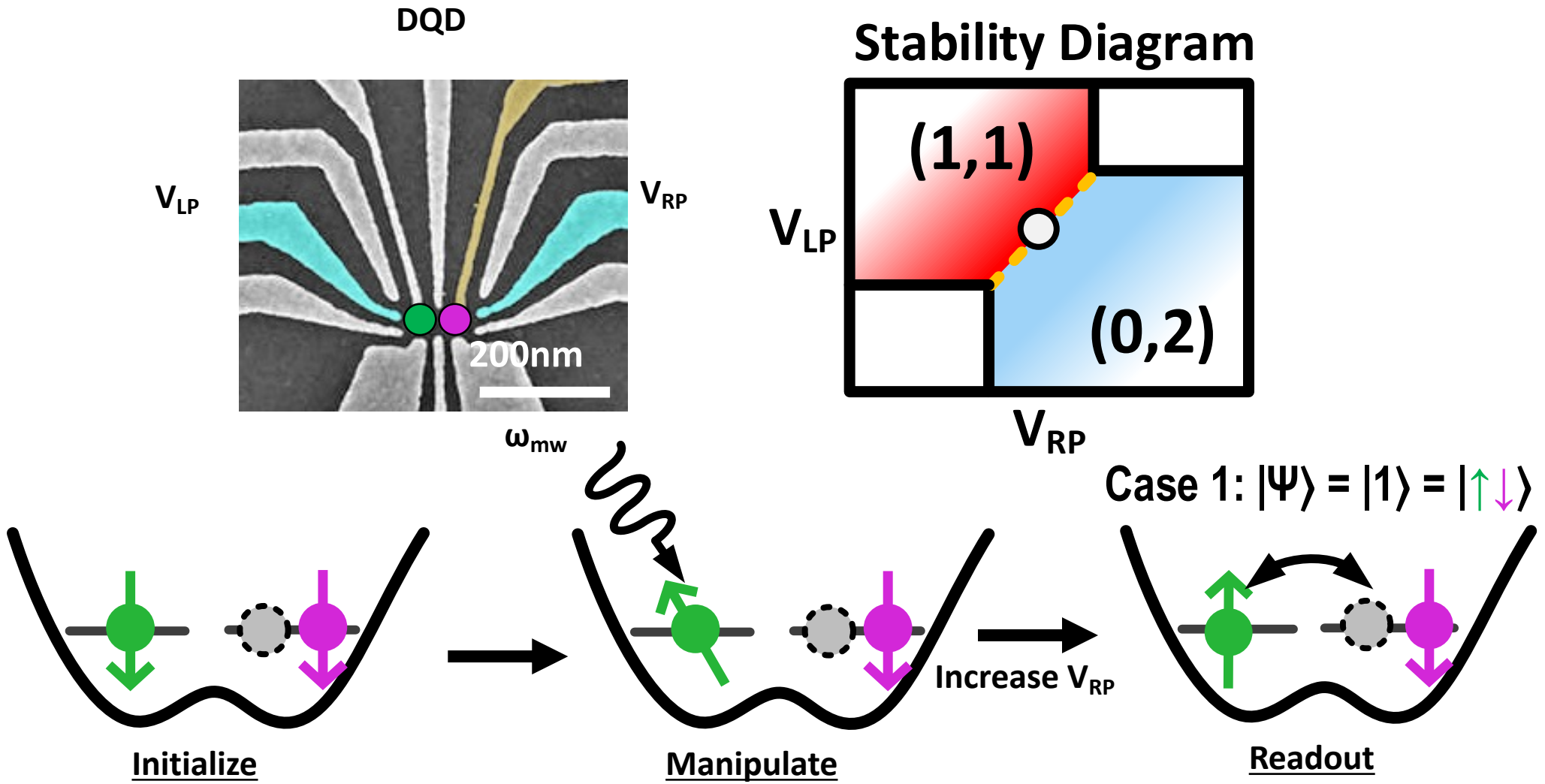

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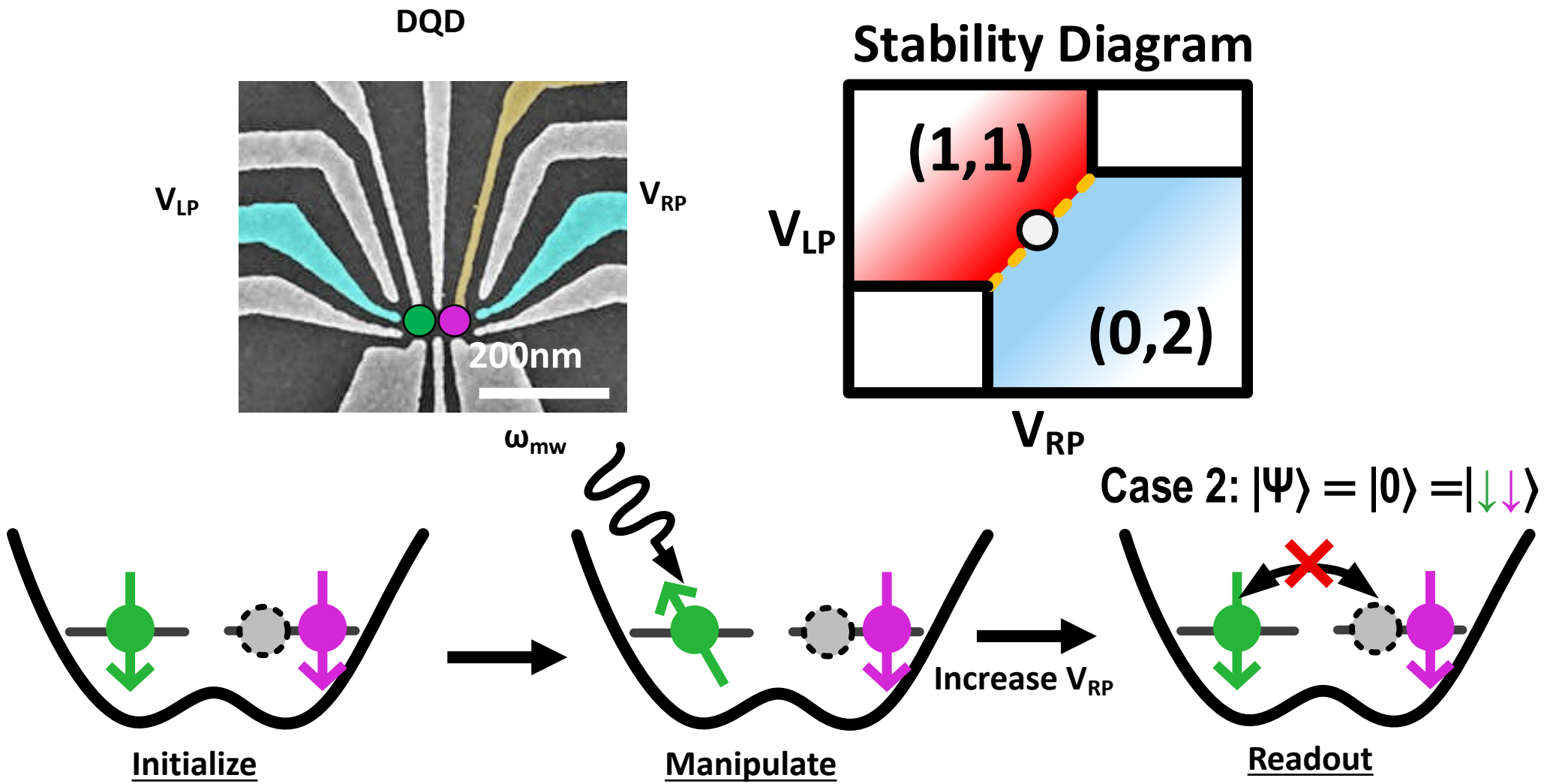

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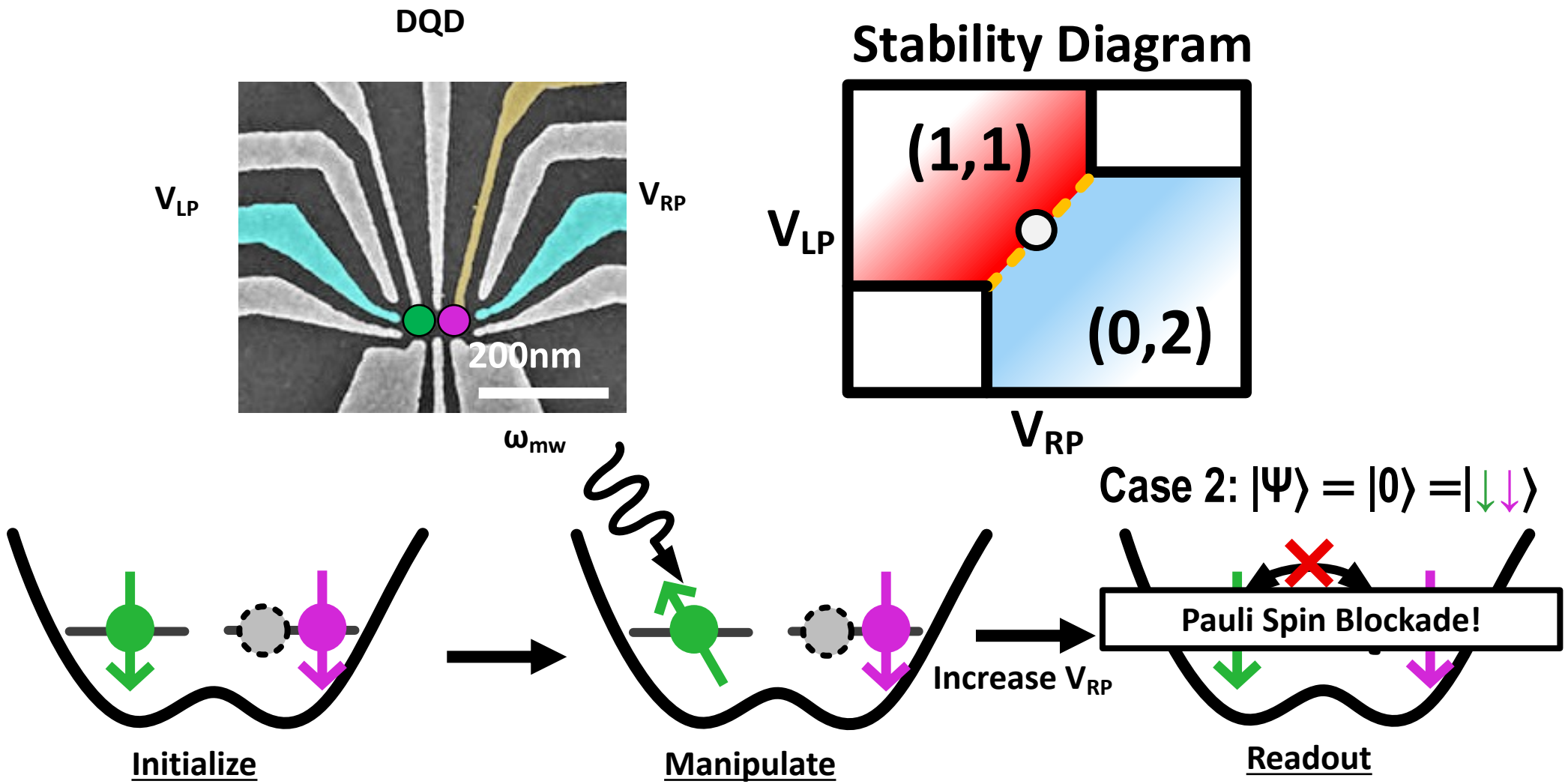
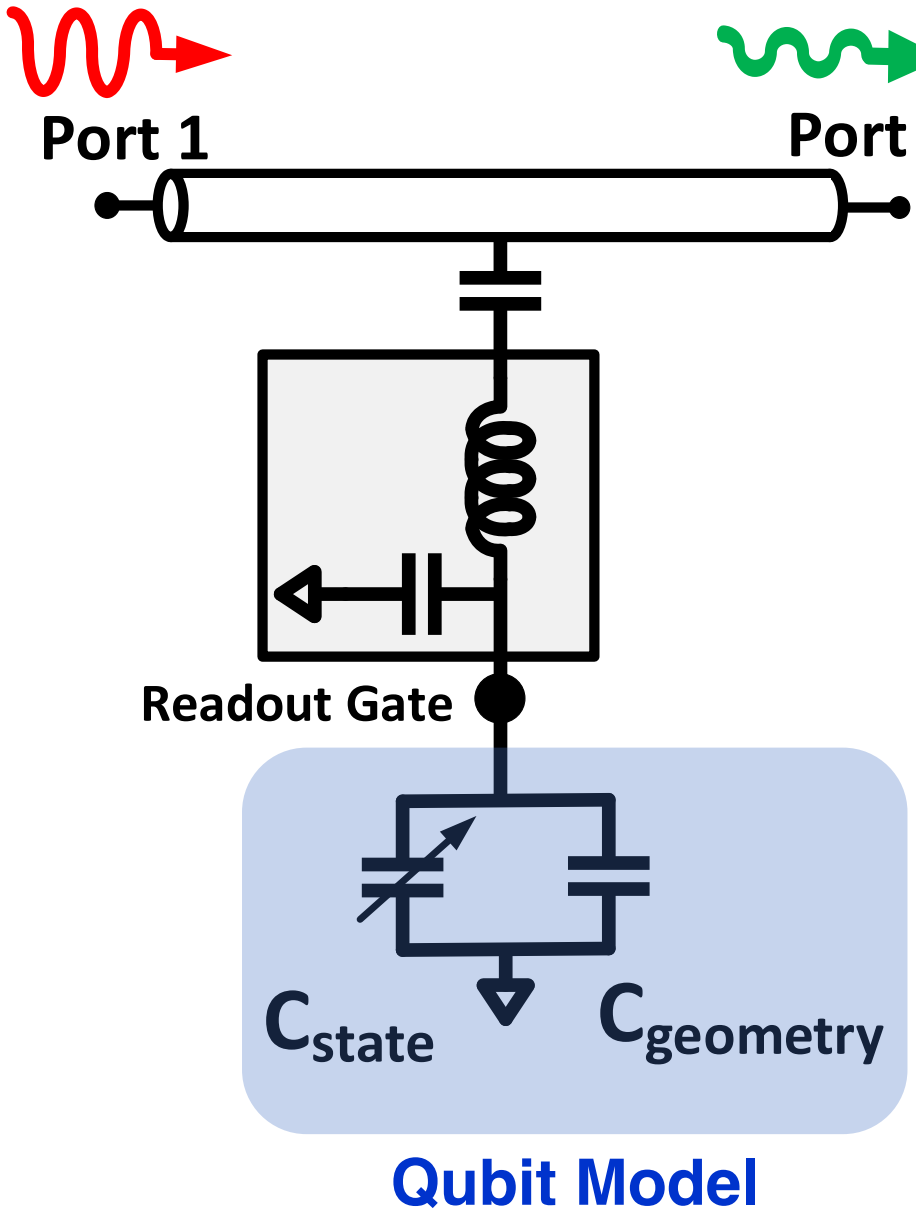
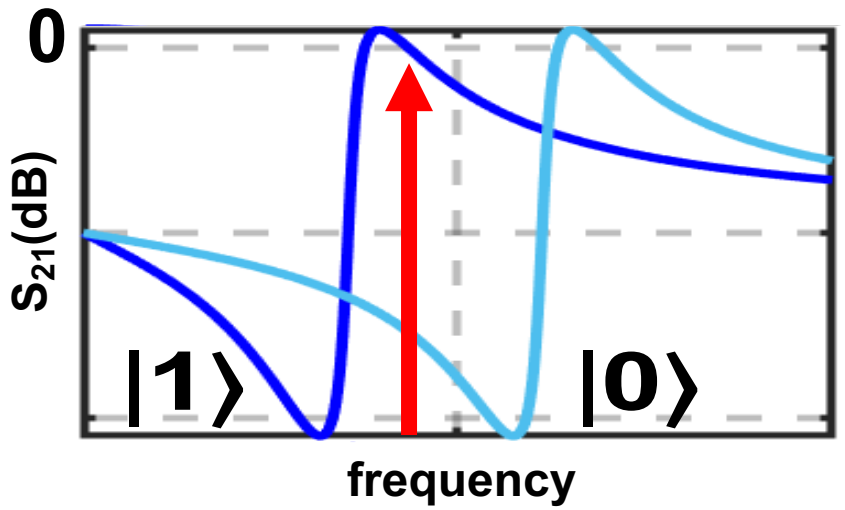
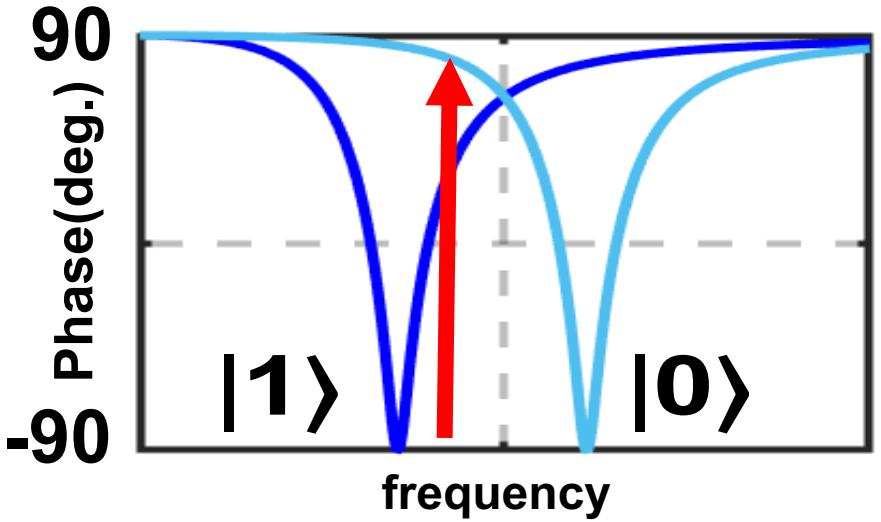


[B. Prabowo, ISSCC'21]

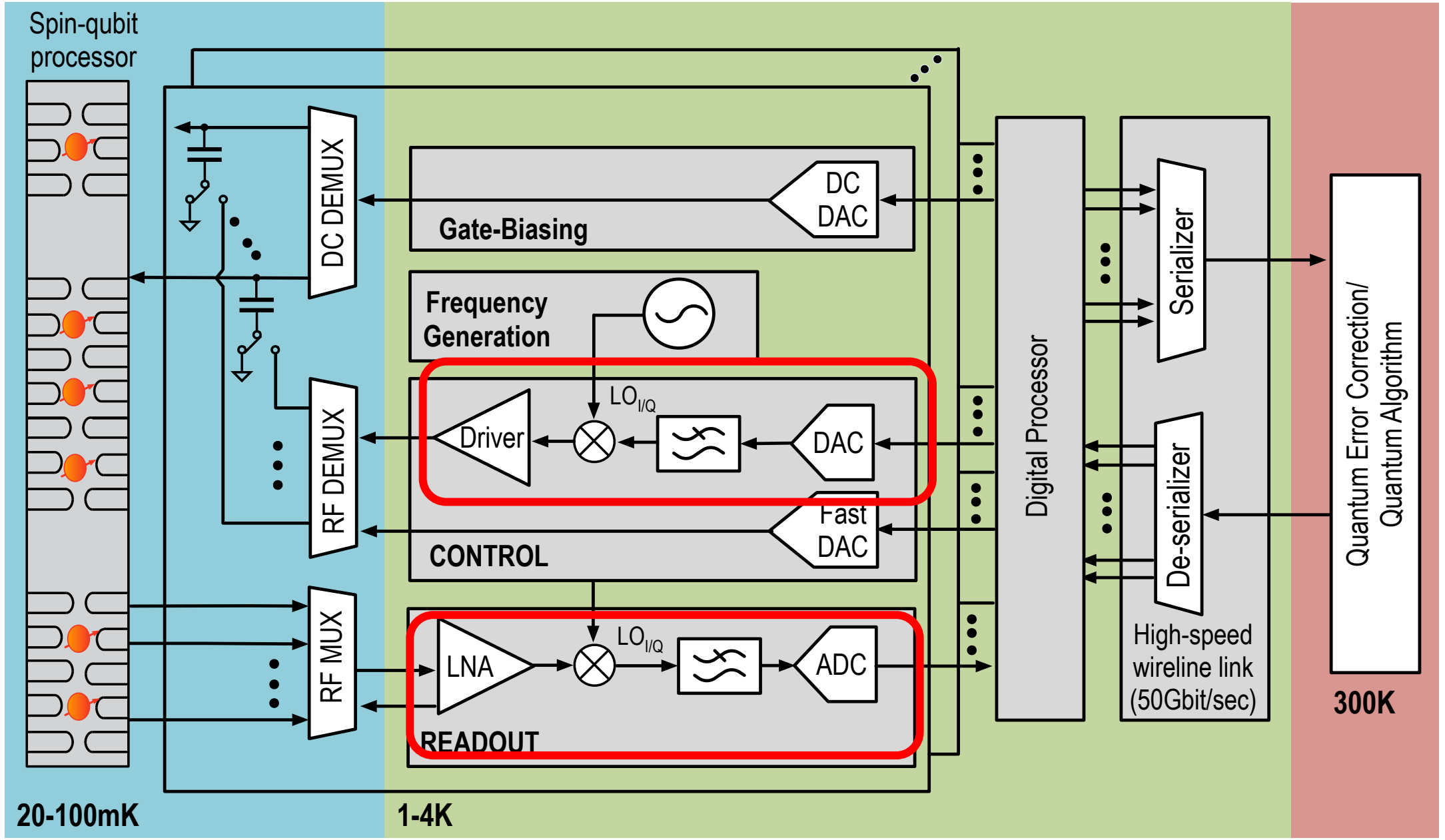
Gate-based Readout







Required Building Blocks



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Modeling: Cryo-CMOS Benefits and Constraints

	Parameter	Behavior
1	Threshold voltage	Increases by ~100mV
2	Mobility	Increases
3	Saturated velocity	Increases by 40%
4	Transconductance	increases
5	G_m/I_D in saturation	No change
6	G_m/I_D in weak-inversion	Up to 3x improvement
7	Subthreshold swing	Decreases but not proportionally to temp.
8	Leakage current	Reduces substantially
9	device output resistance	decreases by 50%
10	device intrinsic gain	Almost the same
11	Switch ON-resistance	~50% reduction

	Parameter	Behavior
12	Gate resistance	~50% reduction
13	Device parasitic cap.	Almost the same
14	f_t and f_{max}	40% increase
15	Device matching	worse
16	A_{vth}, A_β	25% increase
17	Thermal conductivity	No change (maximizes at 20K)
18	Self heating	Much more serious
19	Thermal noise	Reduces but not proportionally to temp
20	Flicker noise	Almost the same
21	Ind. & cap. value	Almost the same
22	Cap. Q-factor	3x improvement <10GHz
23	Ind. Q-factor	2.5x improvement

Emulating Qubit Behavior

$$H = (\omega_{mw} - \omega_0)\frac{\boldsymbol{\sigma_z}}{2} + \omega_R\left[\cos(\varphi)\frac{\boldsymbol{\sigma_x}}{2} - \sin(\varphi)\frac{\boldsymbol{\sigma_y}}{2}\right]$$

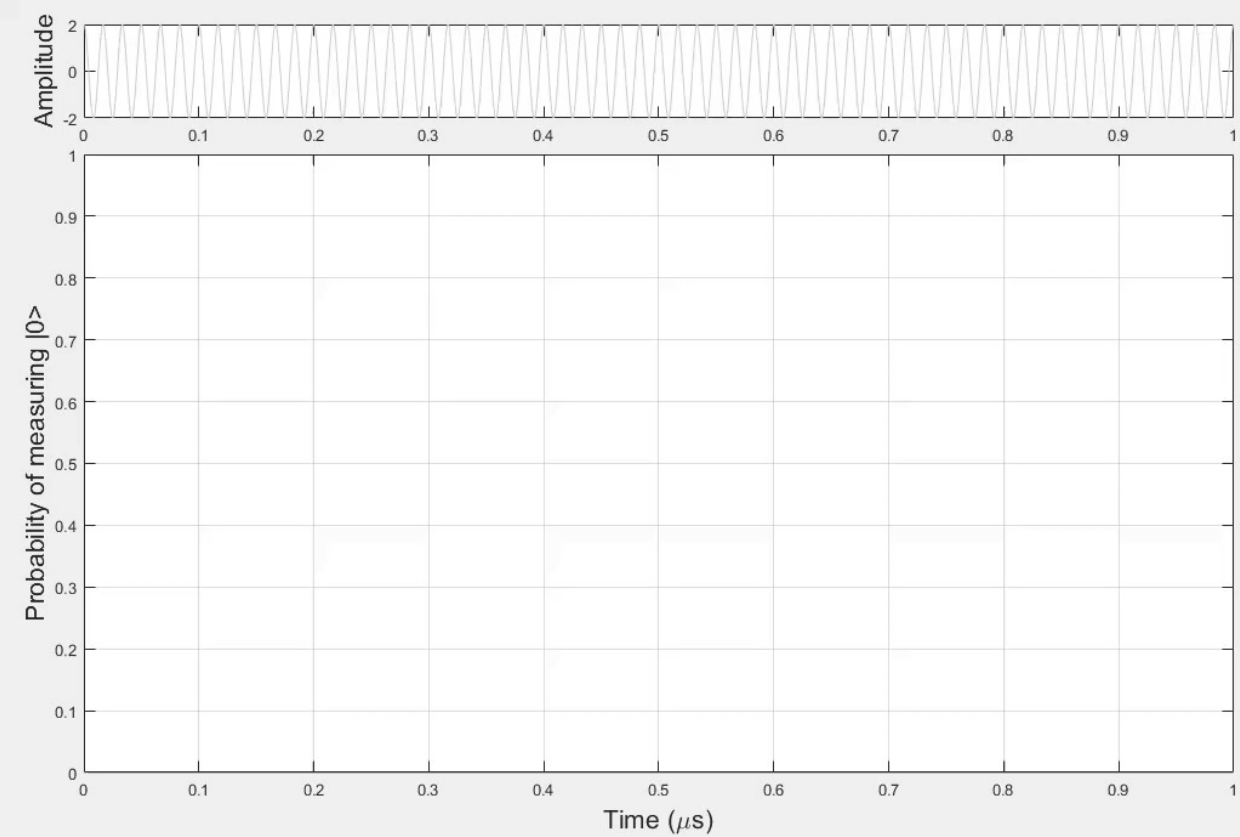
Selects the qubit (frequency)

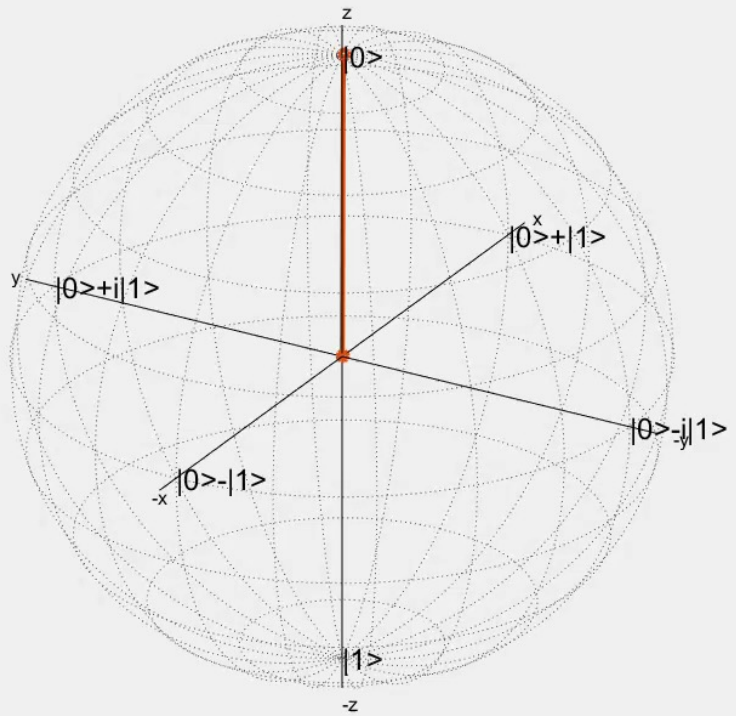
Sets the rotation speed (Amplitude)

Sets the rotation axis (X/Y) (Phase)

$$U = e^{-i\cdot H\cdot t}$$

Sets the rotation time



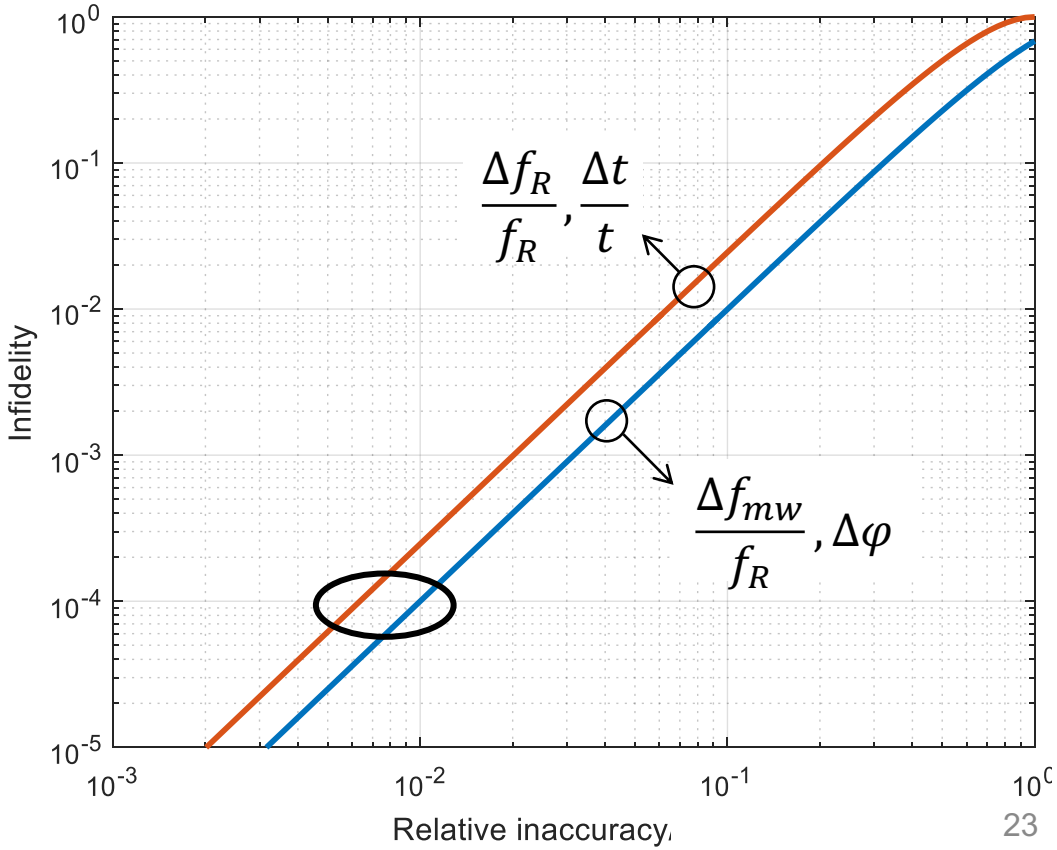


System-Level Specifications

$$H = (\omega_{mw} - \omega_0)\frac{\boldsymbol{\sigma_z}}{2} + \omega_R\left[\cos(\varphi)\frac{\boldsymbol{\sigma_x}}{2} - \sin(\varphi)\frac{\boldsymbol{\sigma_y}}{2}\right] \qquad U = e^{-i\cdot H\cdot t}$$

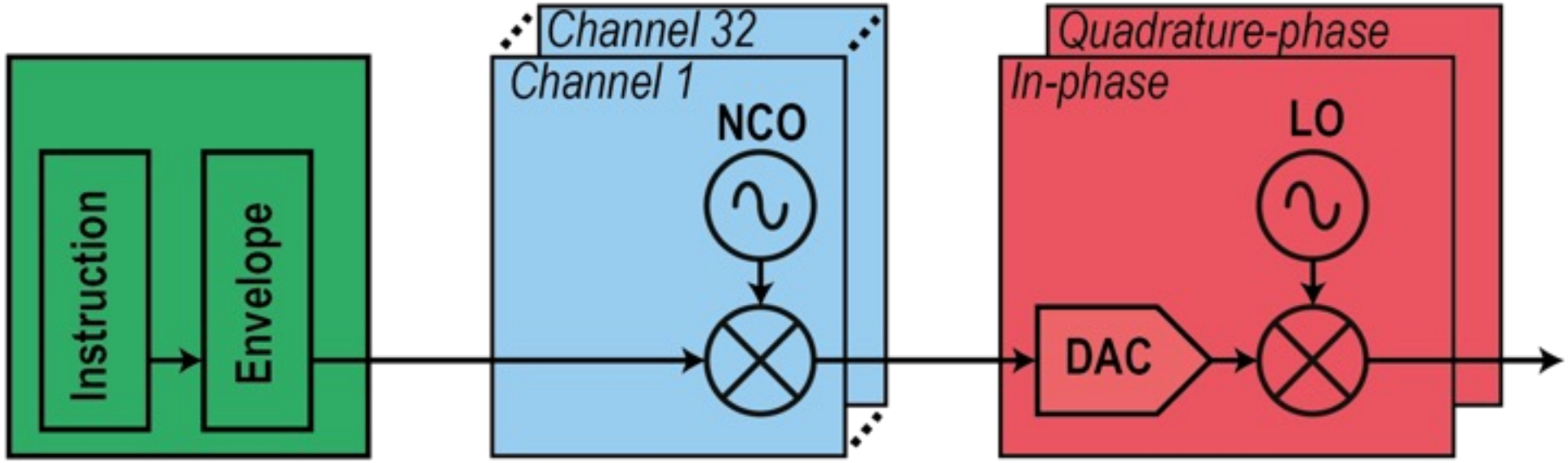
- ω_{mw}: Selects the qubit (frequency)
- ω_R: Sets the rotation speed (Amplitude)
- φ: Sets the rotation axis (X/Y) (Phase)
- t: Sets the rotation time

Frequency noise/inaccuracy $F = 1 - \left(\frac{1-\cos(\theta)}{2}\right)\left(\frac{\Delta f_{mw}}{f_R}\right)^2$	**Amplitude noise/inaccuracy** $F = 1 - \left(\frac{\theta}{2}\right)^2\left(\frac{\Delta f_R}{f_R}\right)^2$
Phase noise/inaccuracy $F = 1 - \left(\frac{1-\cos(\theta)}{2}\right)(\Delta\varphi)^2$	**Timing jitter/inaccuracy** $F = 1 - \left(\frac{\theta}{2}\right)^2\left(\frac{\Delta t}{T_{pulse}}\right)^2$



[J. P. G. van Dijk, PRA'19]

Controller Architecture

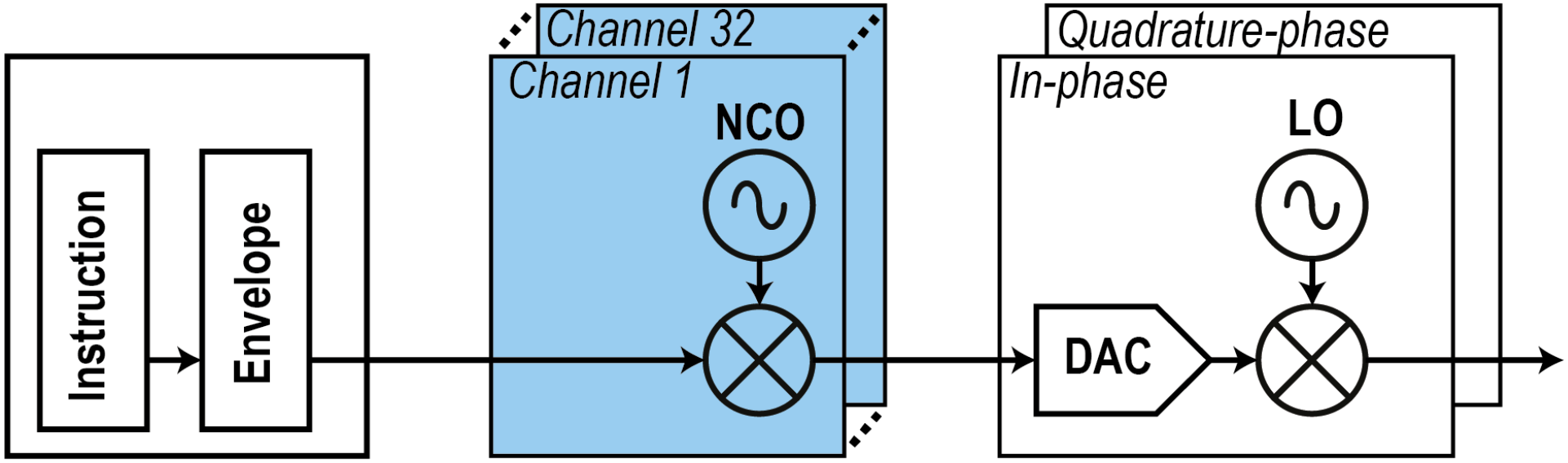


Digital Controller

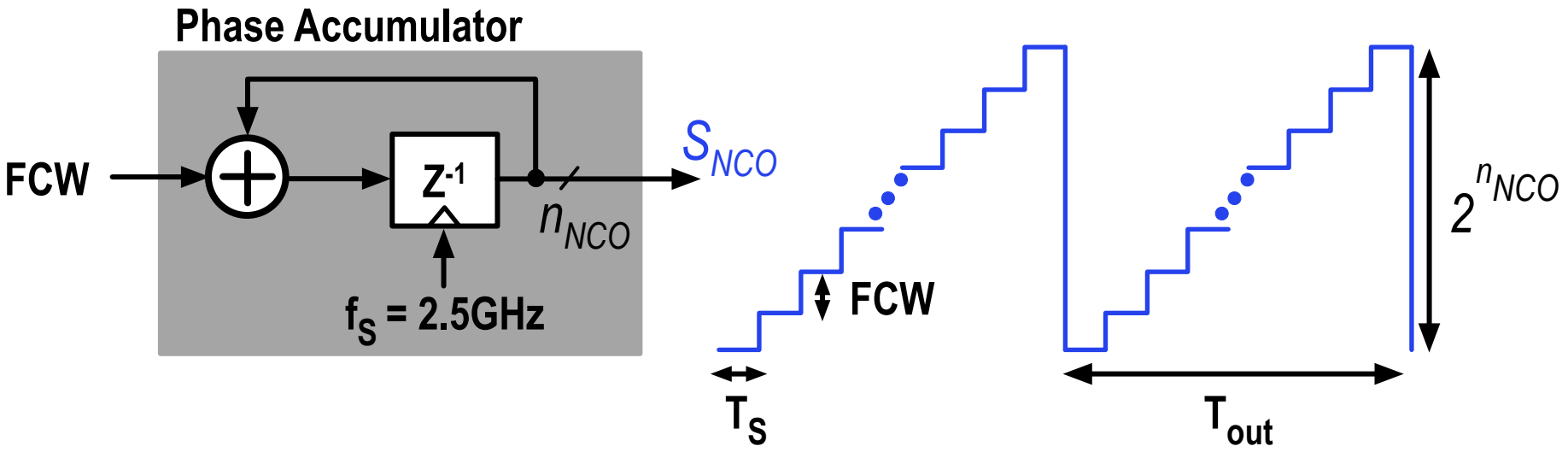
Digital Signal Generation

Single-Sideband Transmitter

Controller Architecture



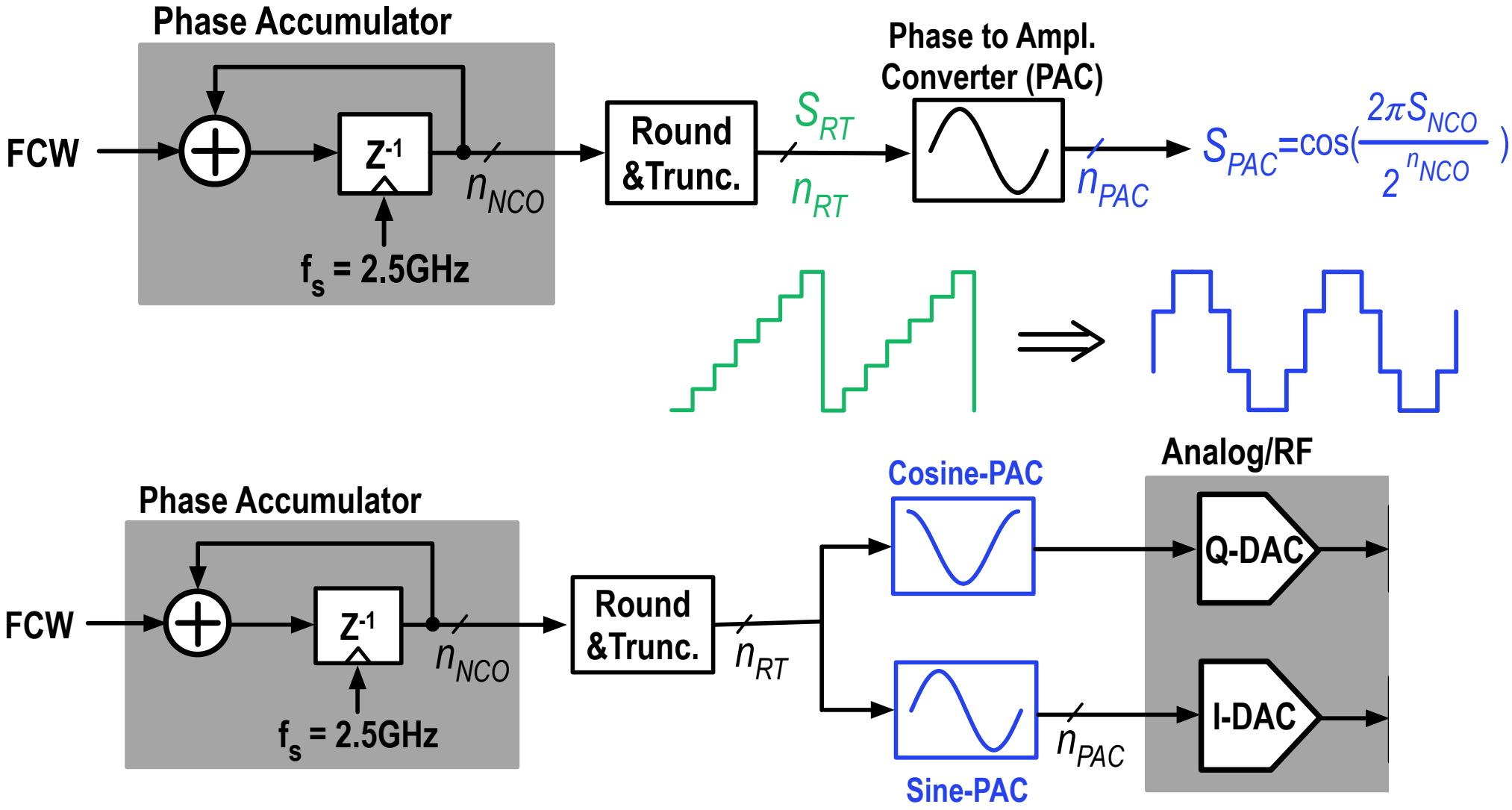
Numerically-Controlled Oscillator (NCO)



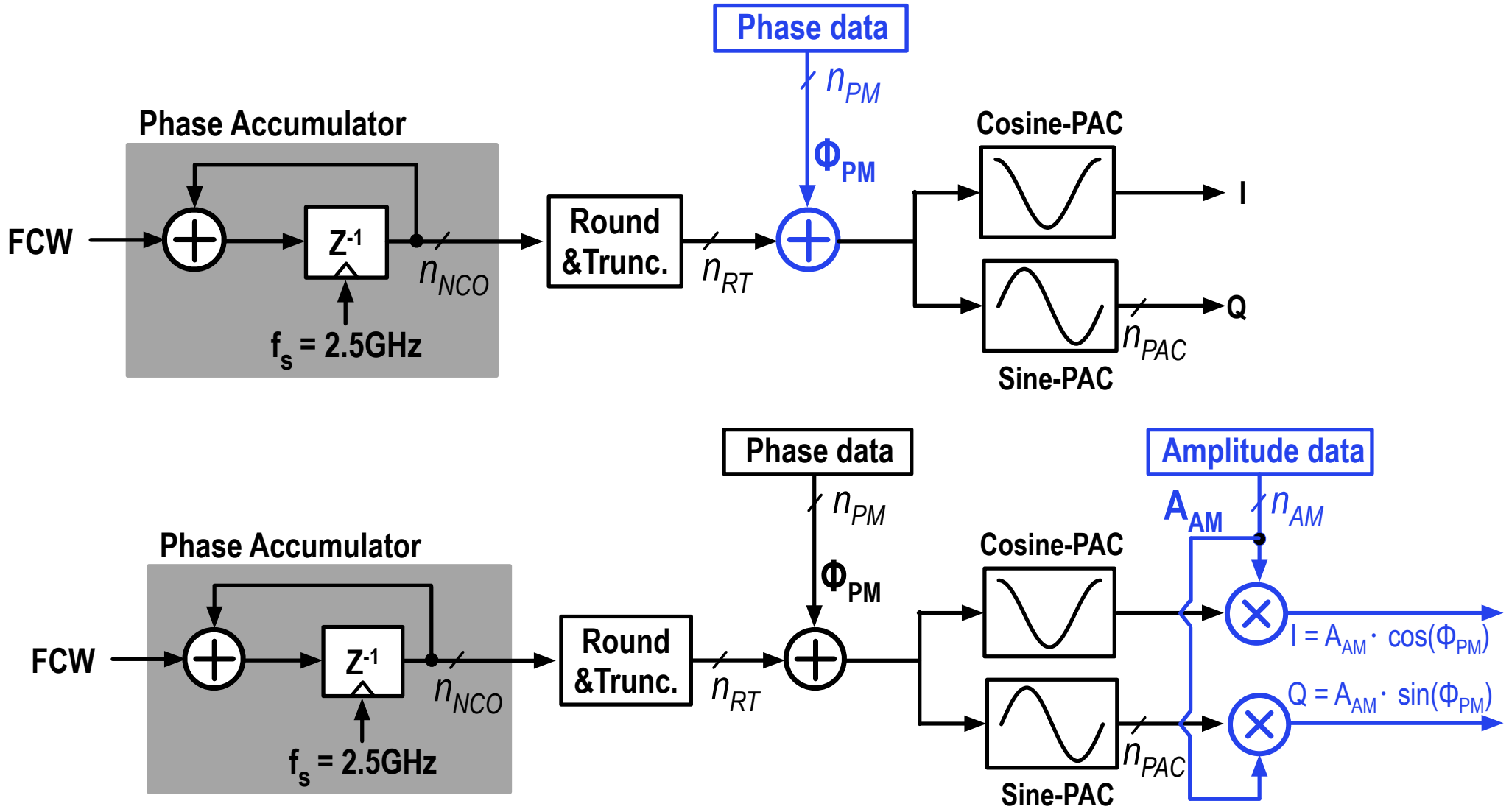
- Output frequency→ $f_{out} = FCW \cdot \frac{f_s}{2^{n_{NCO}}}$
- Frequency resolution→ $f_{res} = \frac{f_s}{2^{n_{NCO}}}$

$$n_{NCO} > \log_2 \frac{f_s}{2f_R\sqrt{1-F}} \xrightarrow{F=99.99\%, f_R=1MHz} \boxed{n_{NCO} \geq 17 - \text{bit}}$$

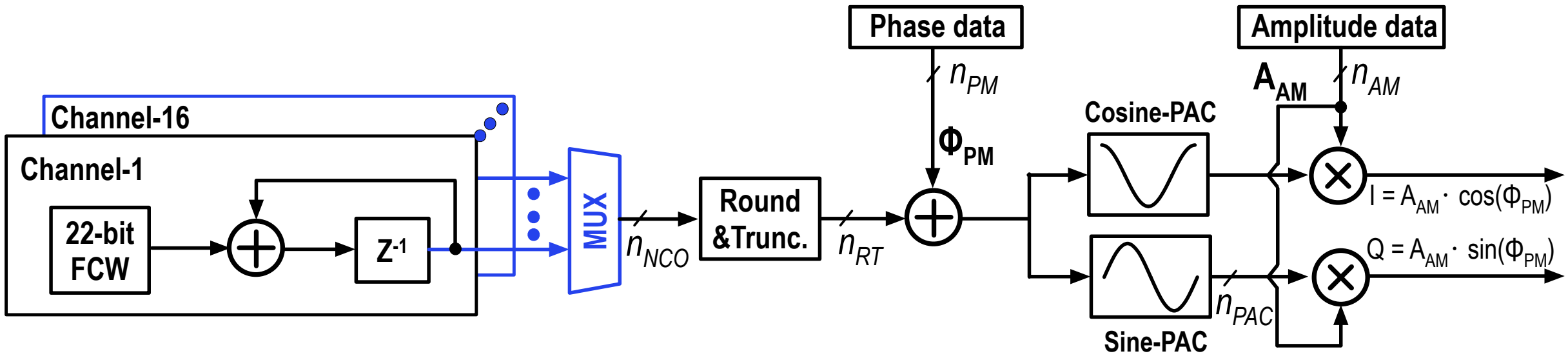
Phase-to-Amplitude Conversion



Need for Amplitude & Phase Modulation

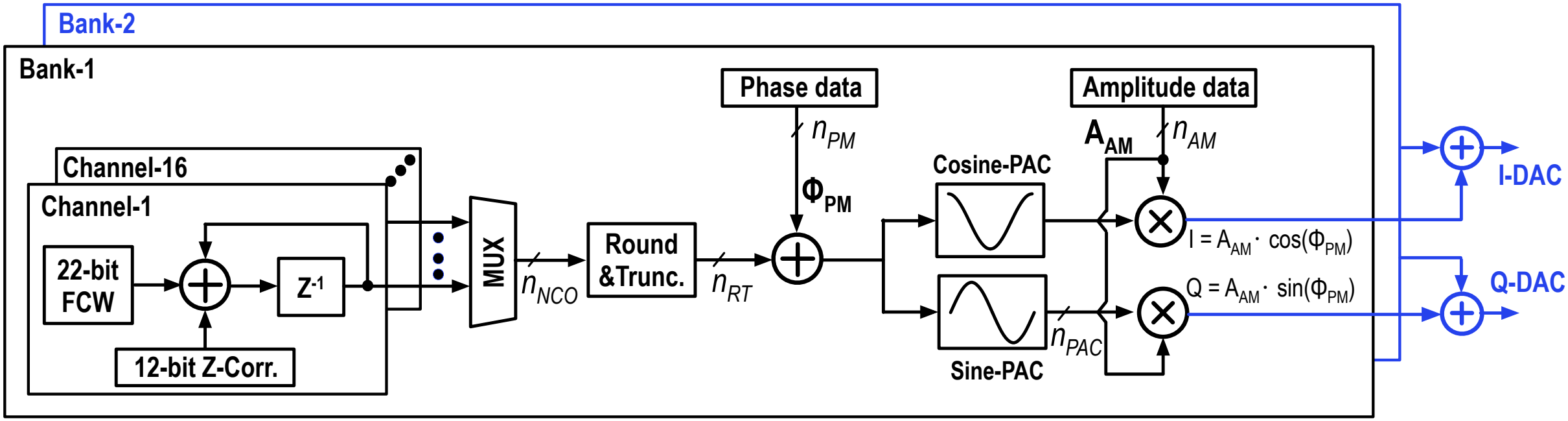


Deriving Frequency Multiplexed Qubits



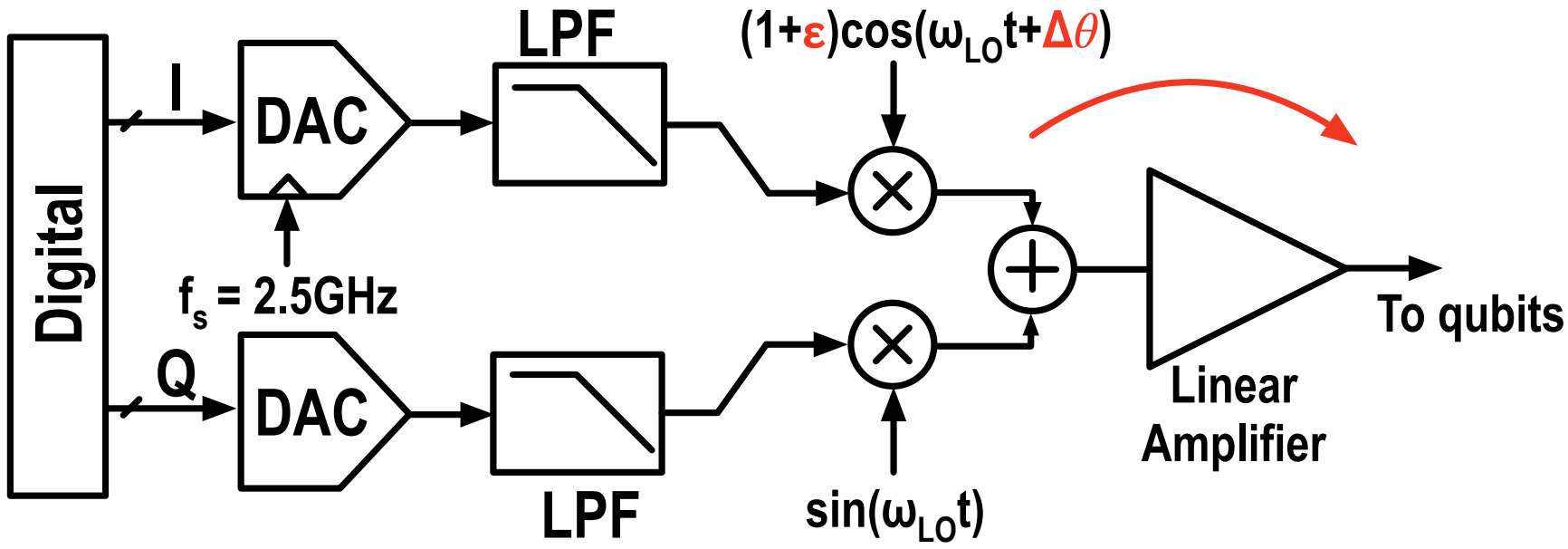
- Intermittent sequential operations on any qubit demand keeping track of the phase of all qubits.
- Consequently, an individual reference clock would be required for each qubit.
- NCO outputs are time-multiplexed to allow operation on one qubit at a time to reduce system.

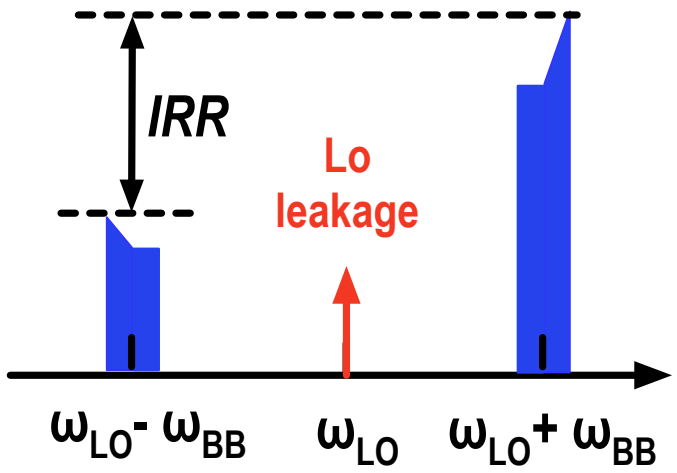
Simultaneous Qubit Operation



- Corresponding signal of two qubits can be generated simultaneously.

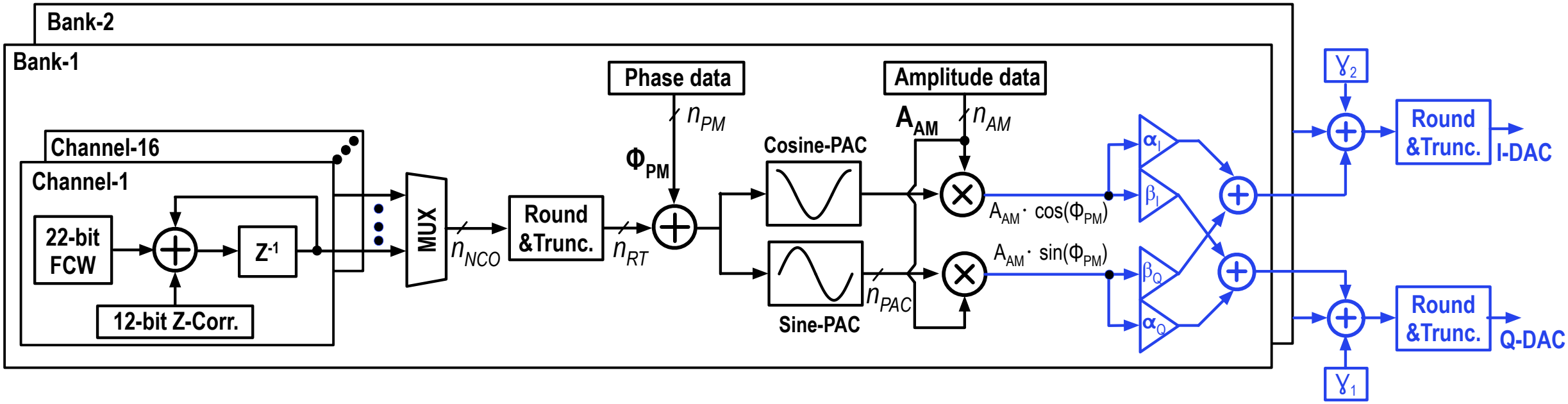
LO Feedthrough and Image Problems





$$IIR \approx \frac{4}{\epsilon^2 + \Delta\theta^2} \xrightarrow{IIR \gg 50dB} \begin{cases} \Delta\theta \ll 0.3^\circ \\ \epsilon \ll 0.5\% \end{cases}$$

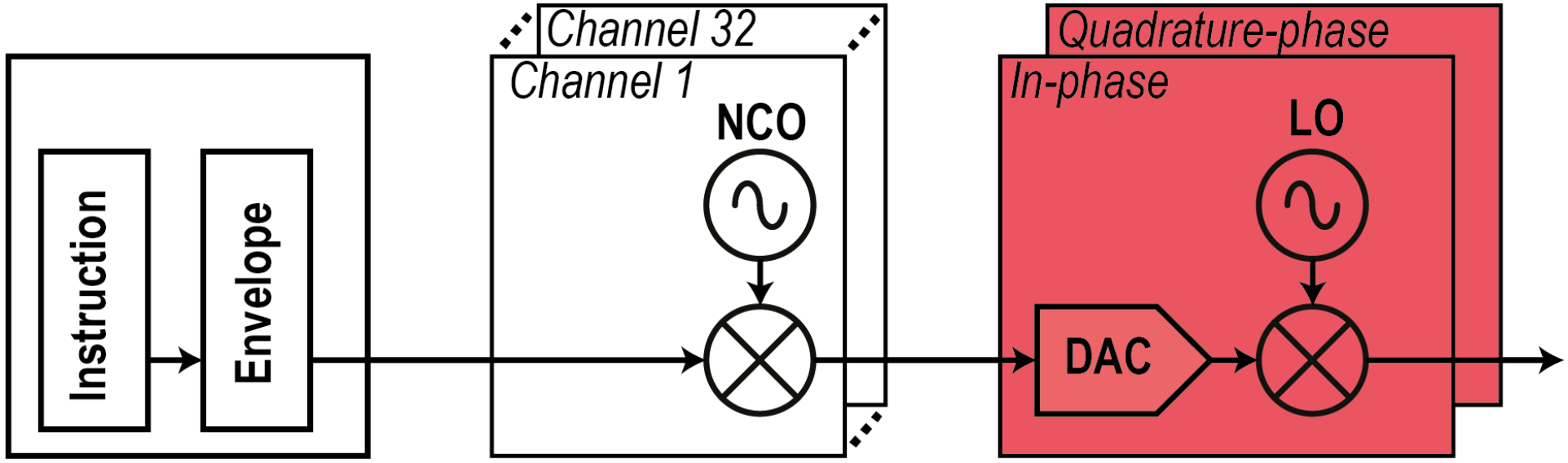
LO Feedthrough and Image Cancellation



- α_I and α_Q for compensating for gain imbalance.
- β_I and β_Q for compensating for phase imbalance.
- γ_I and γ_Q for cancelling LO leakage.

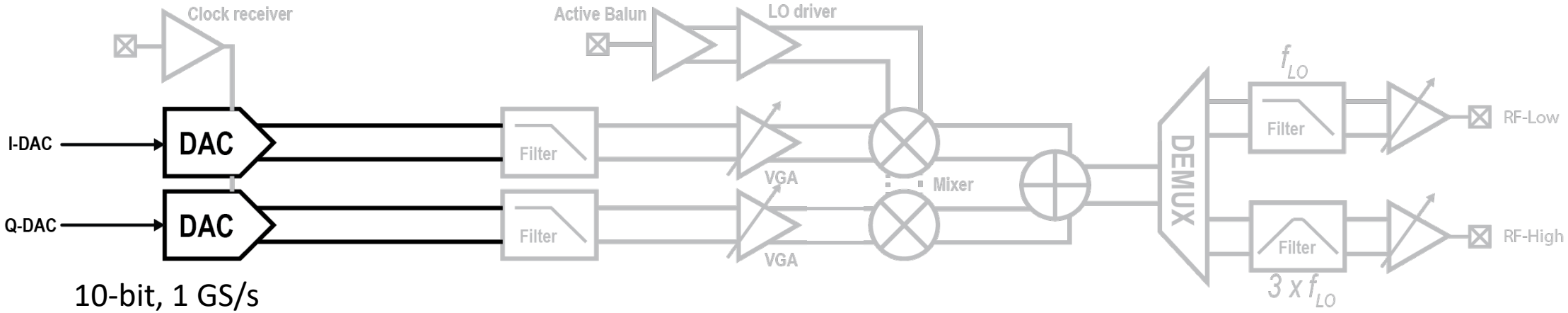
[B. Patra, ISSCC'20]

System Architecture

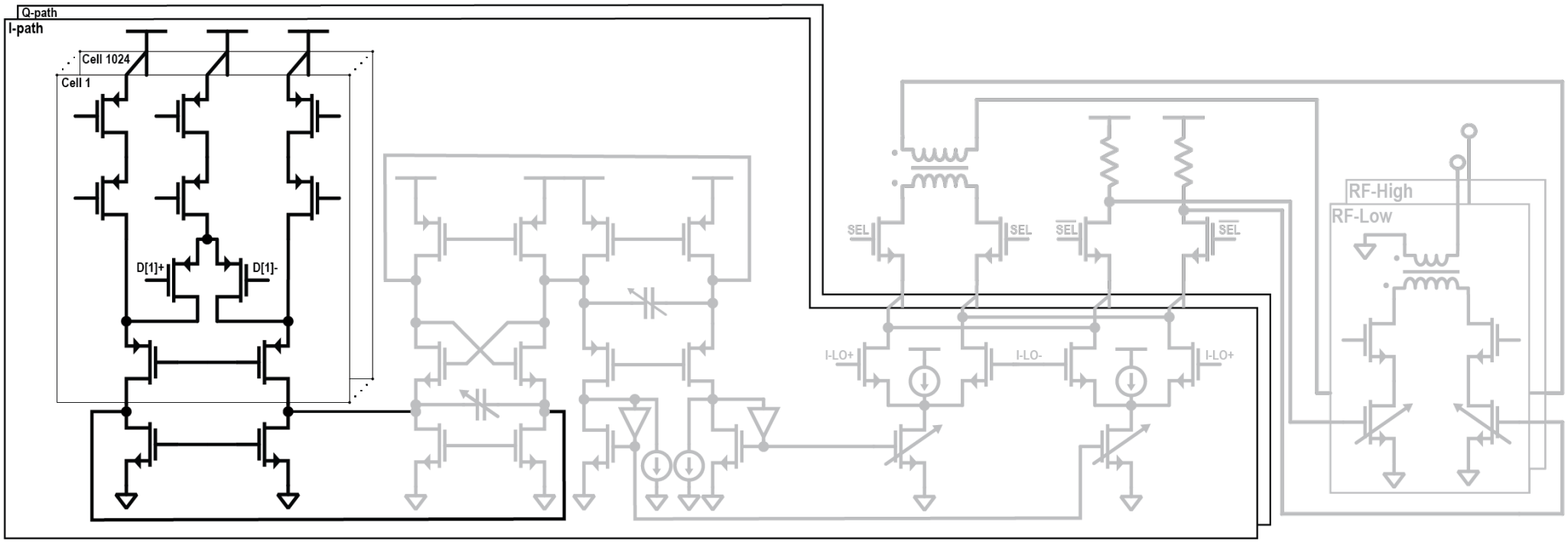


[B. Patra, ISSCC'20]

Single-Sideband Transmitter

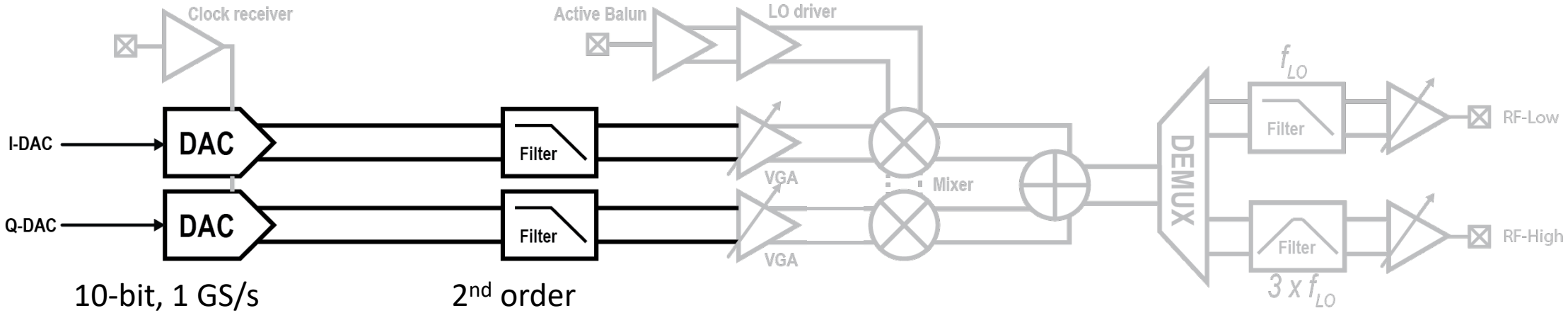


10-bit, 1 GS/s



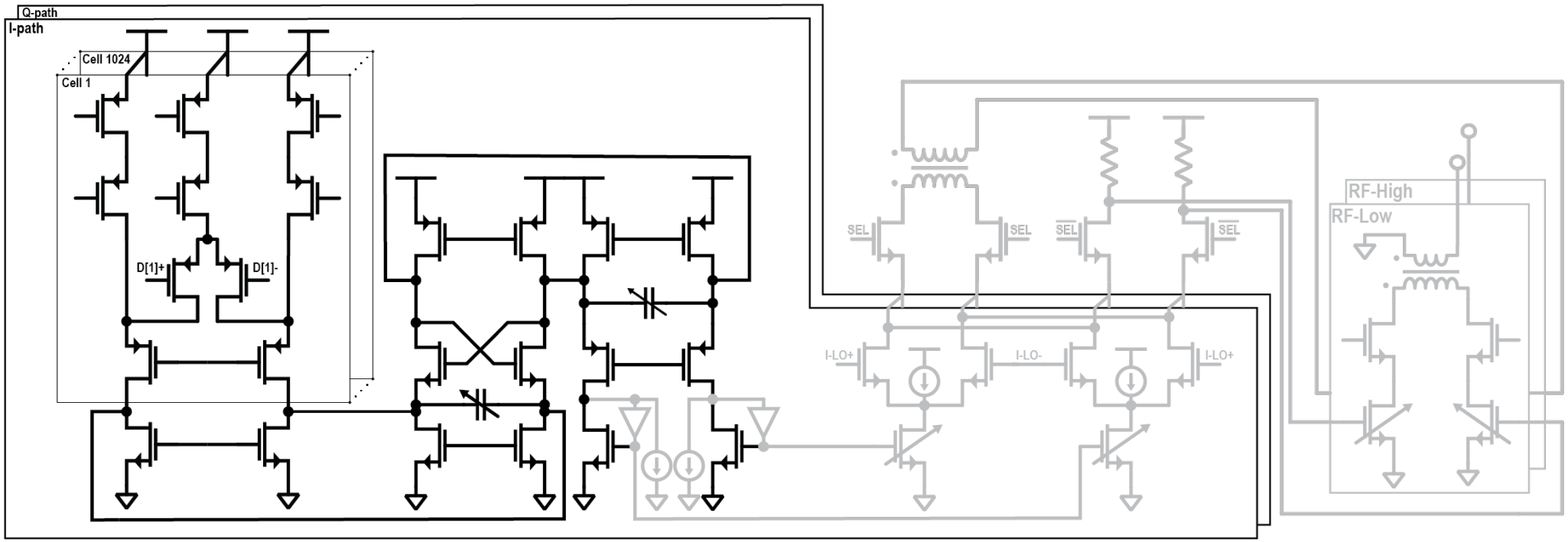
[B. Patra, ISSCC'20]

Single-Sideband Transmitter



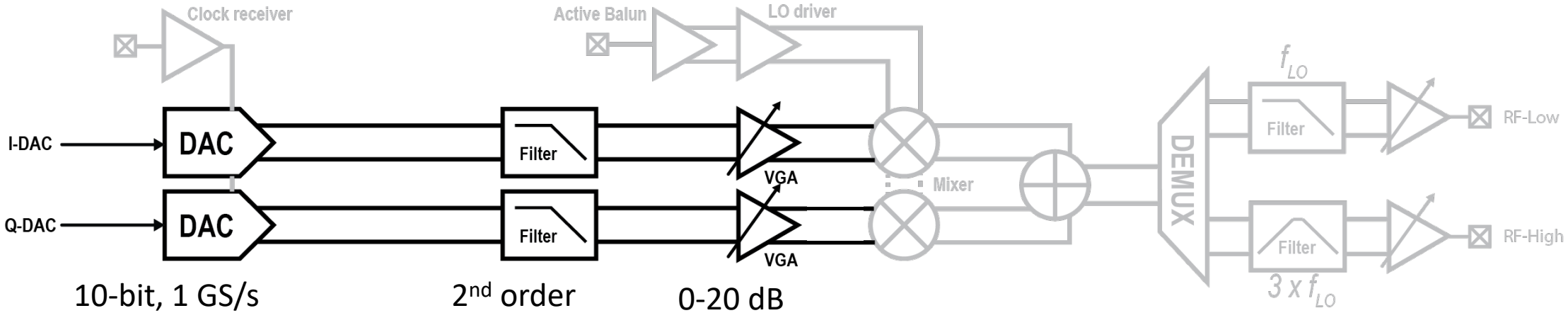
10-bit, 1 GS/s

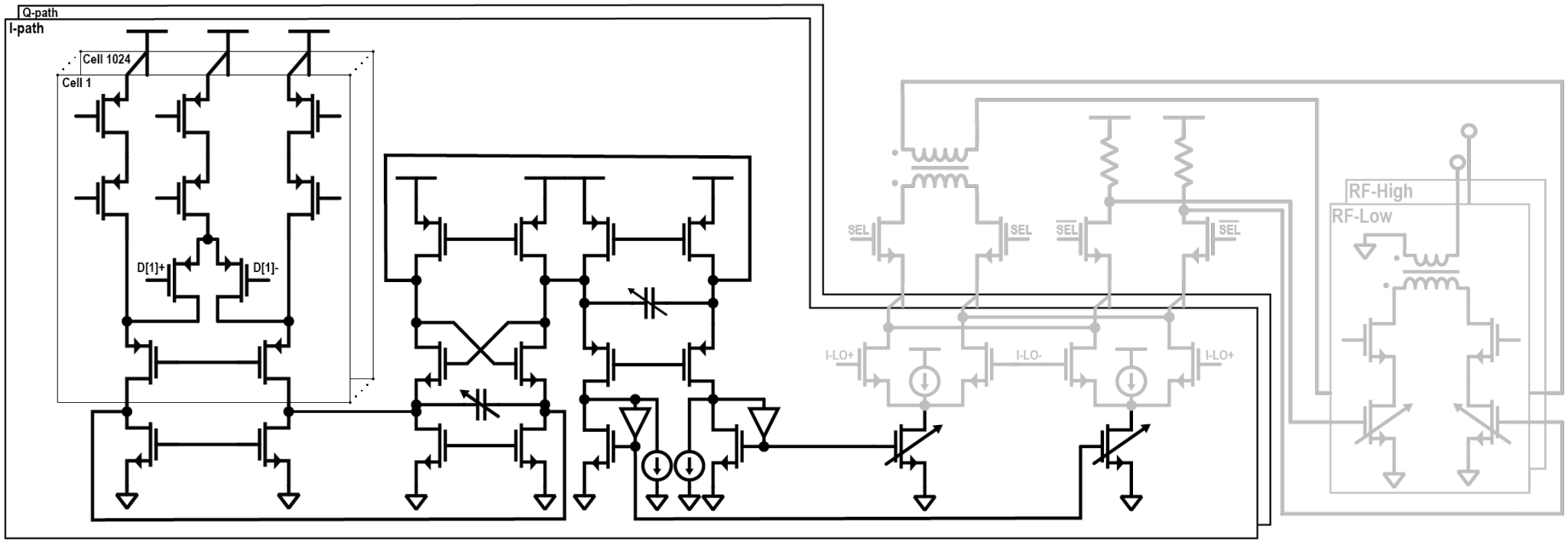
2nd order



[B. Patra, ISSCC'20]

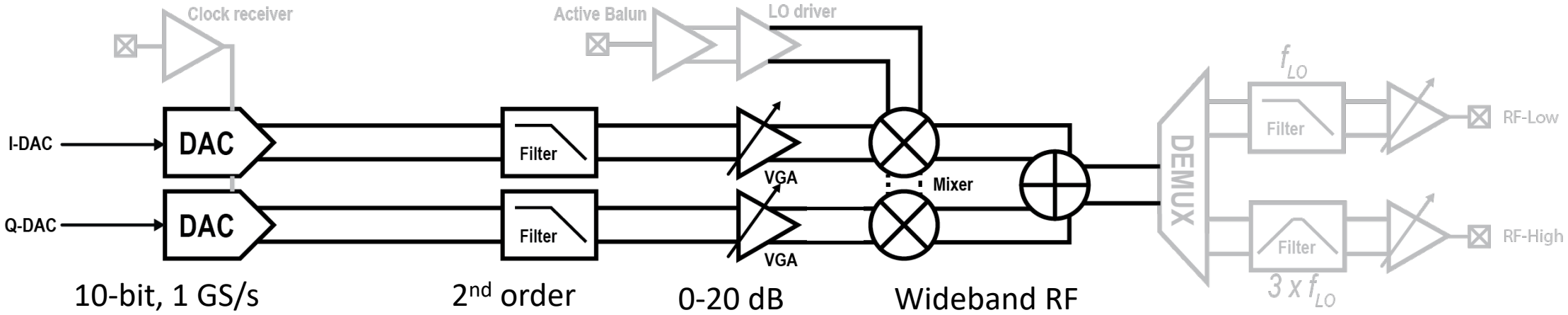
Single-Sideband Transmitter

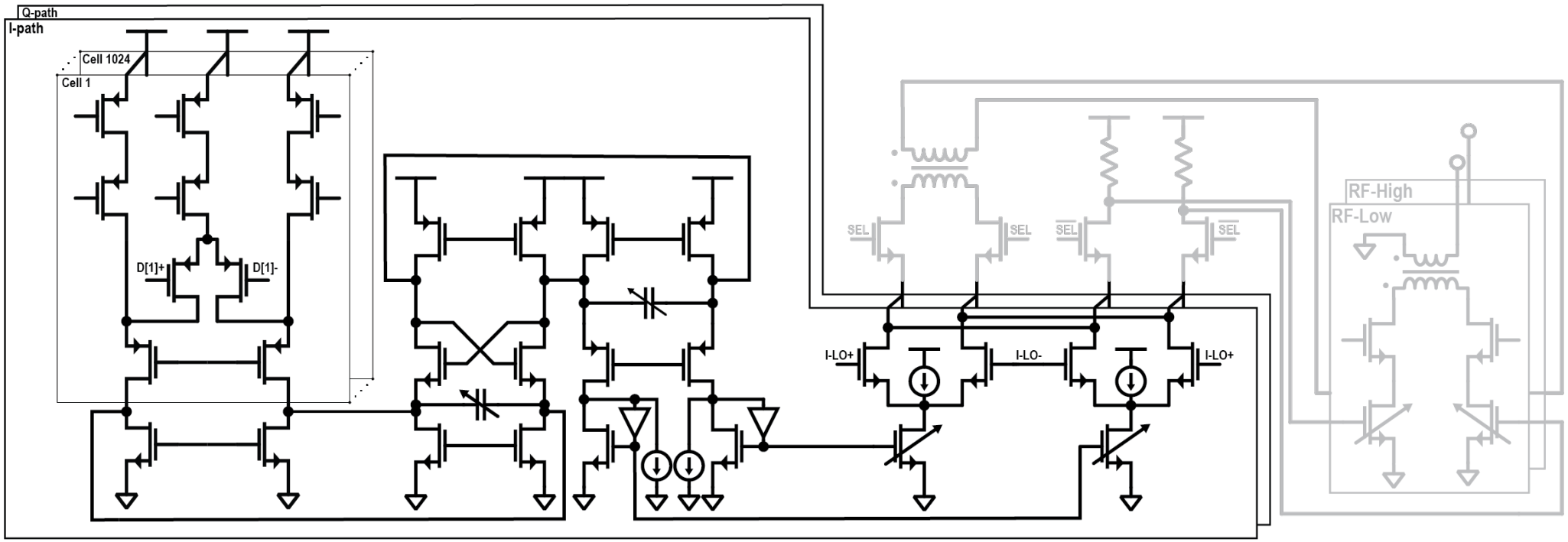




[B. Patra, ISSCC'20]

Single-Sideband Transmitter





[B. Patra, ISSCC'20]

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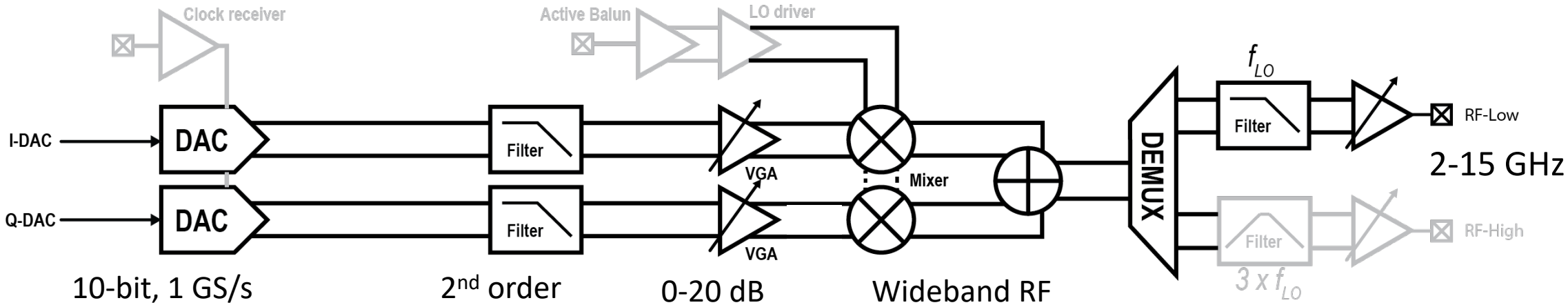
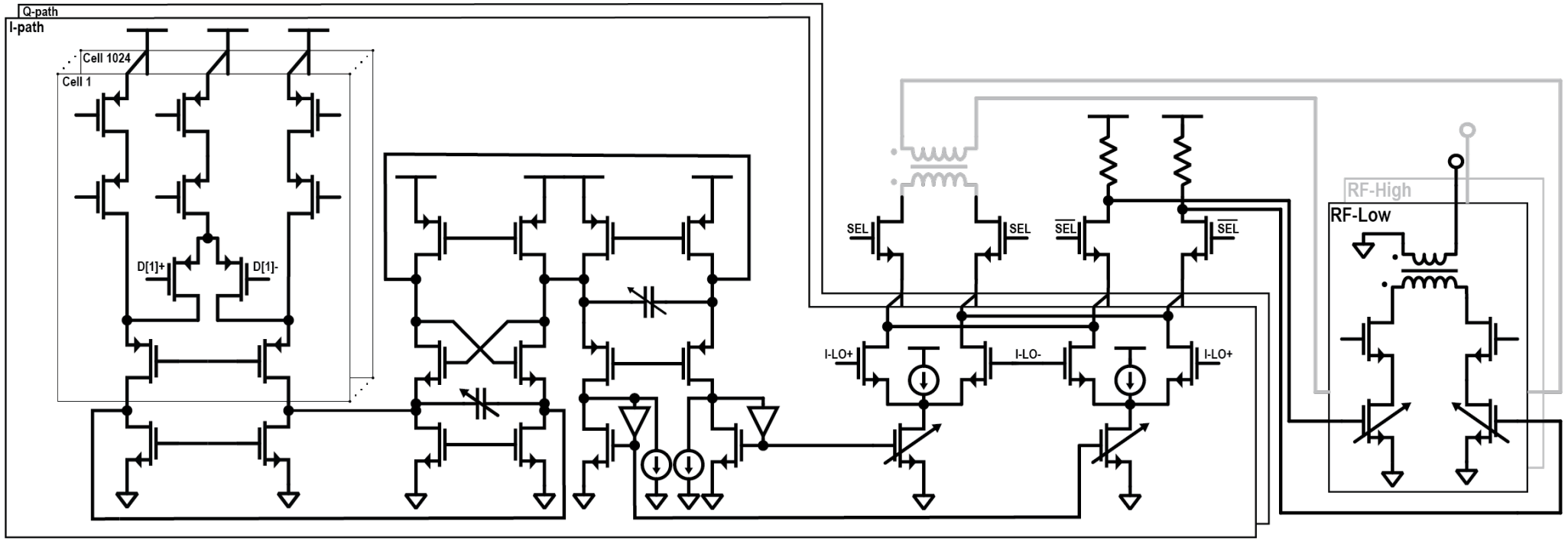
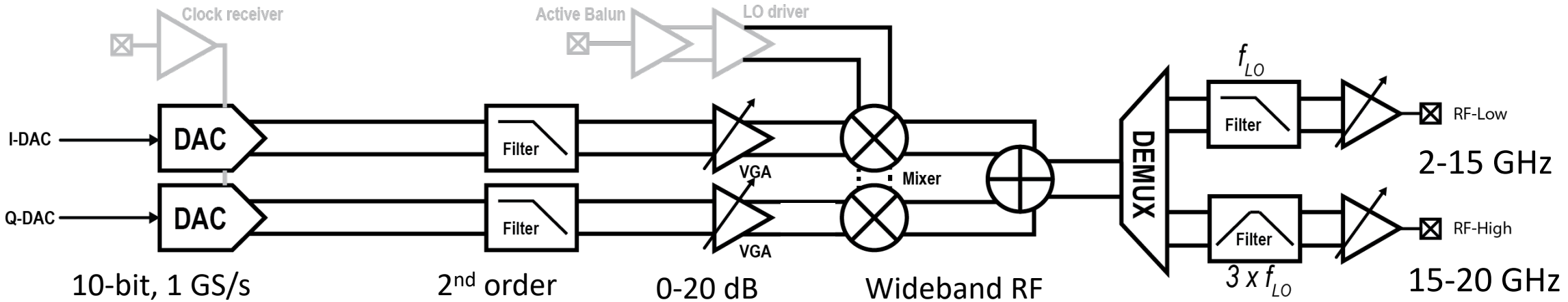
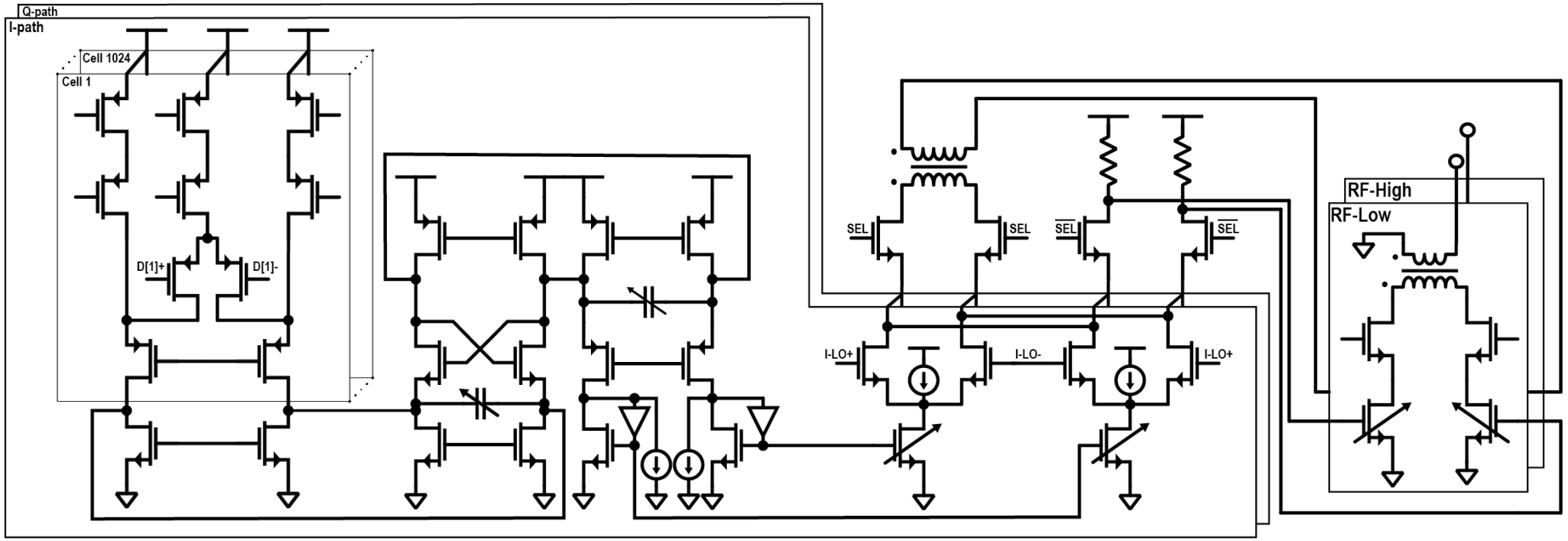




[B. Patra, ISSCC'20]

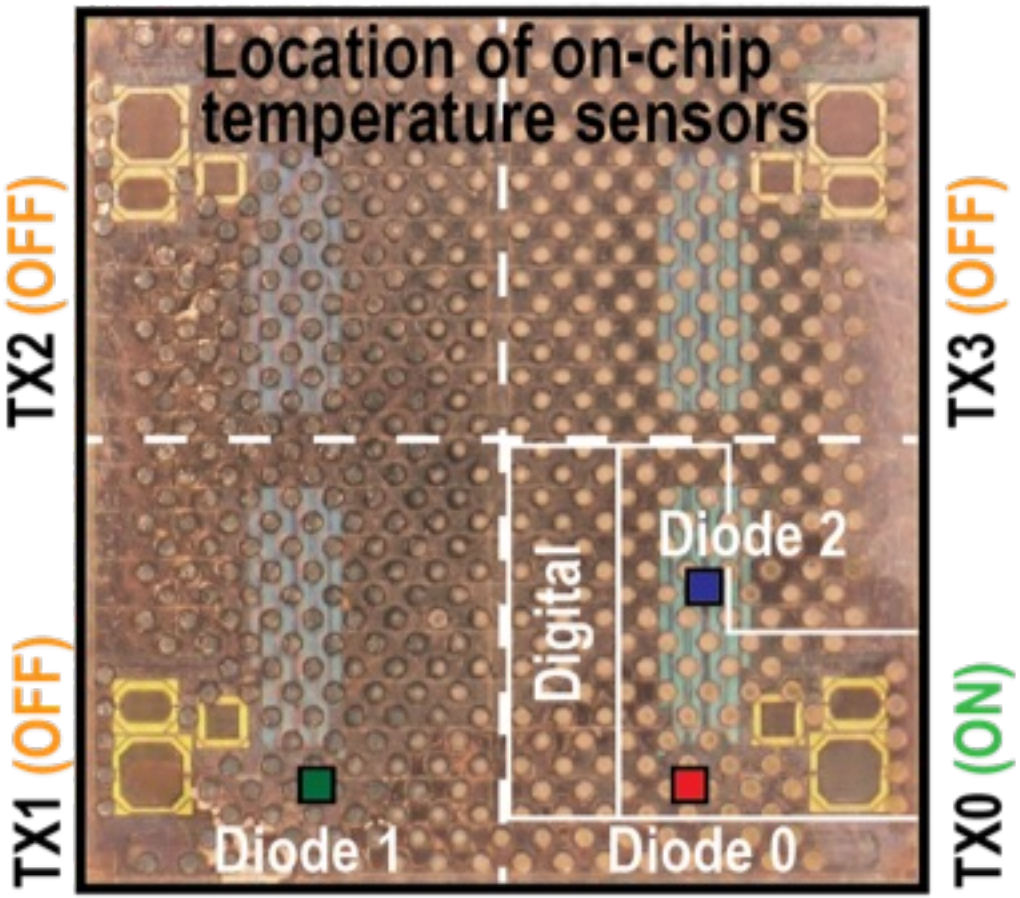
Single-Sideband Transmitter

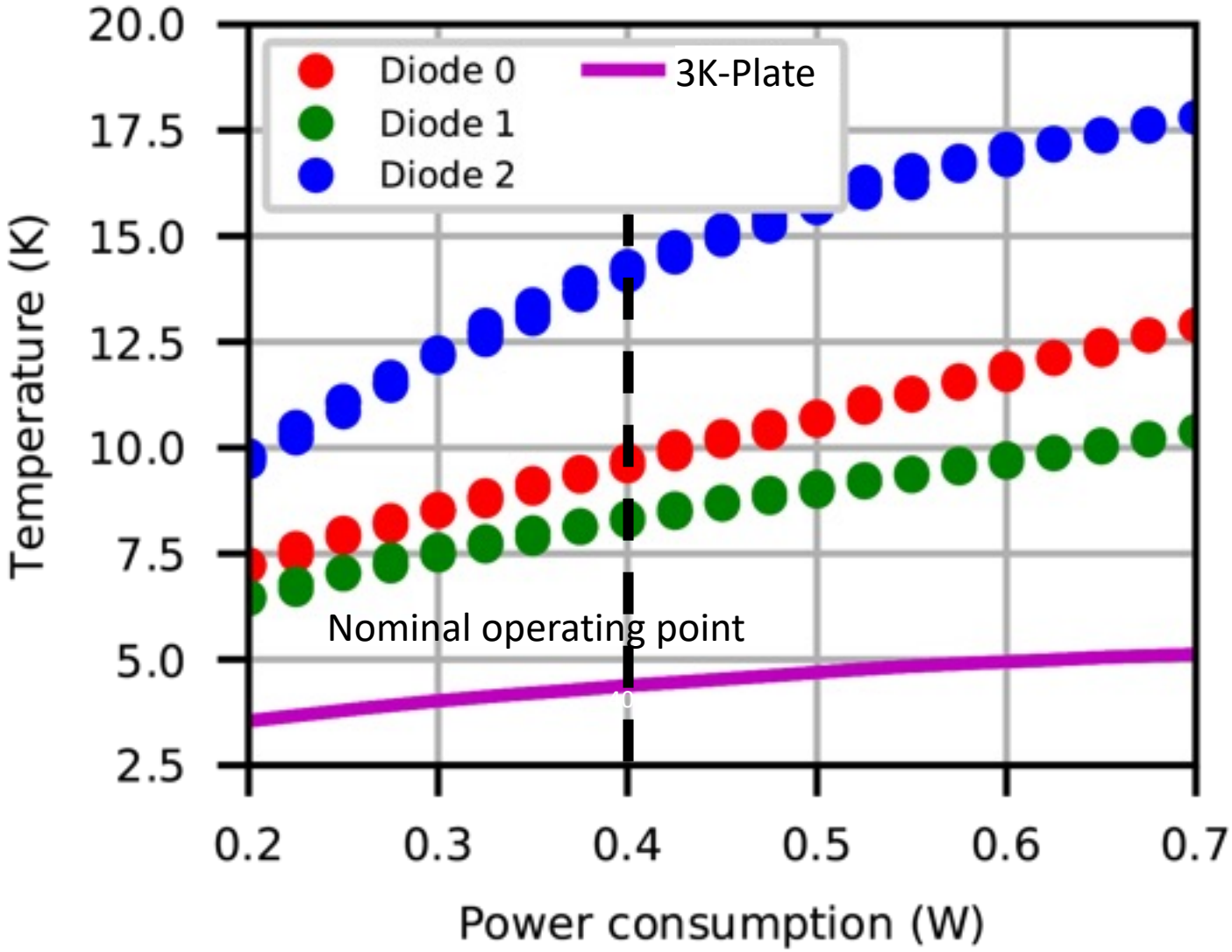




[B. Patra, ISSCC'20]

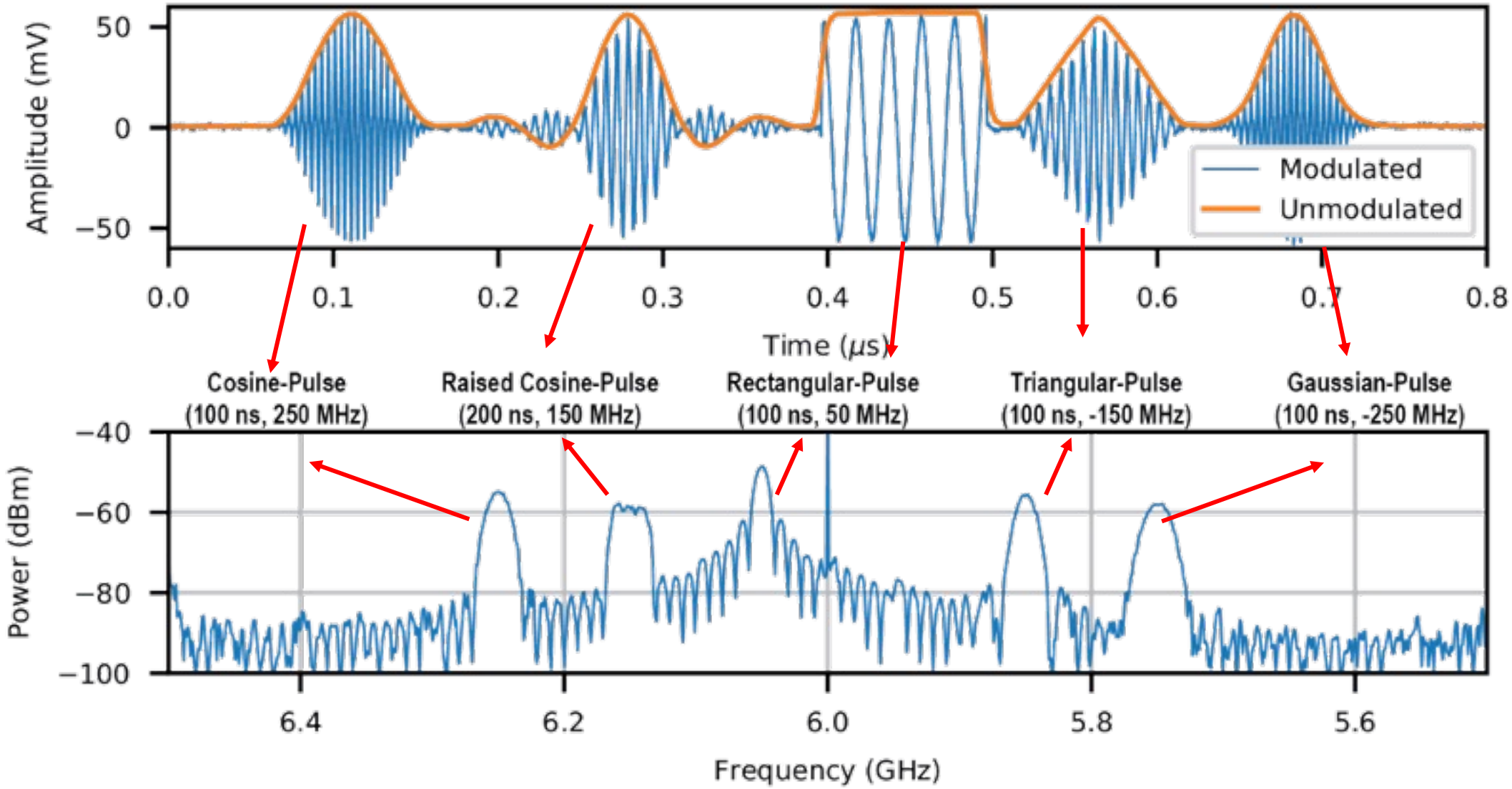
Chip Micrograph & Self heating





[B. Patra, ISSCC'20]

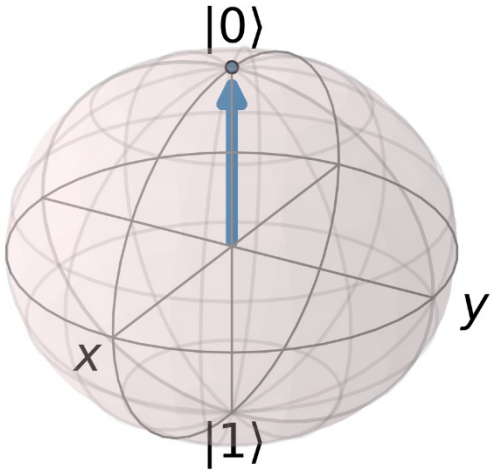
Experimental results – Pulse Shaping

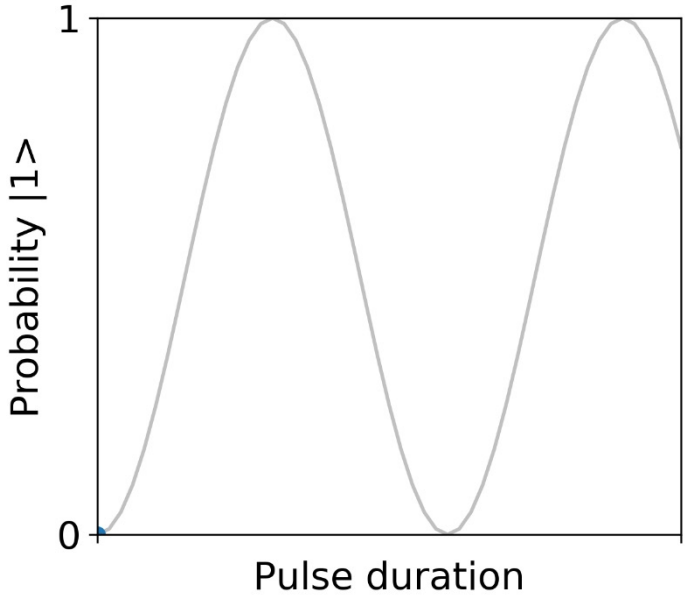


[B. Patra, ISSCC'20]

Explaining Rabi Experiment

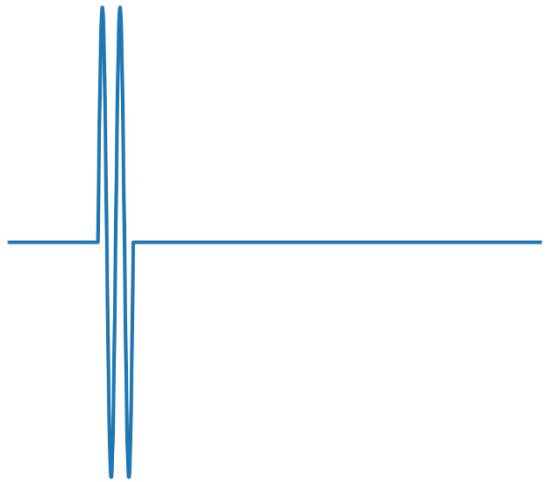
- Initialization

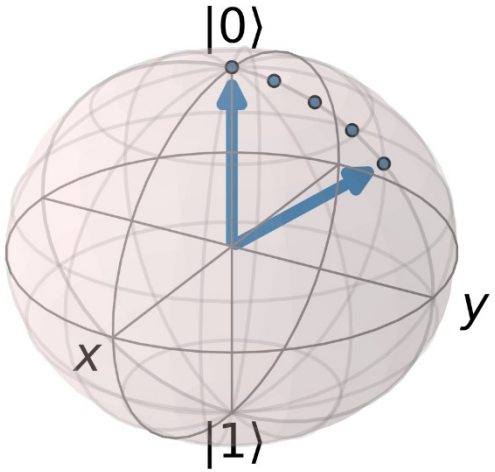


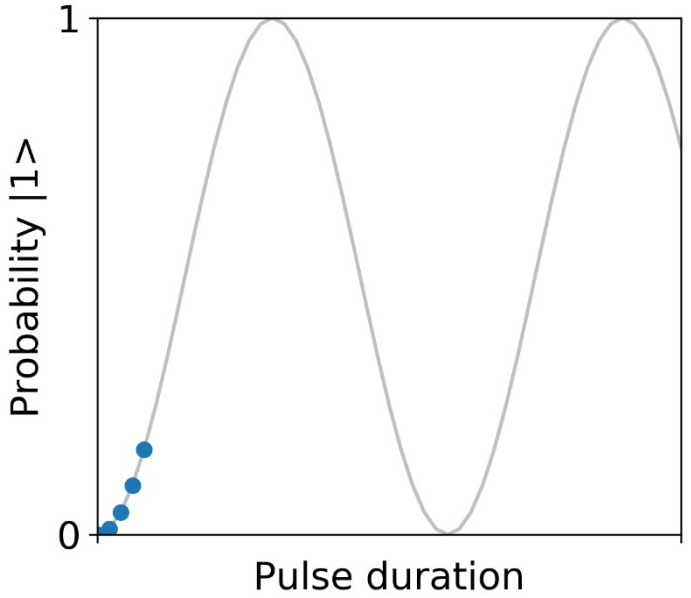


Explaining Rabi Experiment

- Increase pulse duration in steps

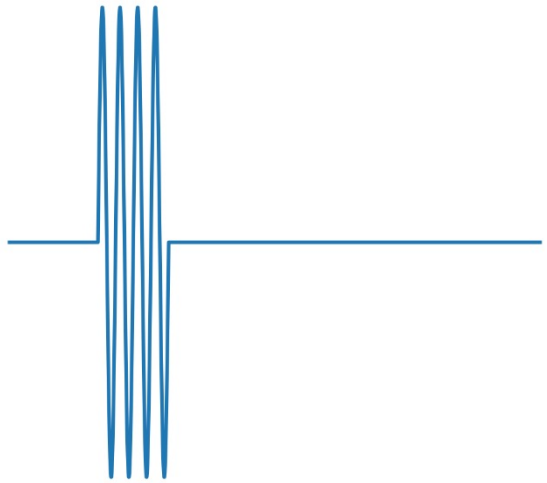


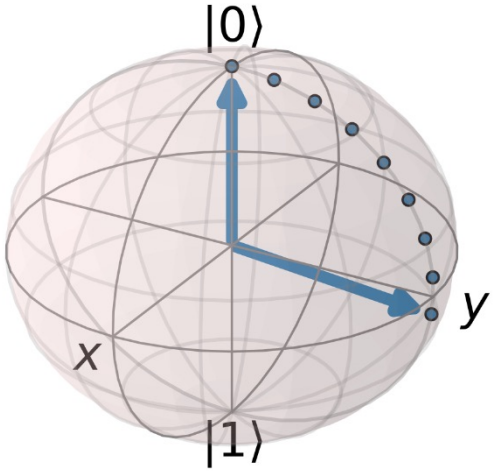


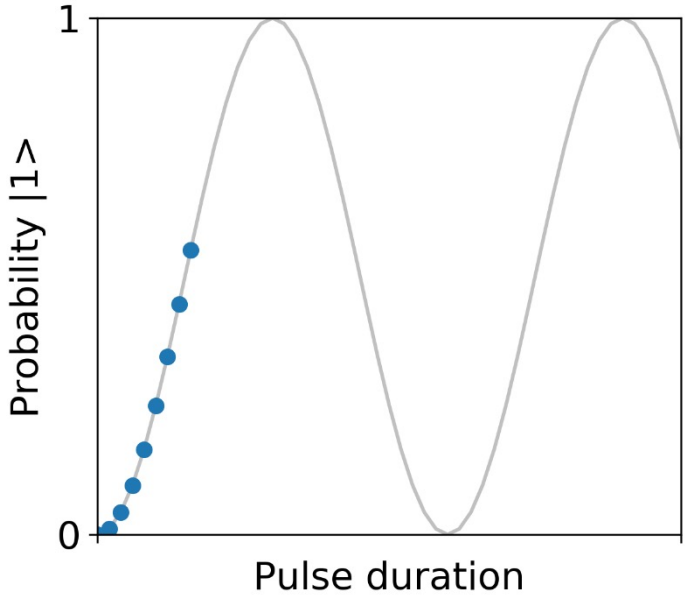


Explaining Rabi Experiment

- Increase pulse duration in steps

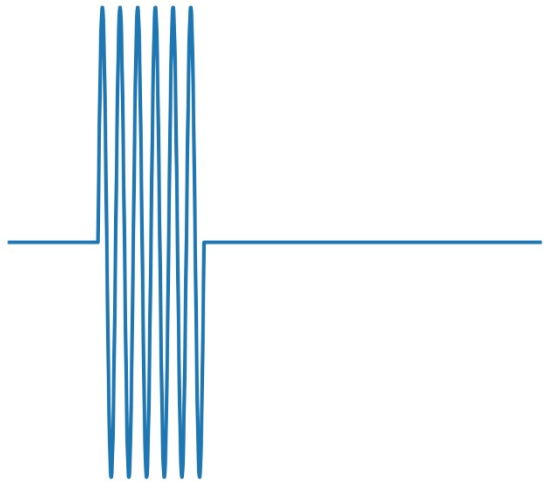


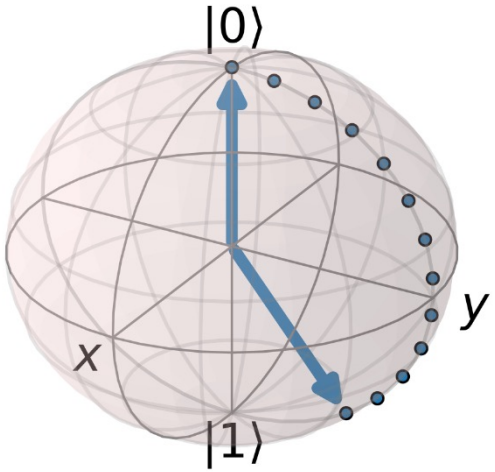


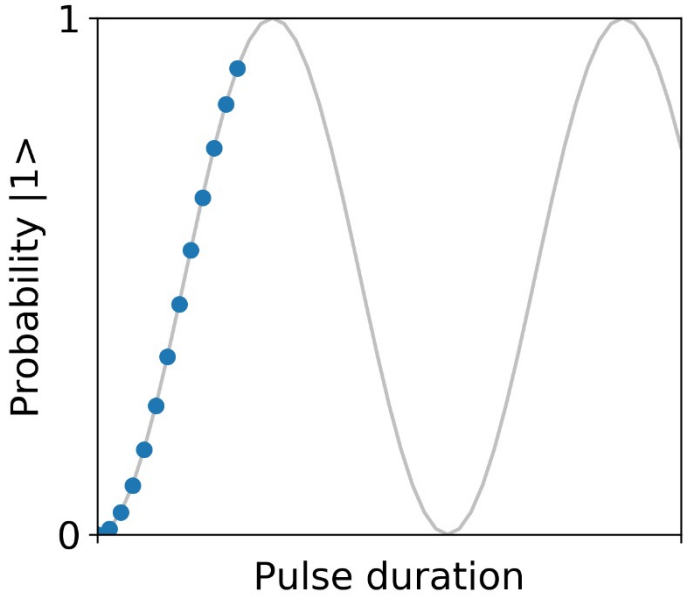


Explaining Rabi Experiment

- Increase pulse duration in steps

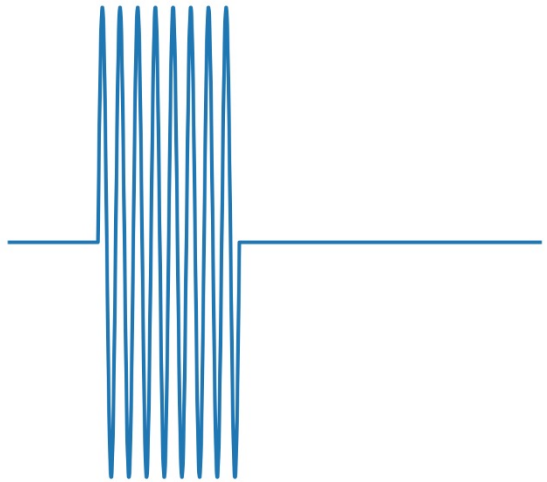


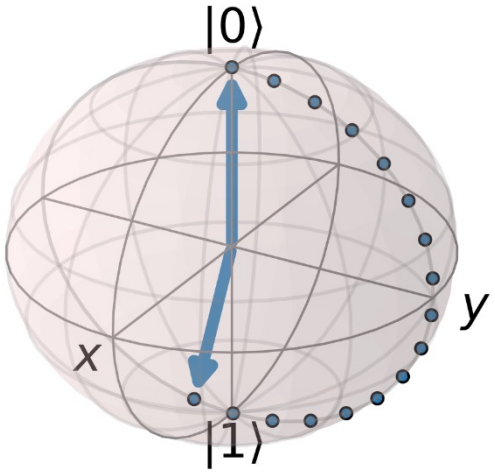


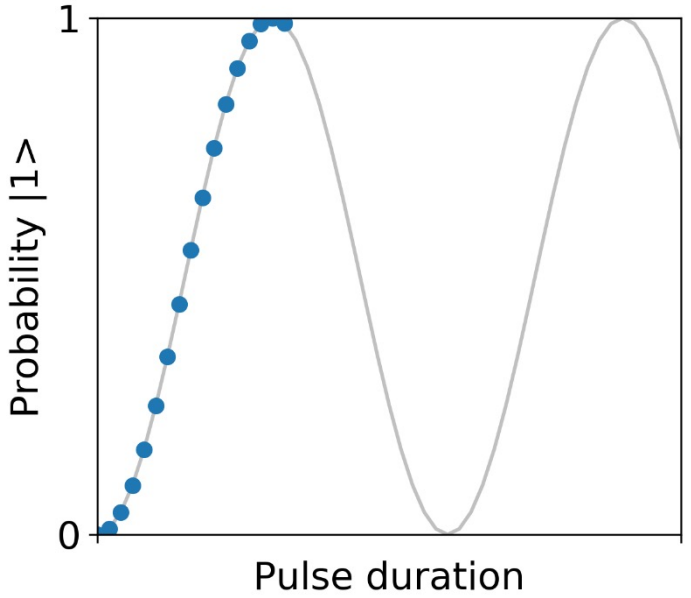


Explaining Rabi Experiment

- Increase pulse duration in steps

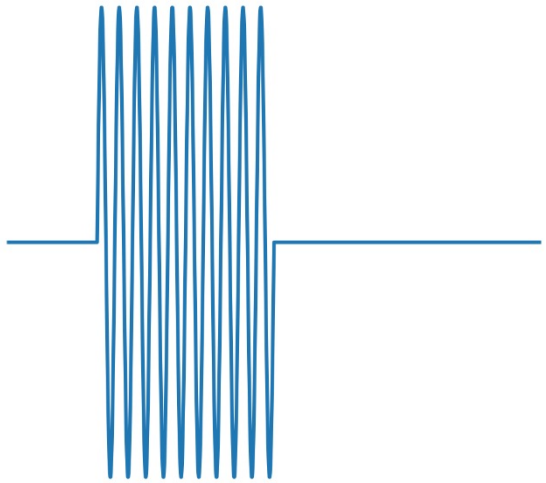


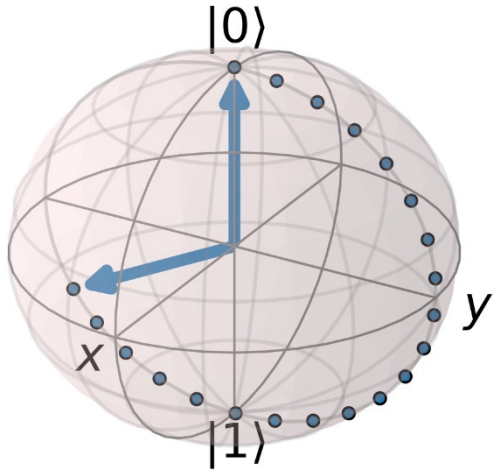


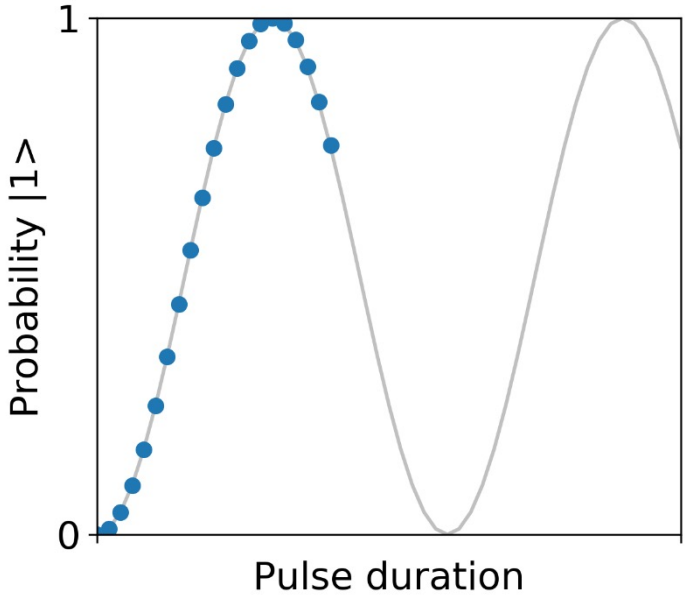


Explaining Rabi Experiment

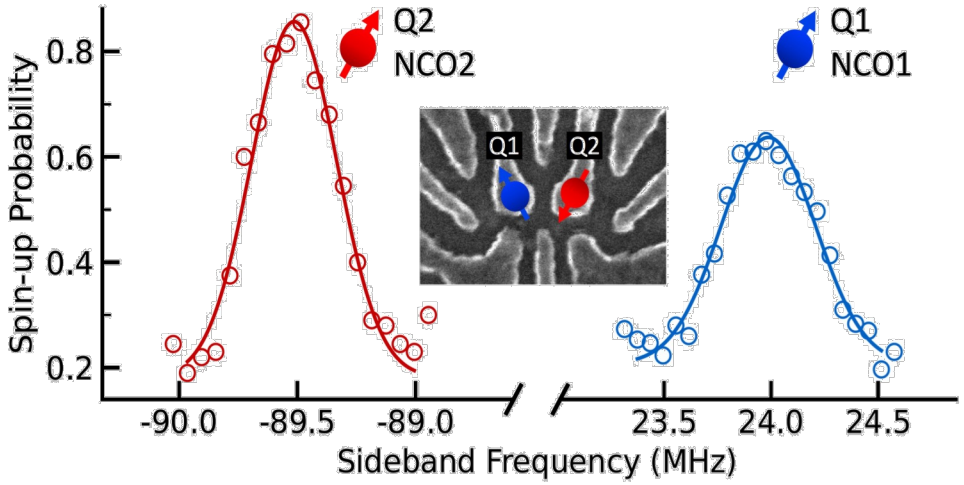
- Increase pulse duration in steps

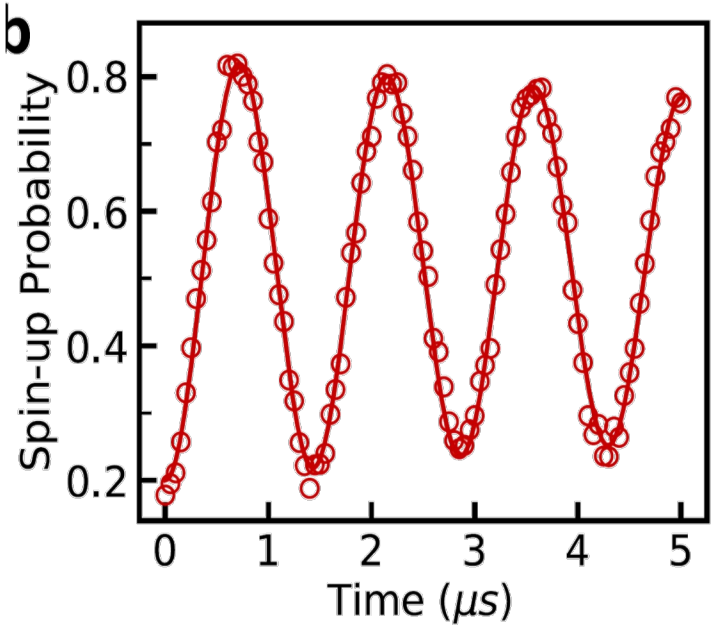


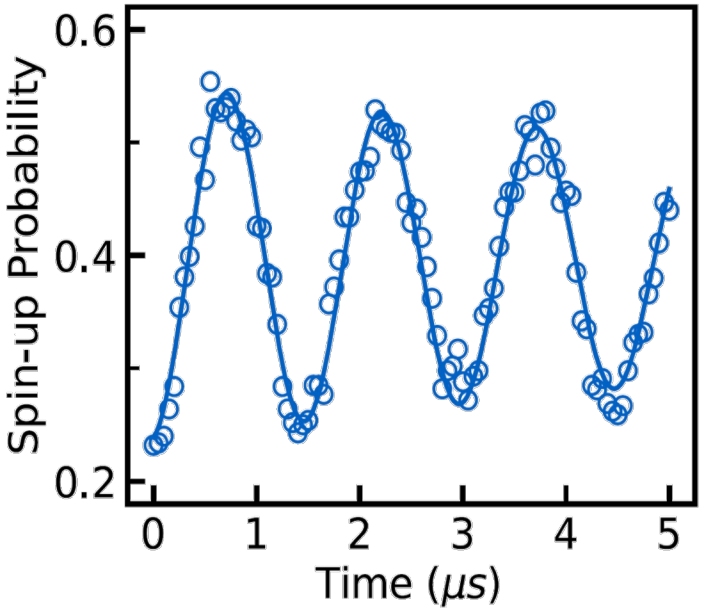




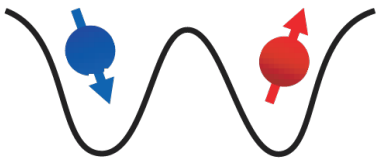
Simultaneous Rabi Oscillation on Two Qubits



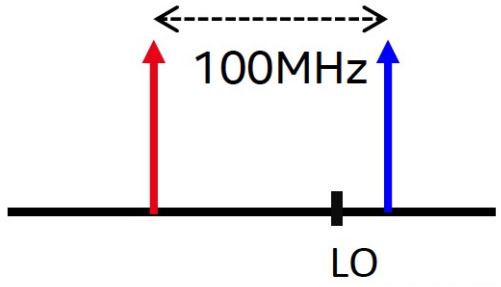




Coupling OFF

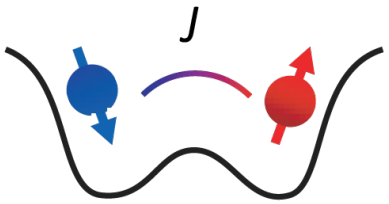


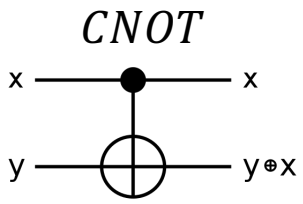
Generate two-tone signal with Horse Ridge



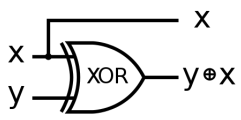
Towards Two-Qubit Gate Operation

Coupling ON

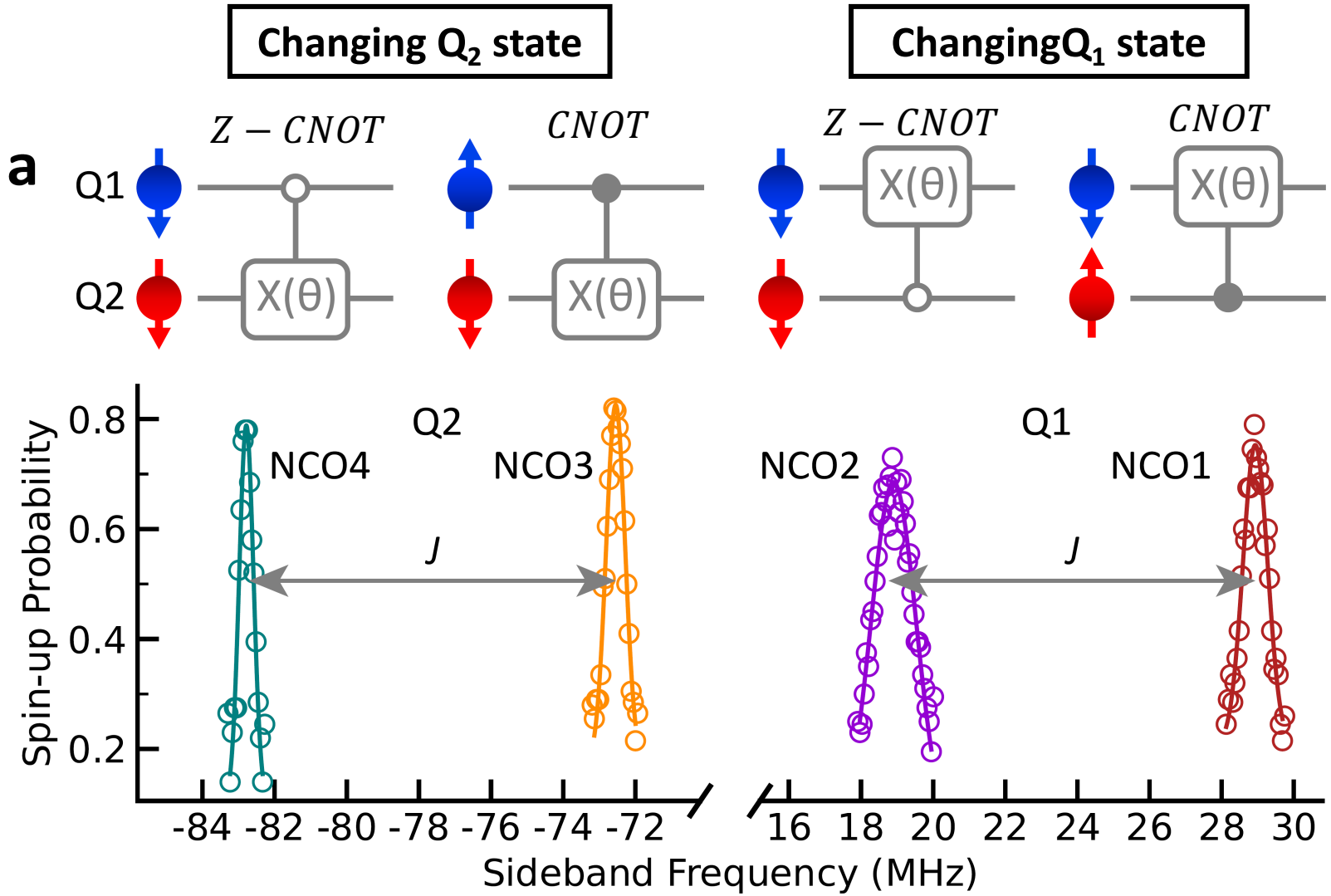




input		output	
x	y	x	y+x
|0⟩	|0⟩	|0⟩	|0⟩
|0⟩	|1⟩	|0⟩	|1⟩
|1⟩	|0⟩	|1⟩	|1⟩
|1⟩	|1⟩	|1⟩	|0⟩



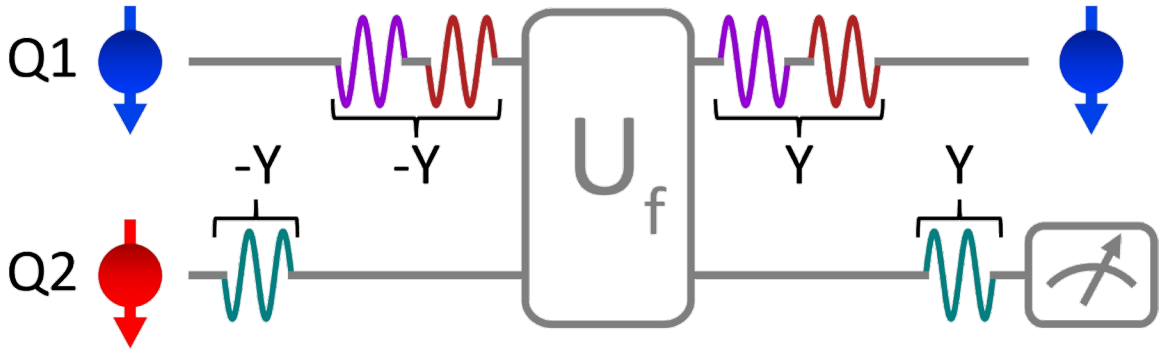
input		output	
x	y	x	y+x
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

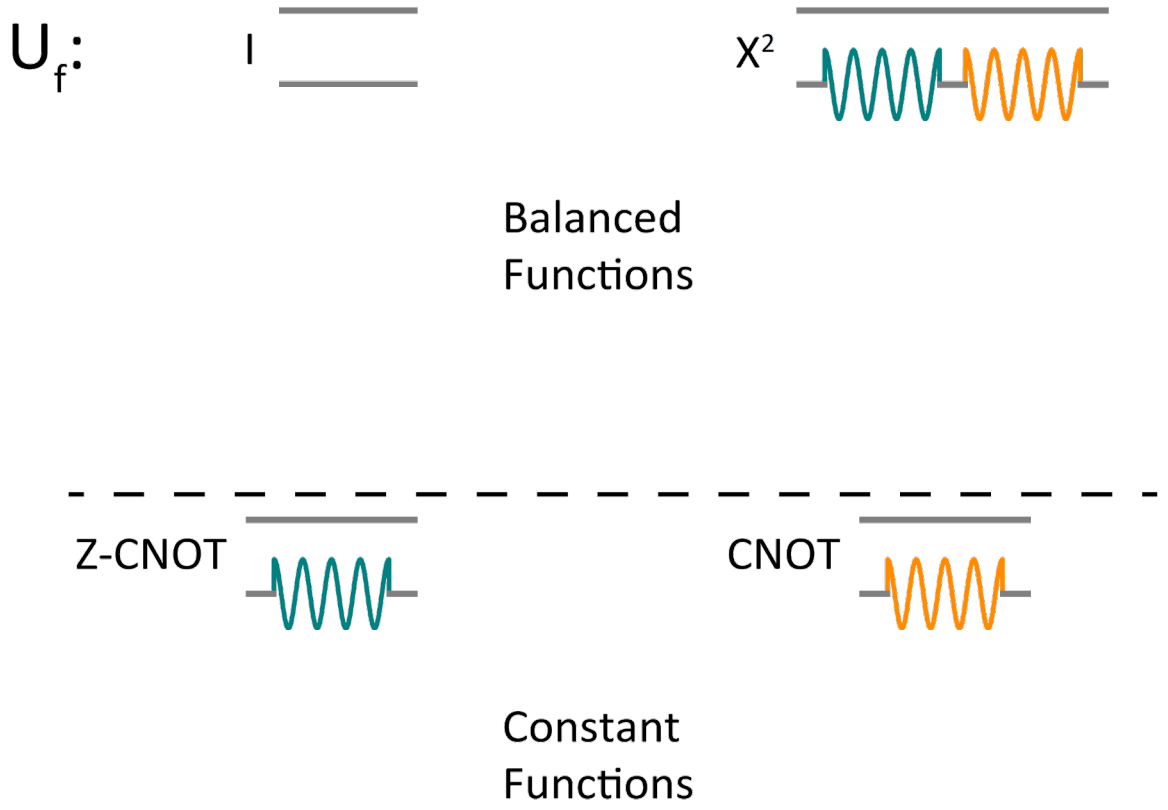


[X. Xue, Nature'21]

A Cryo-CMOS-Driven Quantum Algorithm

Deutsch-Jozsa algorithm:
identify in one-shot if U_f is balanced or not



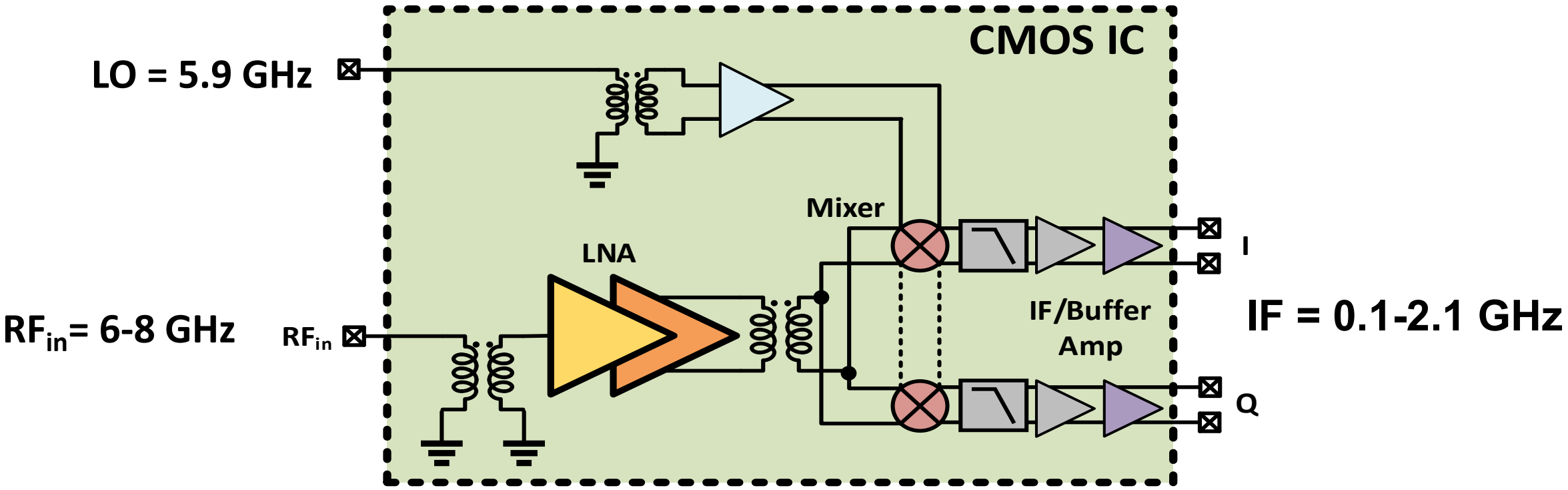


[X. Xue, Nature'21]

Outline

- Need for cryogenic electronics for scalable quantum computers
  - Associated challenges
- Introducing control and readout principles for spin qubits
- Cryo-CMOS controller for spin qubits
  - Behavior of active and passive CMOS devices at cryogenic temperatures
  - Required circuit and system specification
  - Controller architecture and circuit implementation
  - Electrical characterization
  - Experiments with qubits (single- and two-qubit operations)
- Gate-based readout for spin qubits
  - Receiver architecture and implementation
  - Electrical characterization
  - Experiments with qubits
- Conclusions

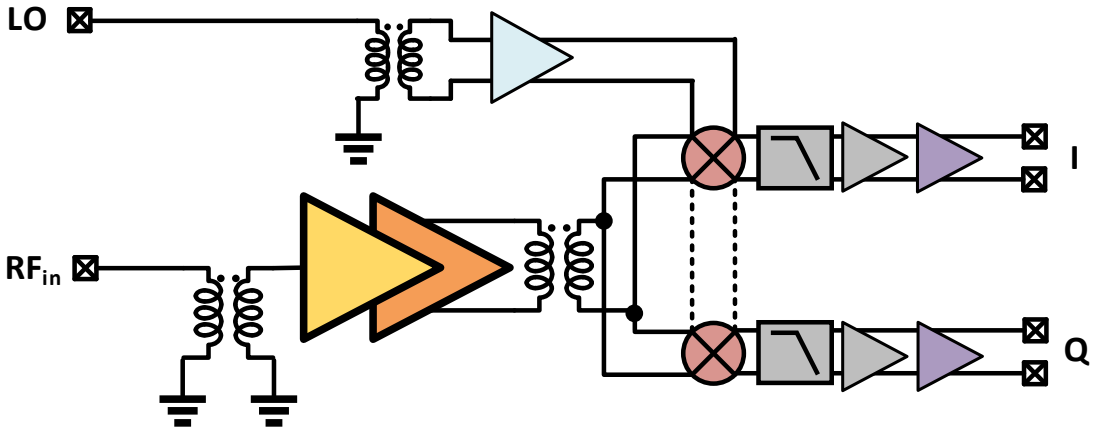
Proposed RX Architecture

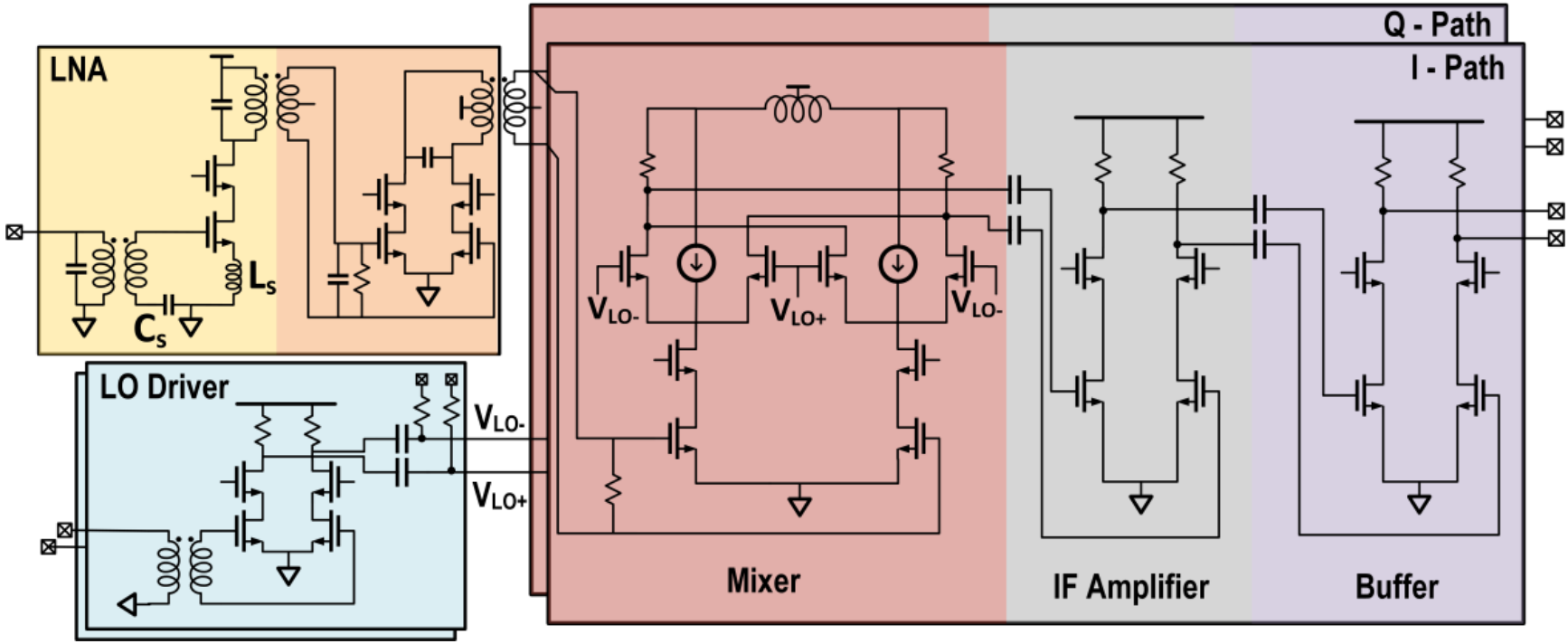


- **High-IF RX architecture**
  - Avoid higher 1/f noise at cryogenic temperatures, thus maintaining the qubits SNR over the entire bandwidth
  - Slightly increasing the power consumption of IF amplifiers and ADCs

[B. Prabowo, ISSCC'21]

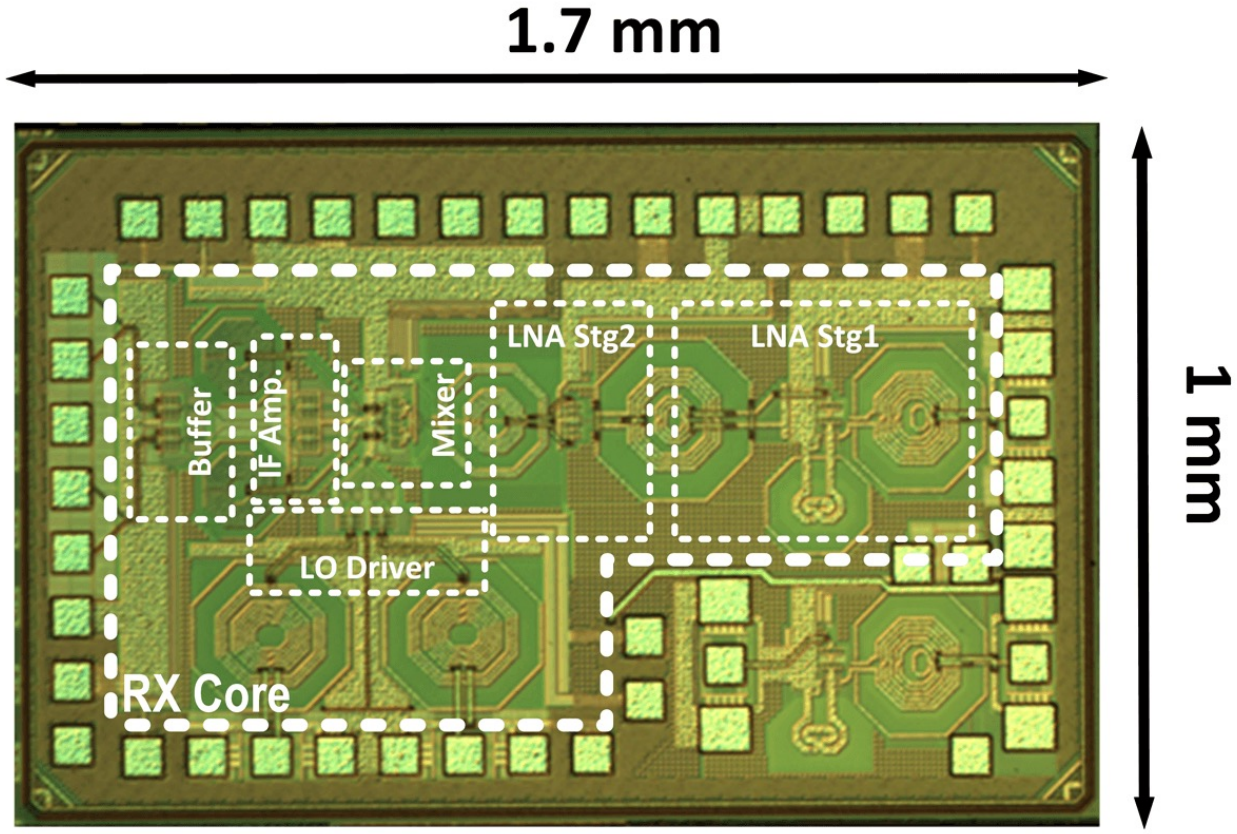
RX Schematic

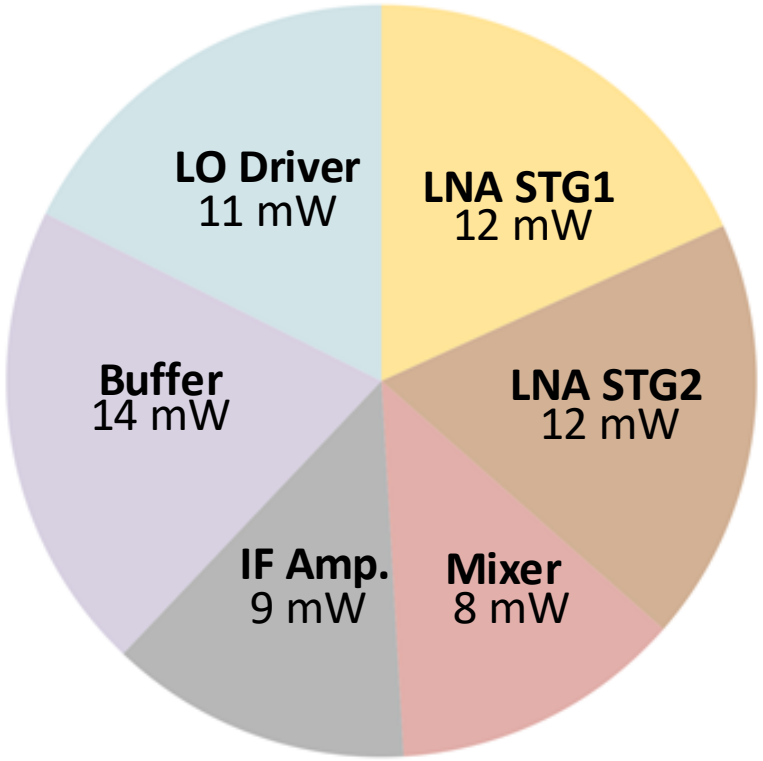




[B. Prabowo, ISSCC'21]

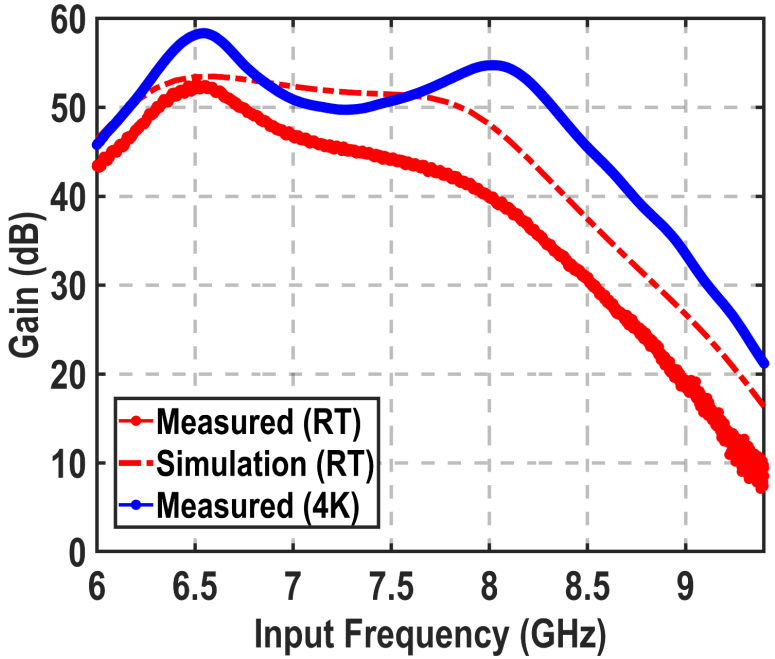
Chip Micrograph & Power Consumption

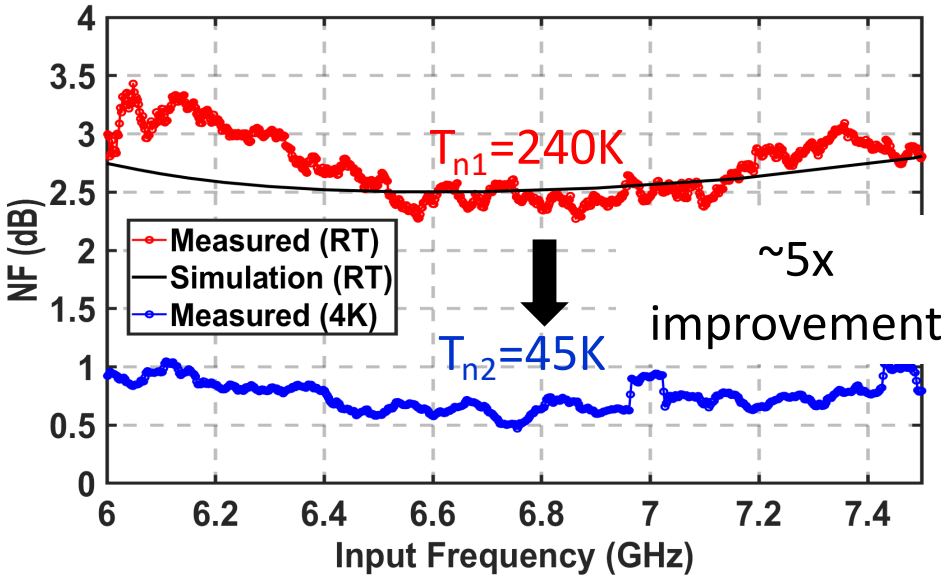


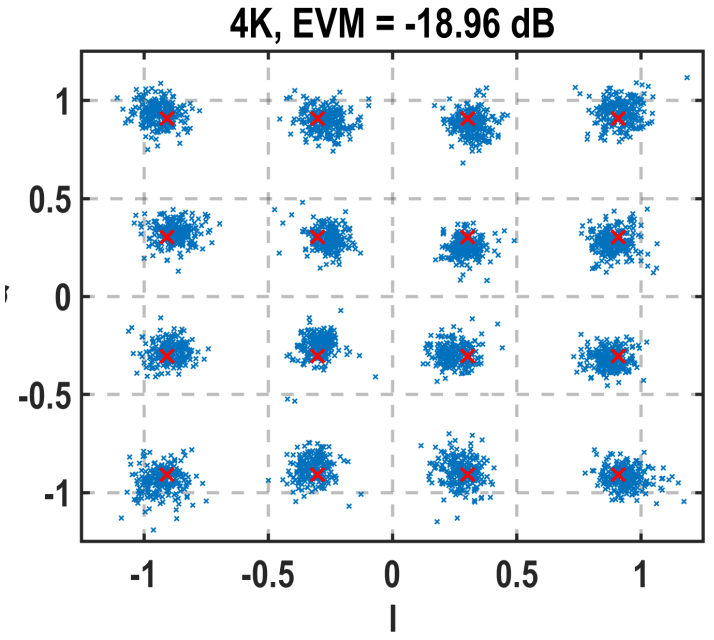


- Total power of 66mW at 4K

RX Characterizations at 300K & 4K







~5 dB gain increase at 4K

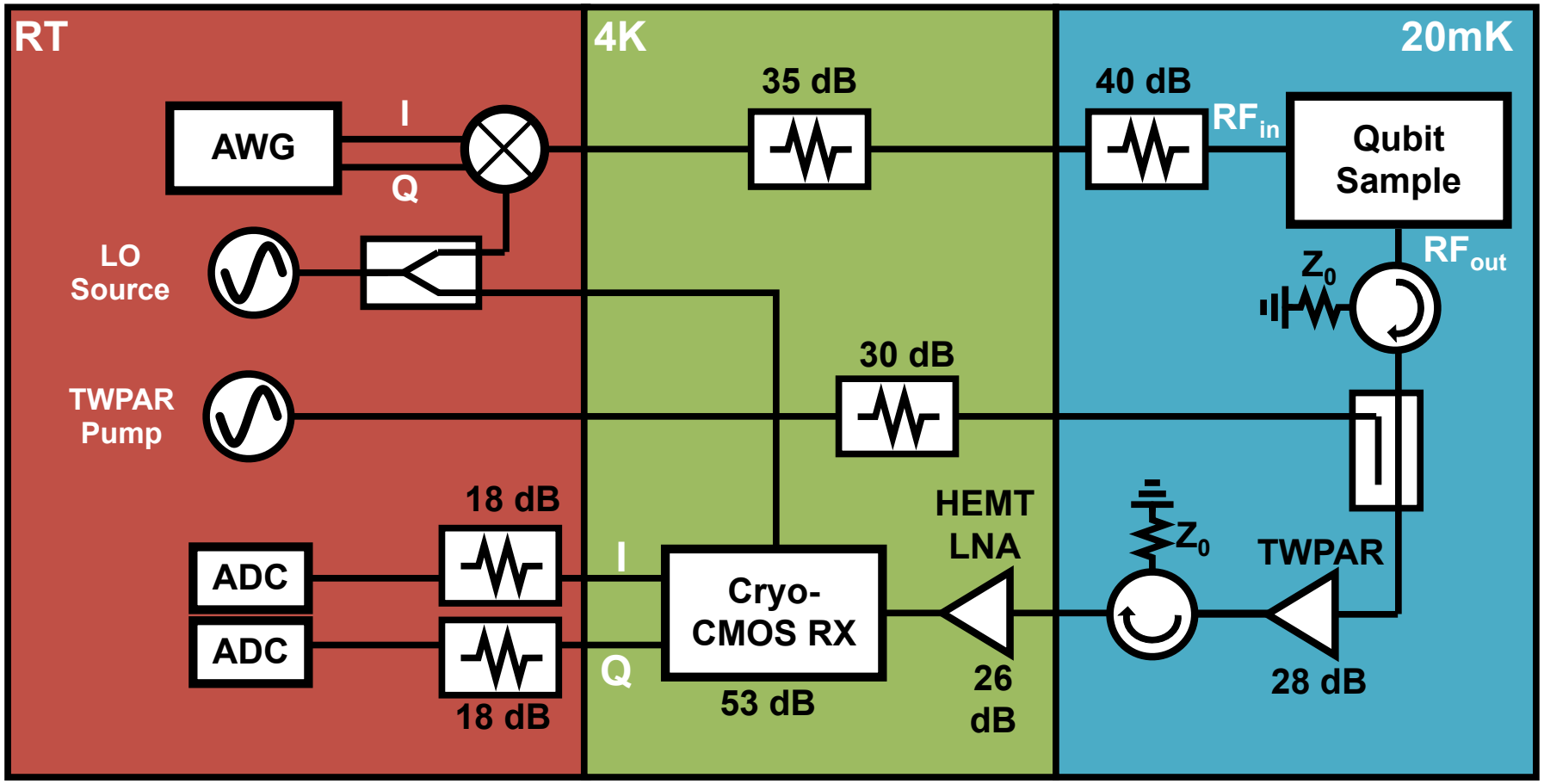
- Increase in mobility
- Increase in Q factor

- **~5x NF reduction**
  - Shot noise
  - Self-heating effect

- 16-QAM -70 dBm input
- 200 MHz Baseband LPF

[B. Prabowo, ISSCC'21]

Measurement Setup

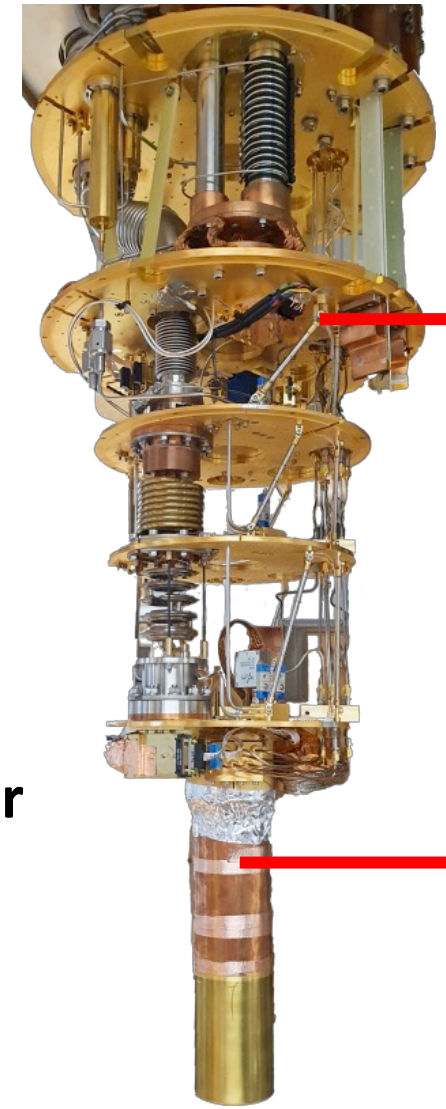


- A traveling-wave parametric amplifier (TWPAR) and a HEMT LNA are used in the readout chain not to limit the inherent qubit SNR.

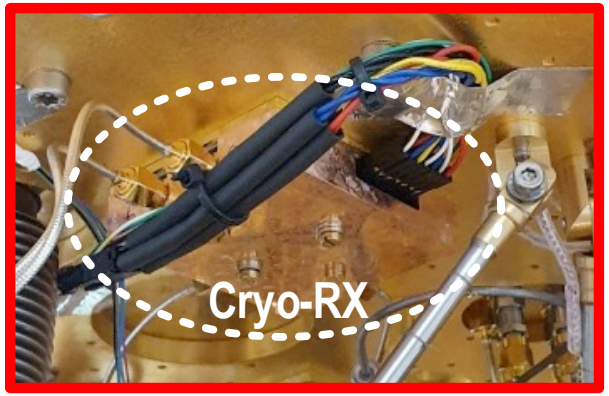
Readout Setup

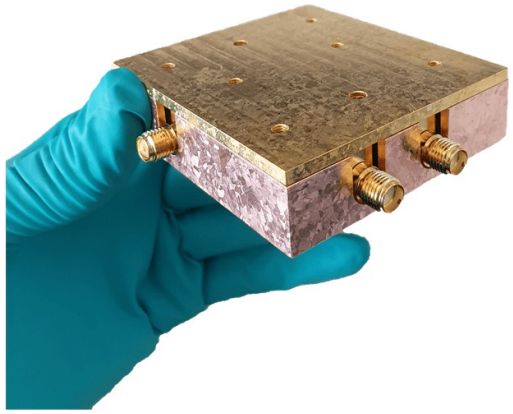
4K Plate

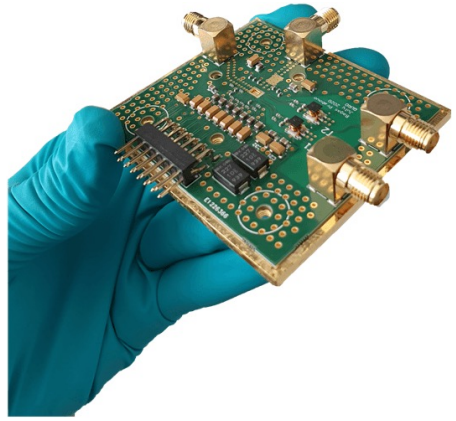
Mixing Chamber

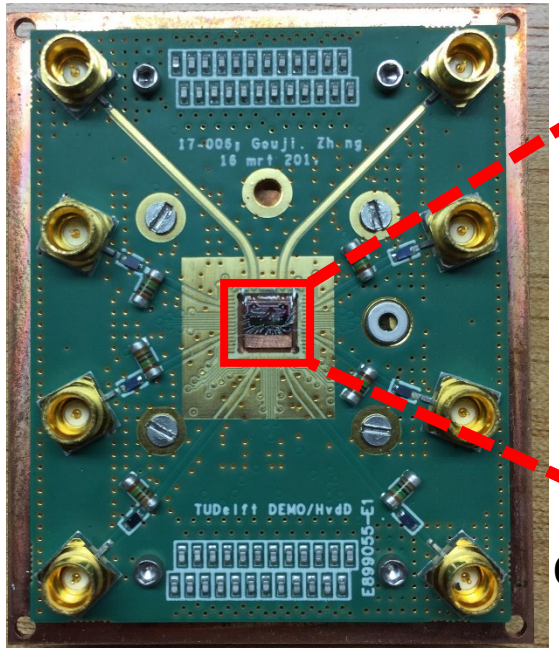


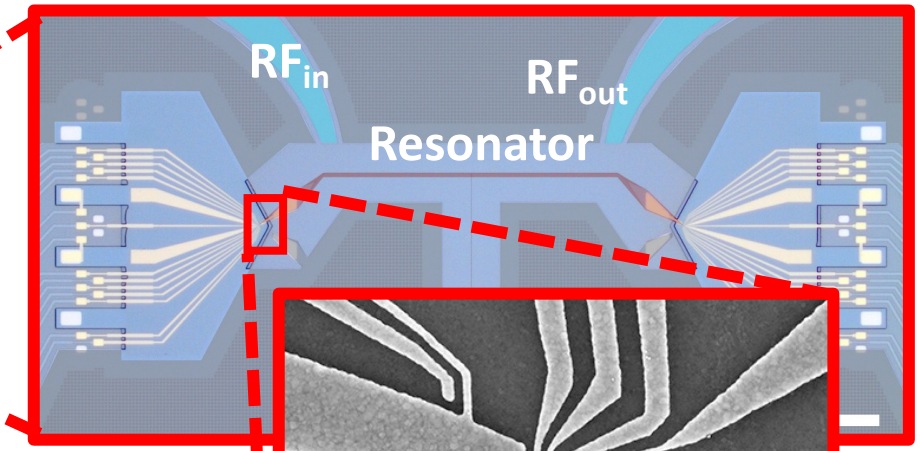
Installed copper enclosure

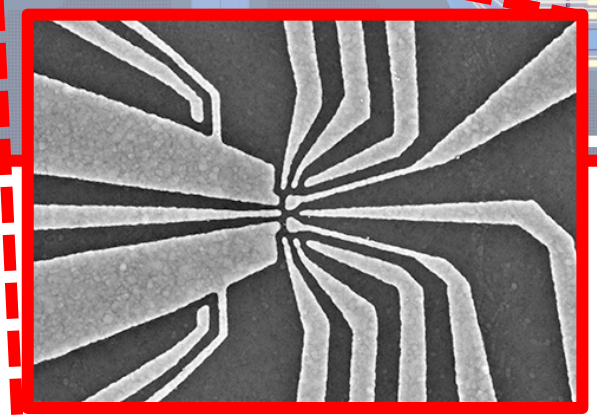






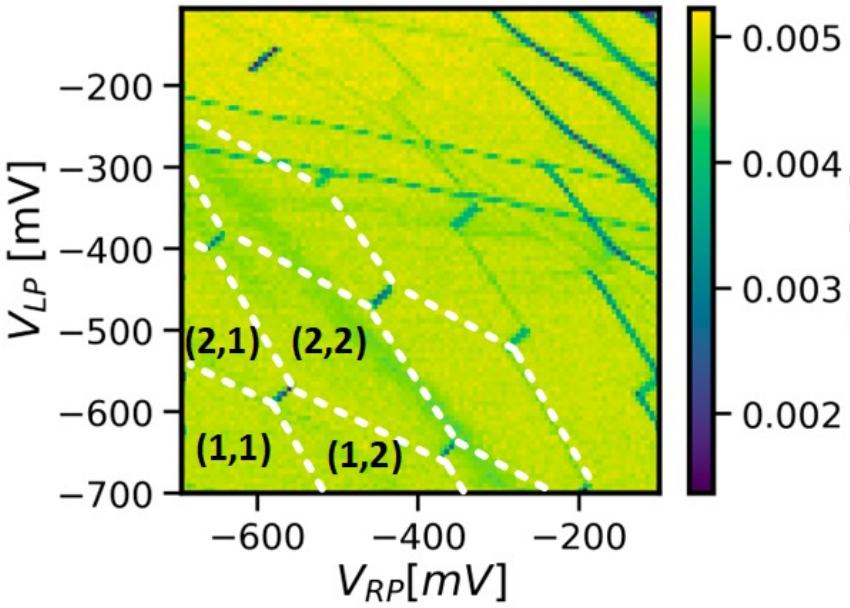


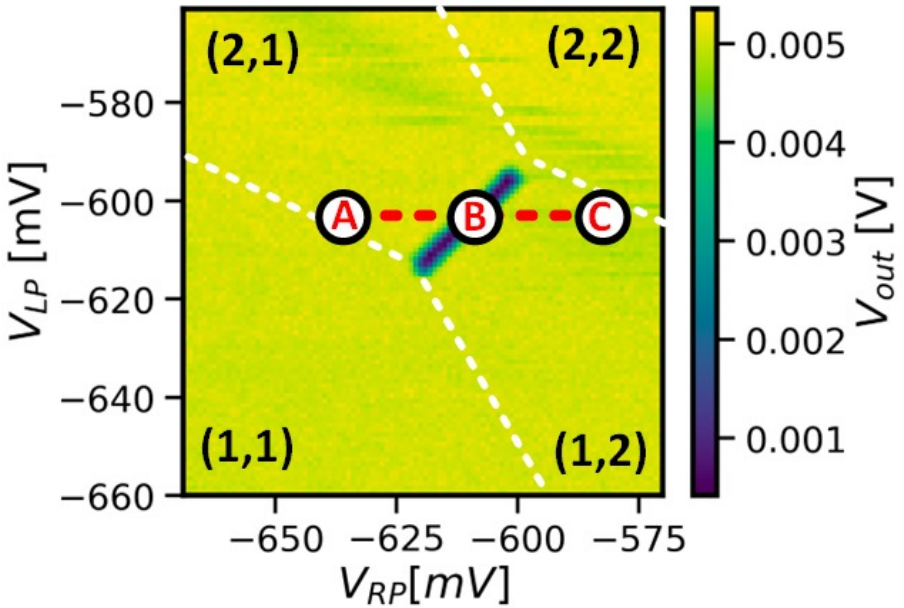


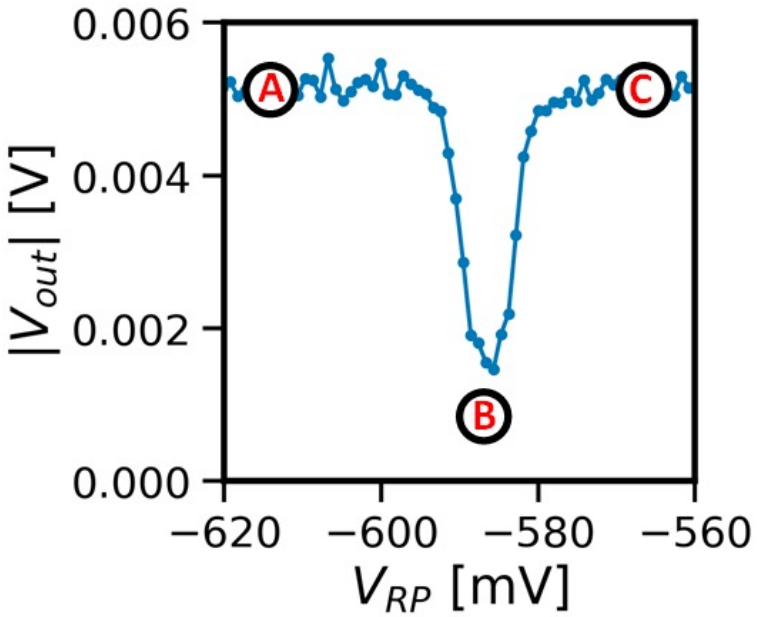


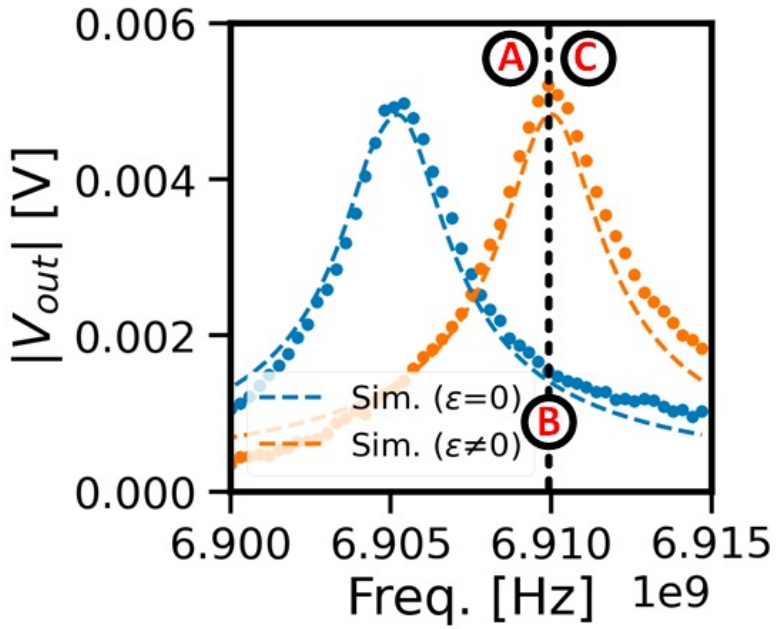
Quantum Dot

Measured Charge Stability Diagram





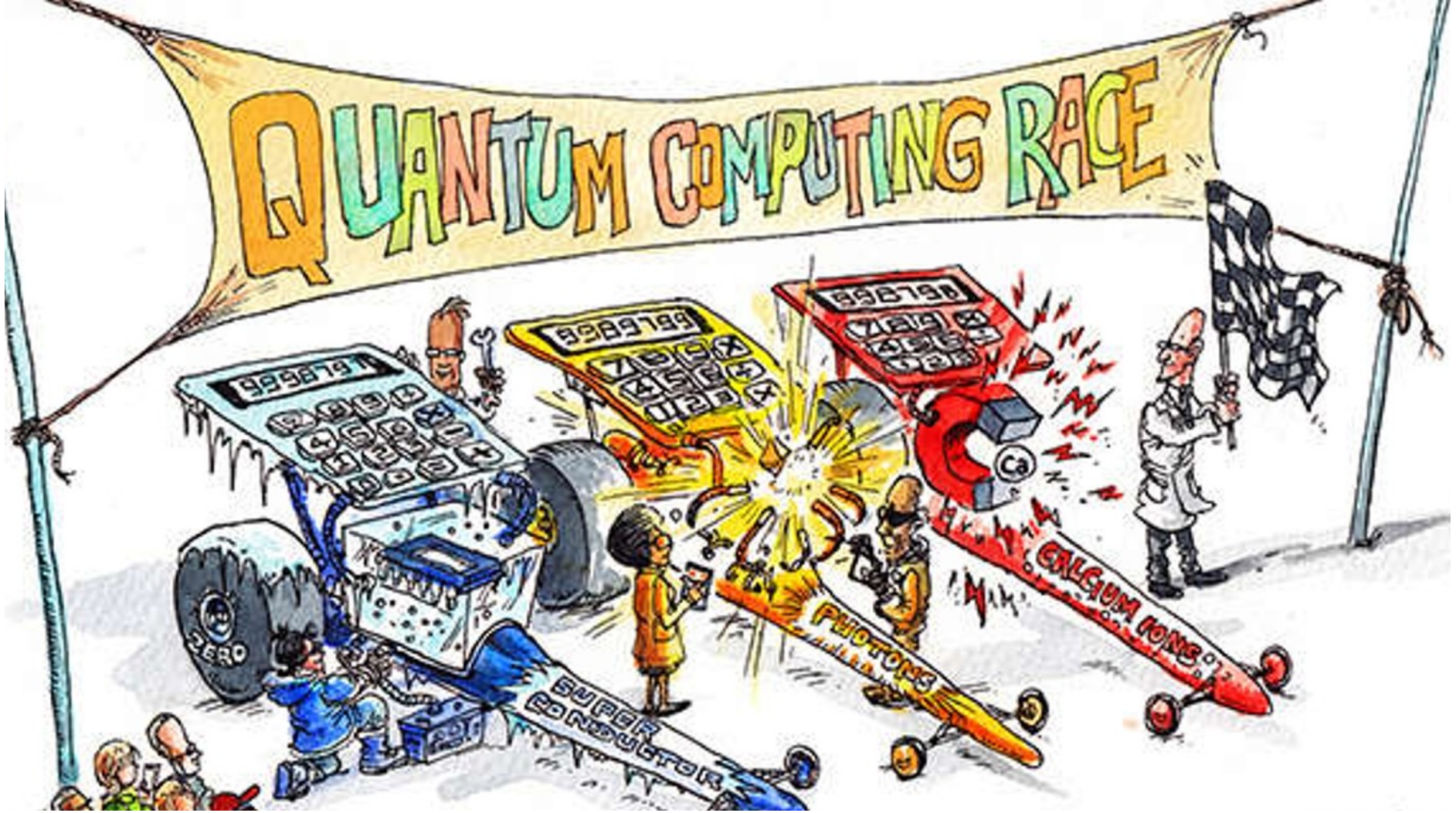




[B. Prabowo, arXiv'23]

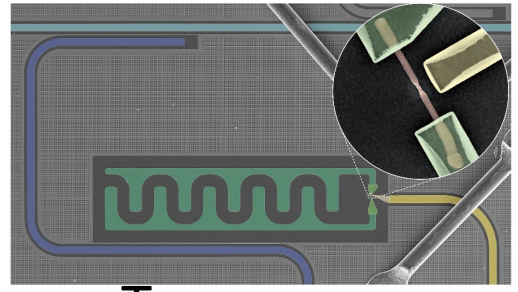
Outline

- Need for cryogenic electronics for scalable quantum computers
  - Associated challenges
- Introducing control and readout principles for spin qubits
- Cryo-CMOS controller for spin qubits
  - Behavior of active and passive CMOS devices at cryogenic temperatures
  - Required circuit and system specification
  - Controller architecture and circuit implementation
  - Electrical characterization
  - Experiments with qubits (single- and two-qubit operations)
- Gate-based readout for spin qubits
  - Receiver architecture and implementation
  - Electrical characterization
  - Experiments with qubits
- Conclusions

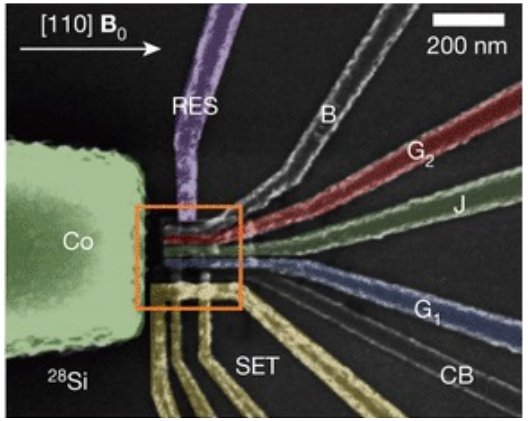


[The Economist, 20th Jun 2015]

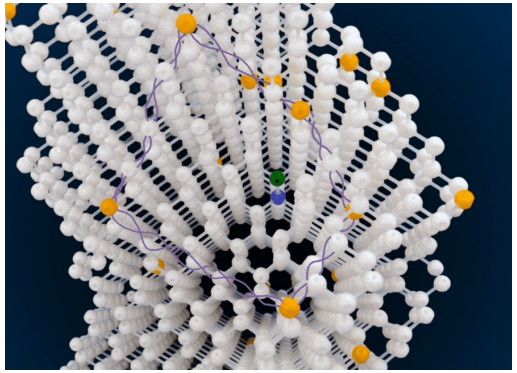
Cryo-CMOS: Betting on the winning horse



Transmons



Spin qubits



NV-Center

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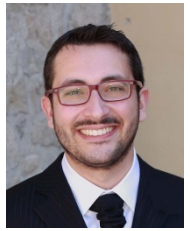
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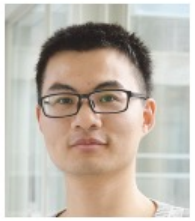
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Thank You for Your Attention!