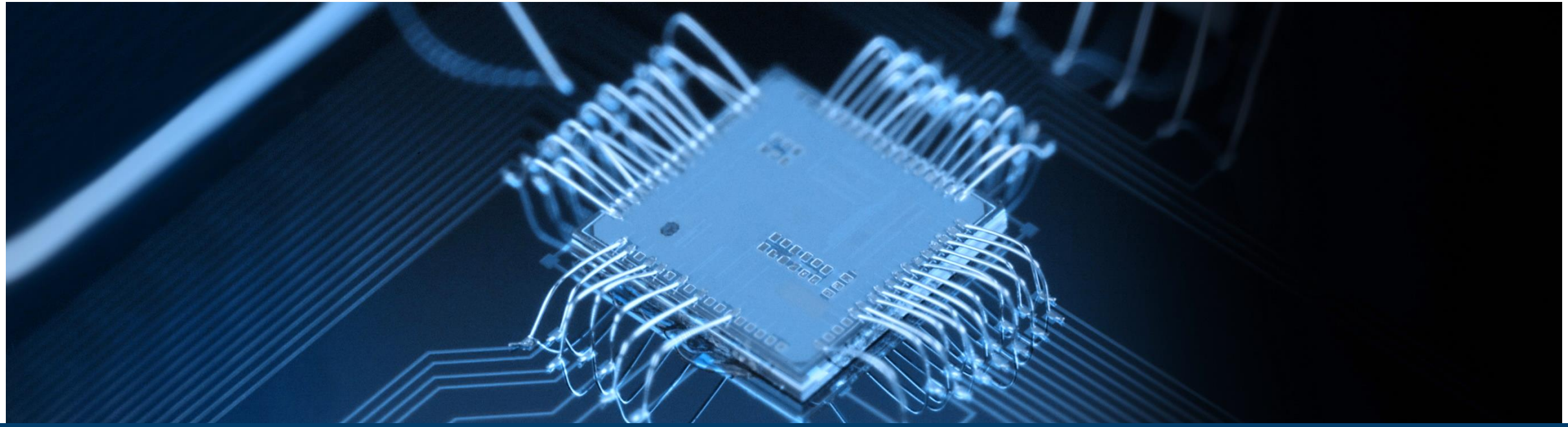
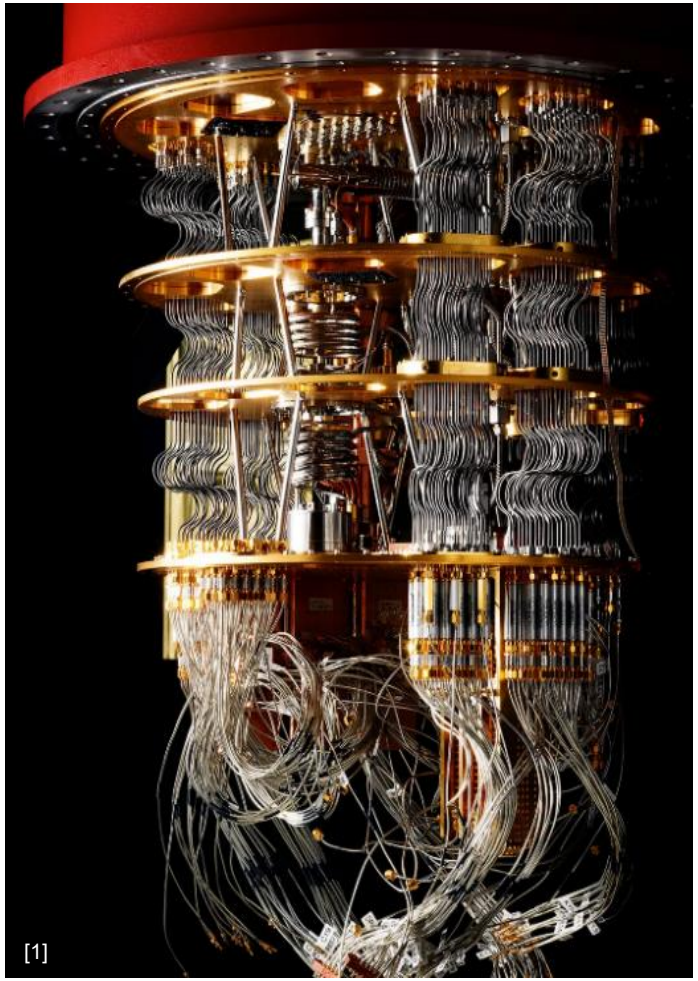


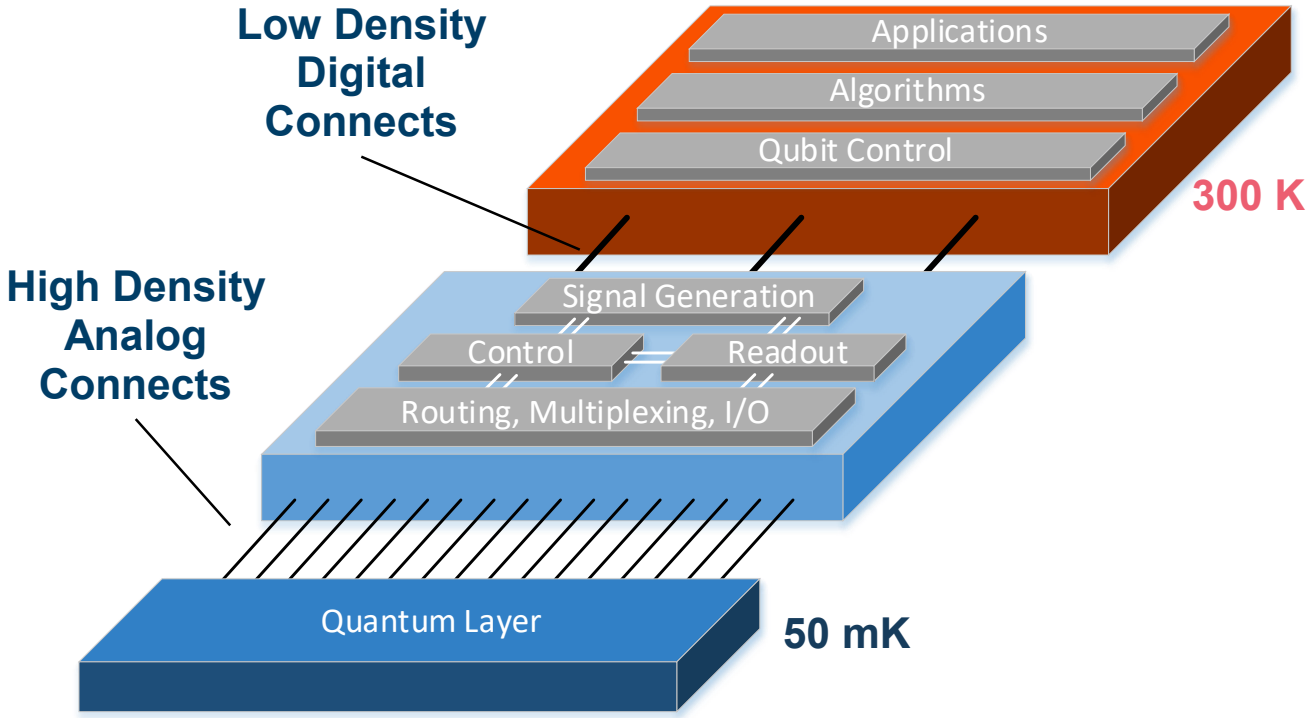
THERMAL MANAGEMENT CHALLENGES IN CRYOGENIC SYSTEM INTEGRATION: SPIN QUBIT BIASING WITH A CMOS DAC AT MK TEMPERATURE

WORKSHOP ON QUANTUM COMPUTING: DEVICES, CRYOGENIC ELECTRONICS AND PACKAGING

25.10.2023 | LEA SCHRECKENBERG, R. OTTEN, G. RIDGARD, P. VLIEX, S. VAN WAASEN

MOTIVATION



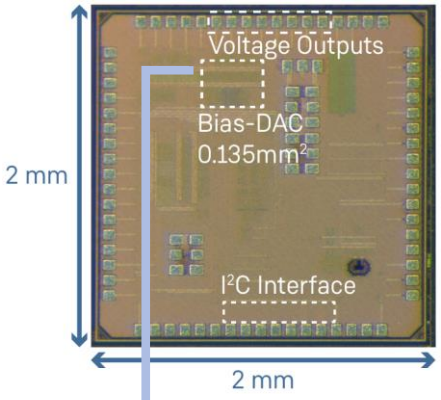


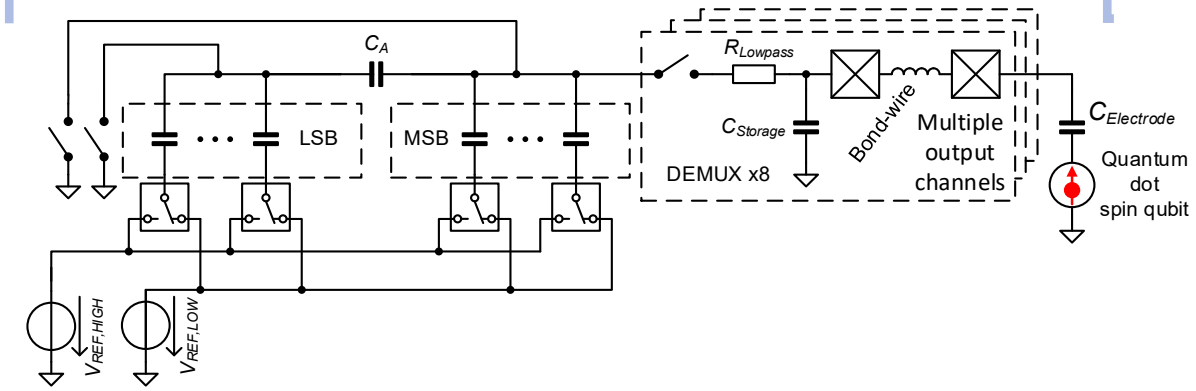
See: Pauka et al. A cryogenic CMOS chip for generating control signals for multiple qubits
Nature Electronics, Springer Science and Business Media LLC, **2021**, *4*, 64-70

ELECTRONS IN QUANTUM DOTS

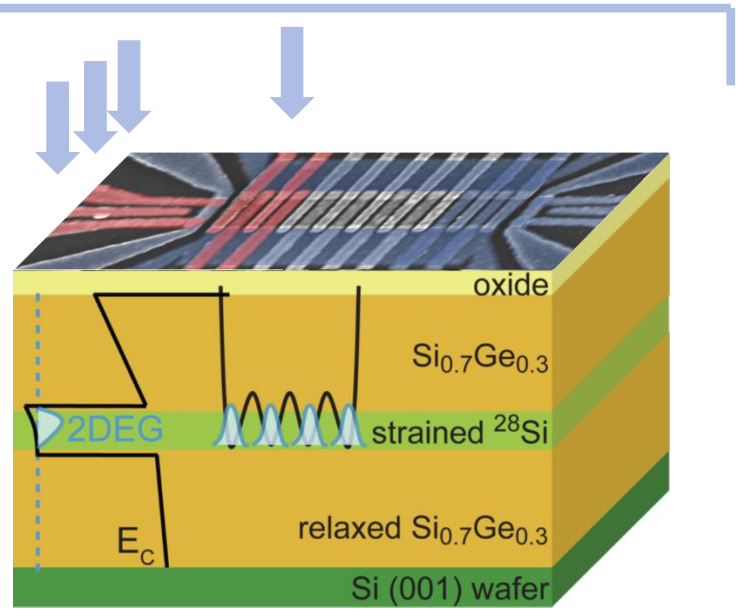
What is needed for a Spin Qubit Device?

Characteristic	Specification
Output channels	8
Voltage range	0V to 1V
Resolution	13 Bit
Step size	~ 122 µV
Consumption	30 - 40 µW





Several uncorrelated bias voltages per Qubit
- **Forming potential wells**



RWTH Aachen Si/SiGe Qubit

P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

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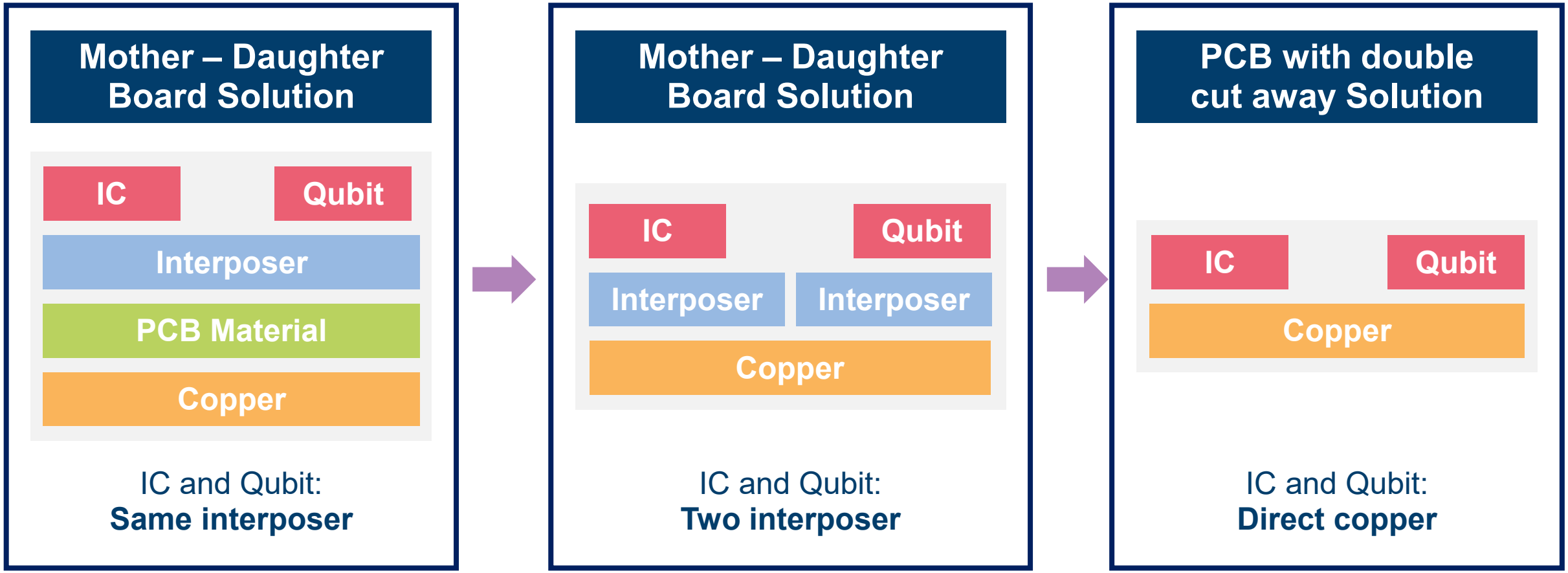
SETUP ITERATIONS

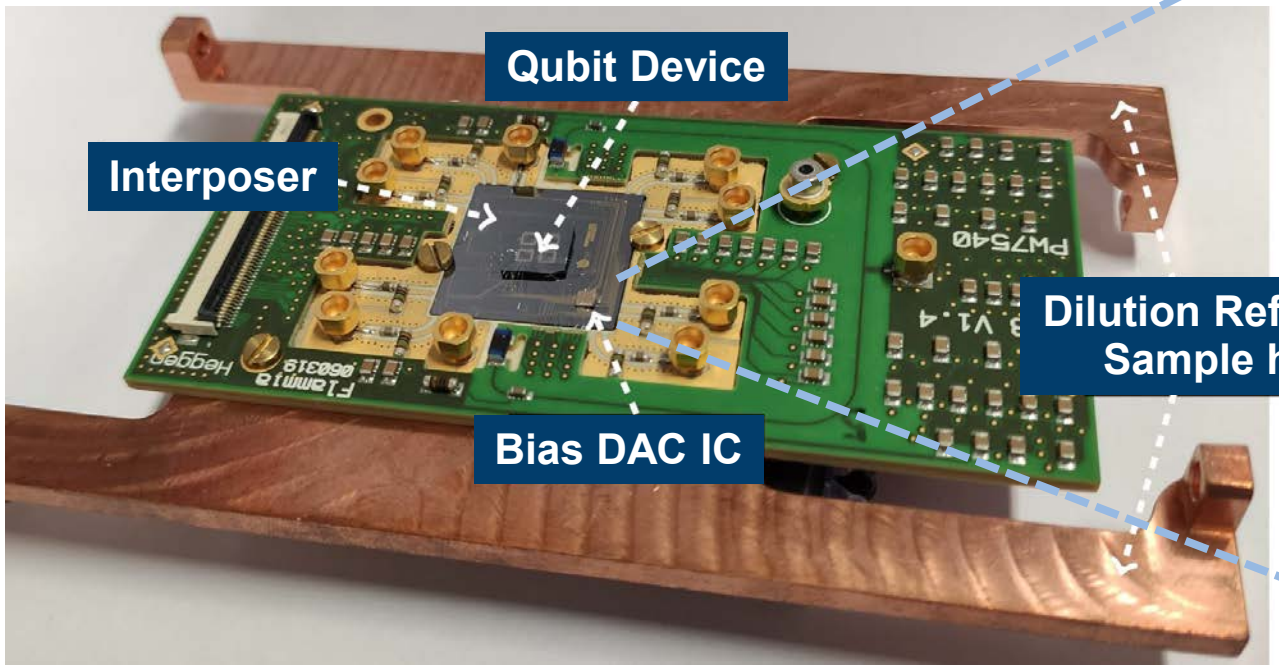


MOTHER – DAUGHTER BOARD SOLUTION

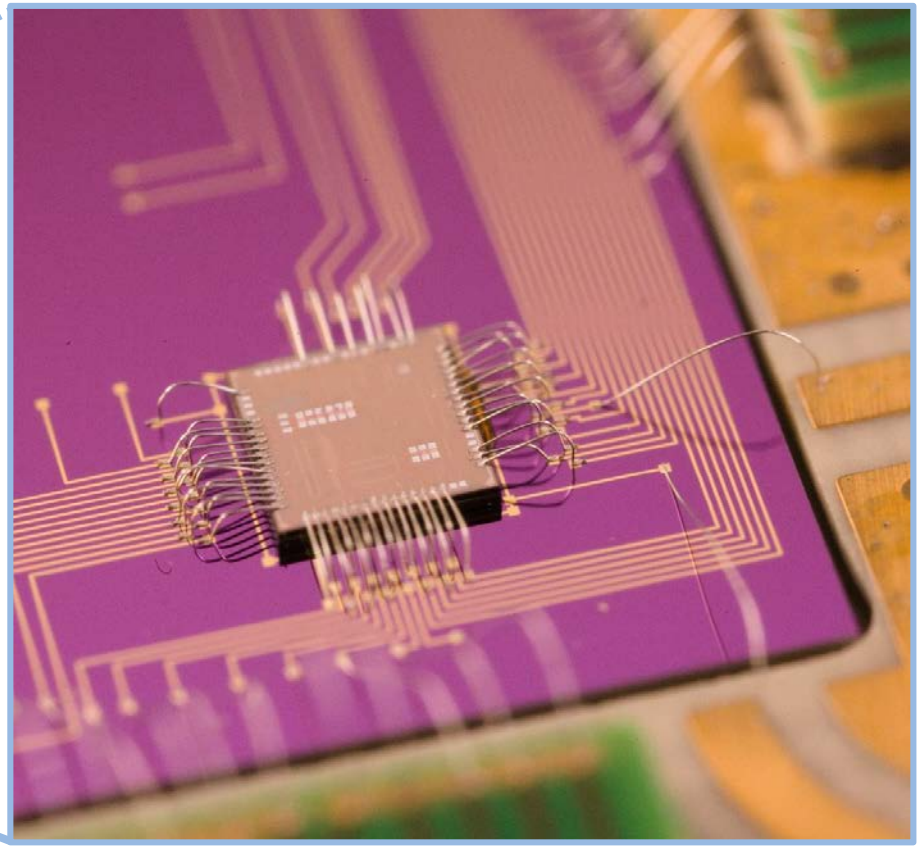
IC and Qubit Same Interposer

IC
Qubit
Interposer
PCB Material
Copper

DC DAC is working at mK mixing chamber temperature



Dilution Refrigerator Sample holder



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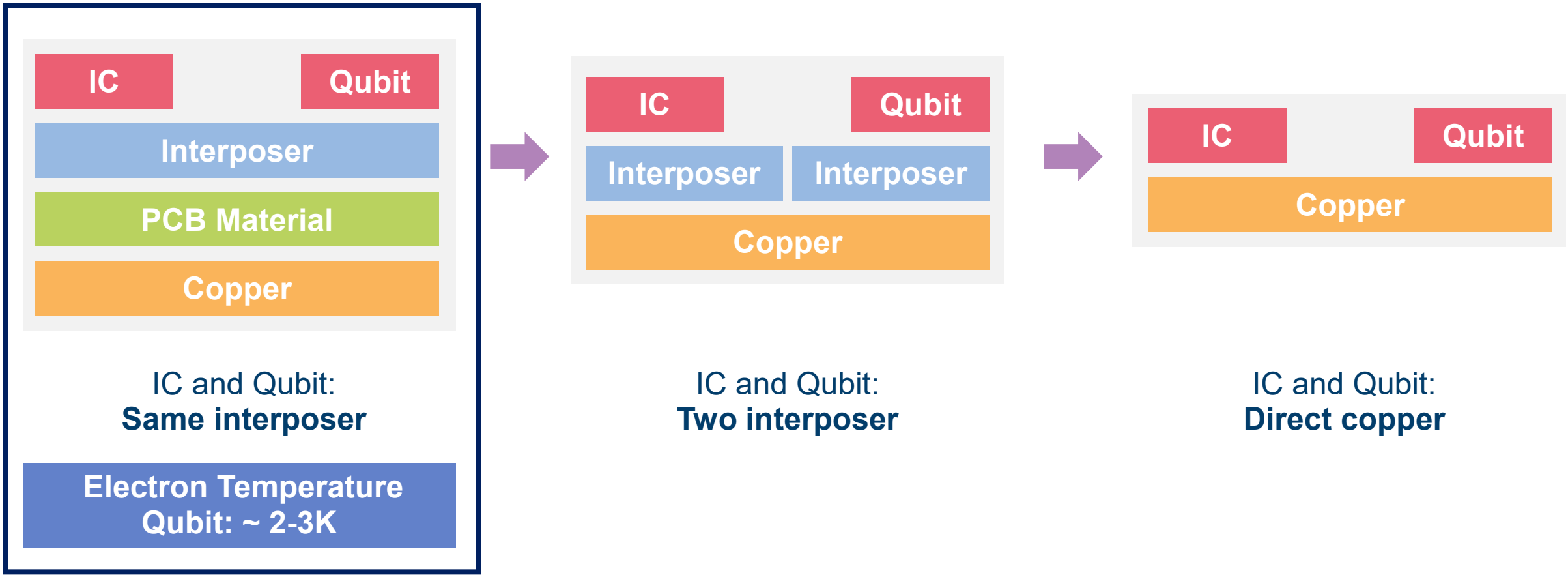
SETUP ITERATIONS



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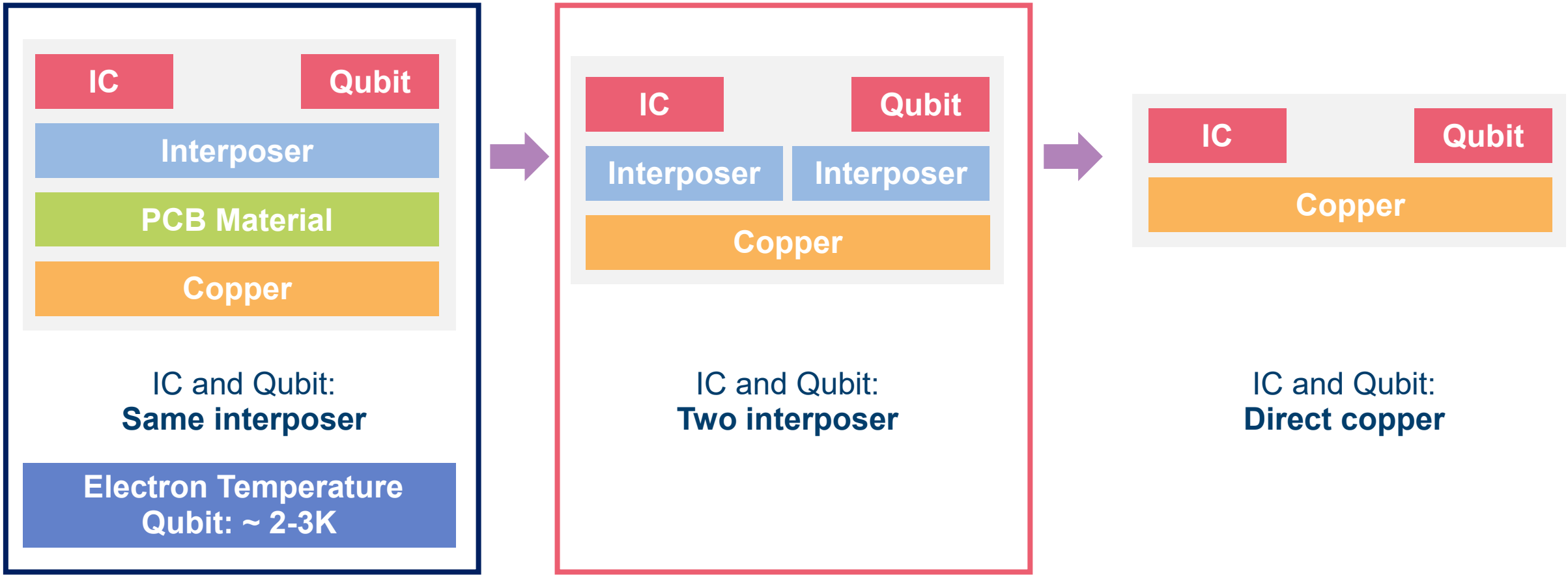
SETUP ITERATIONS



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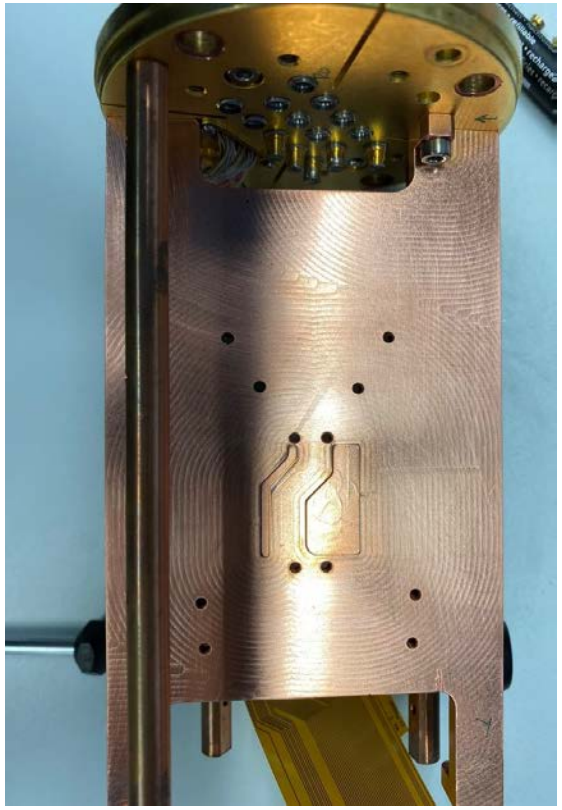
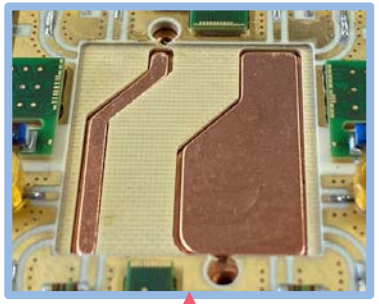
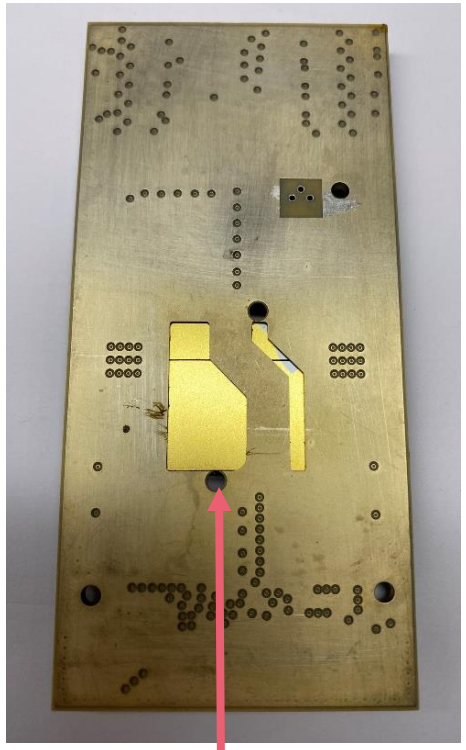
IC AND QUBIT: DIVIDED INTERPOSER

Mother – Daughter Board Solution

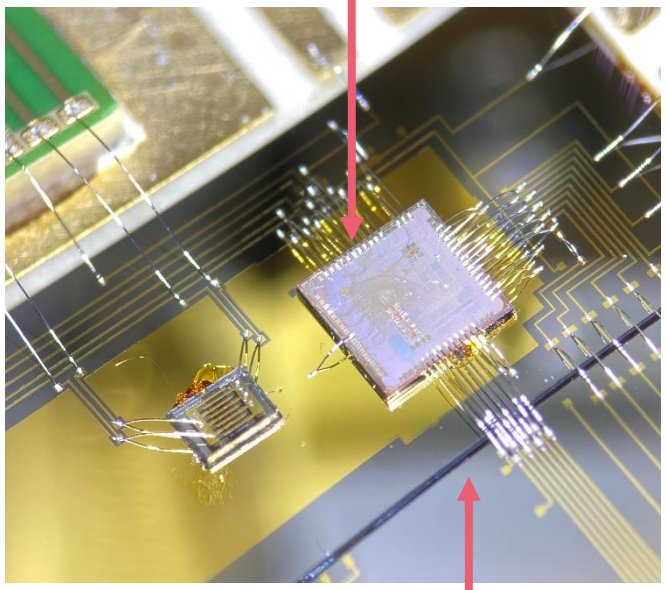






Removed PCB Material

Bare Die Bias-DAC

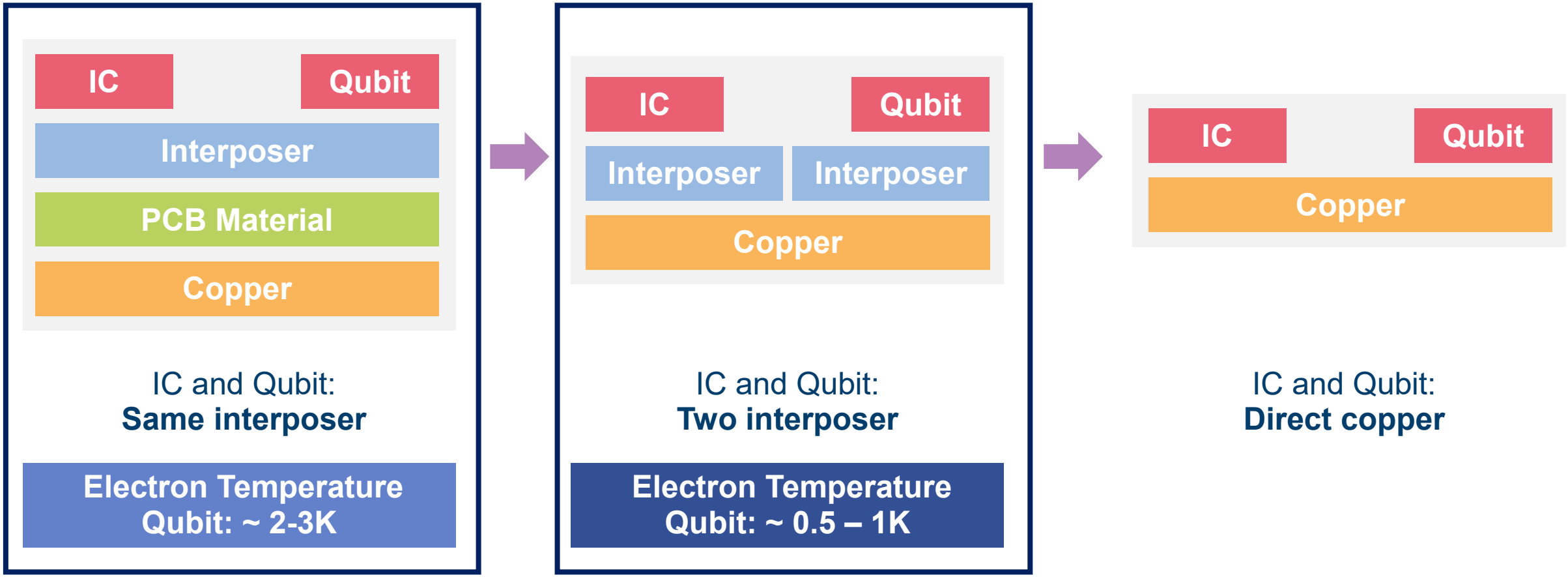


Divided Interposer

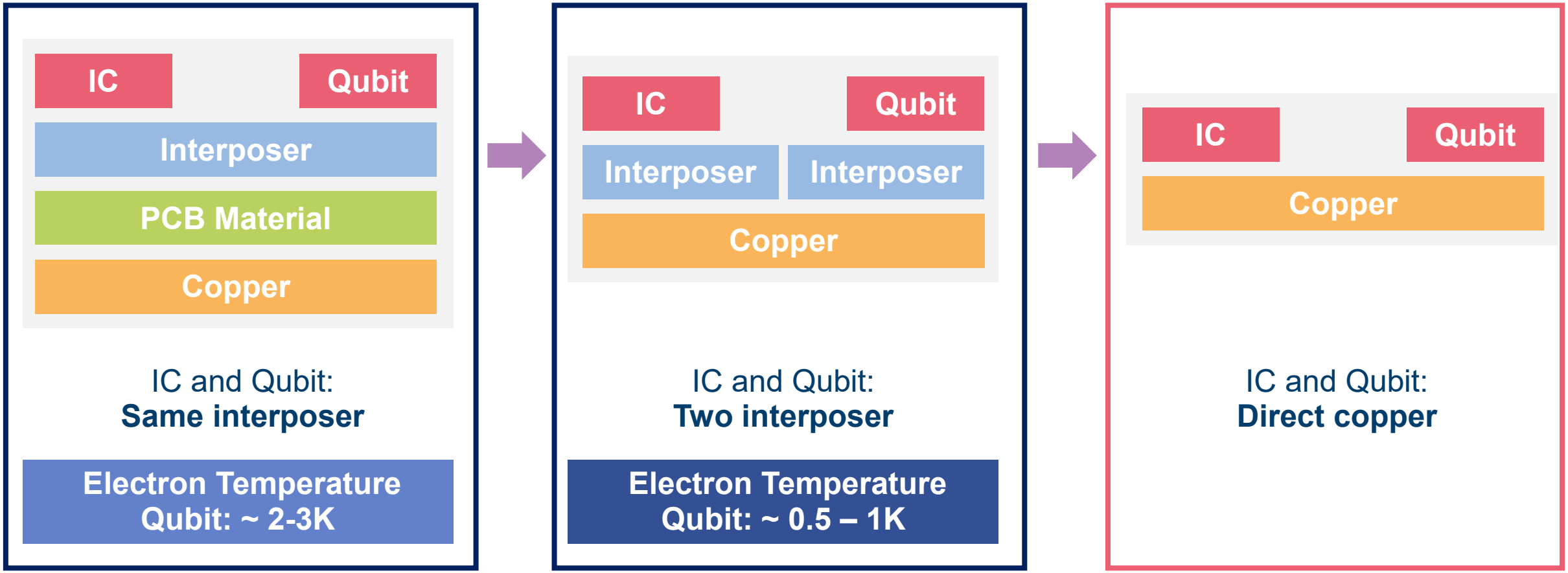
IC | Qubit | Interposer | Interposer | Copper

R. Otten, L. Schreckenberg, et al. "Qubit Bias using a CMOS DAC at mK Temperatures"
2022 29th IEEE International Conference on Electronics, Circuits and Systems ICECS, IEEE, 2022

SETUP ITERATIONS



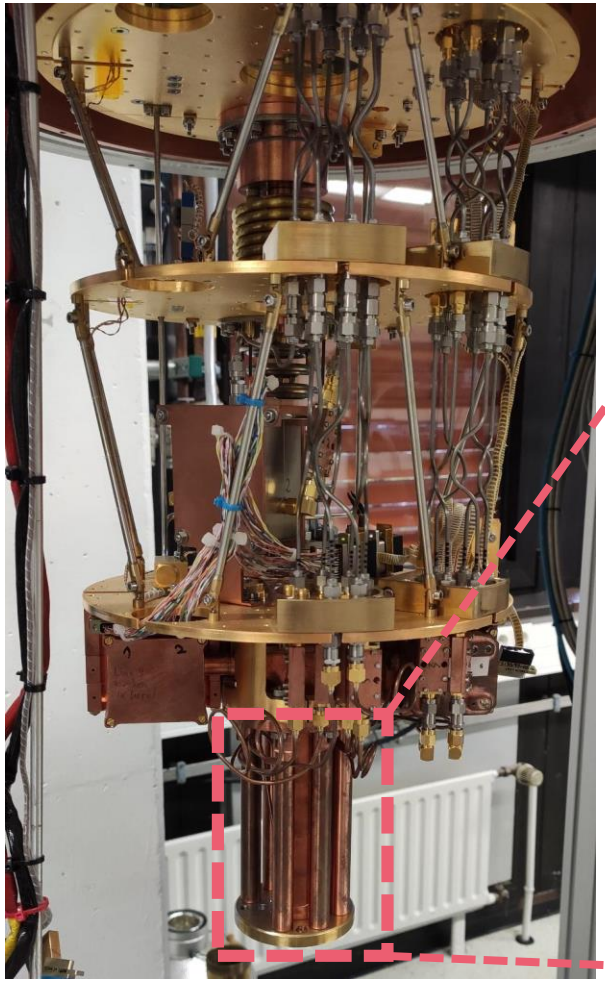
SETUP ITERATIONS



PCB WITH CUT OUT SOLUTION

IC | Qubit

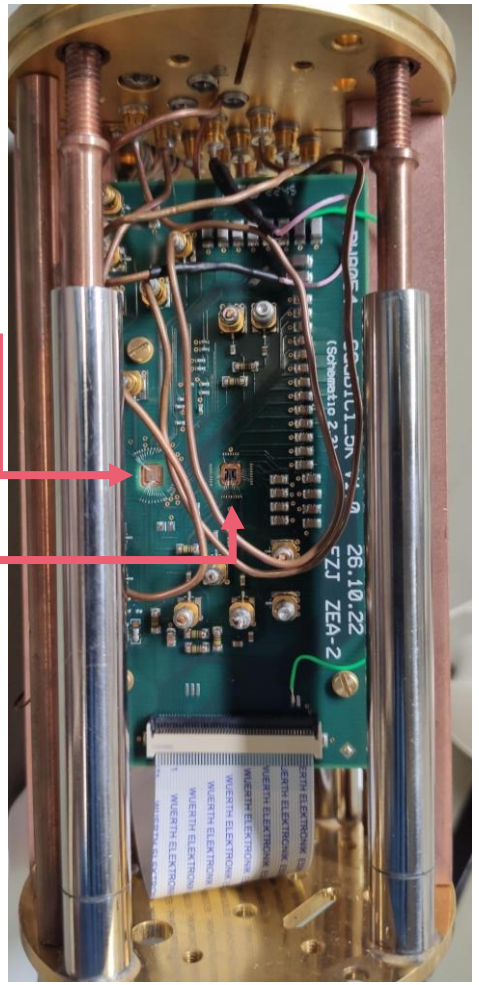
Copper



Rox Sensor

Cryo DAC

Qubit



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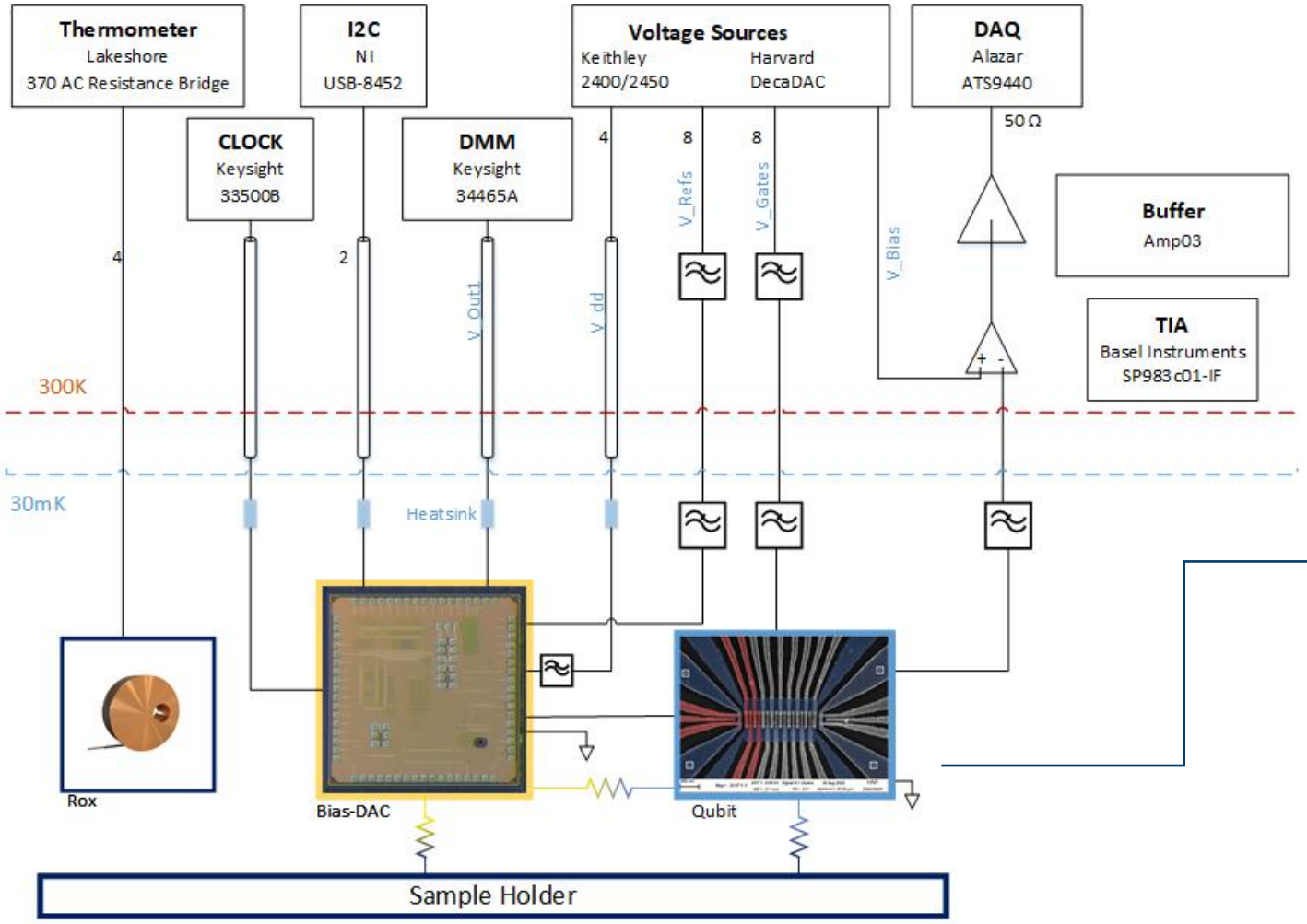
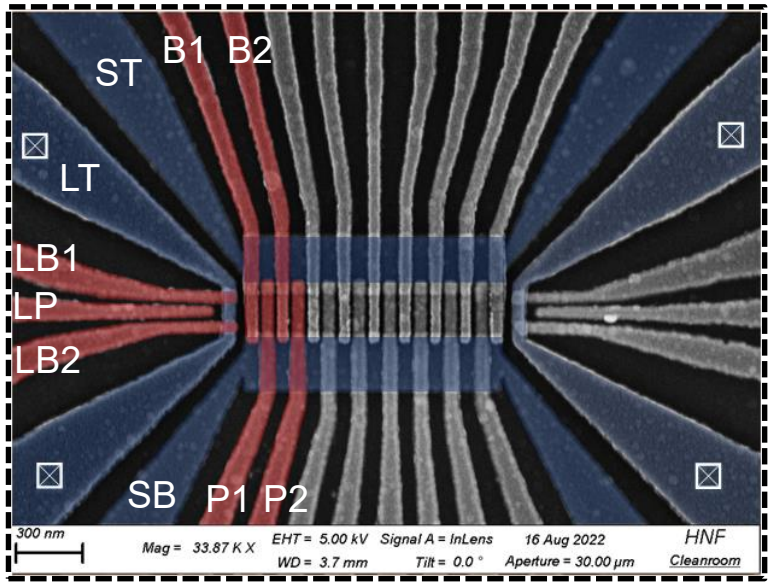
SETUP AND WIRING

IC | Qubit | Copper

Cryostat – PCB – Qubit Device



Si/SiGe Architecture [5]



Cryo DAC

RT DAC

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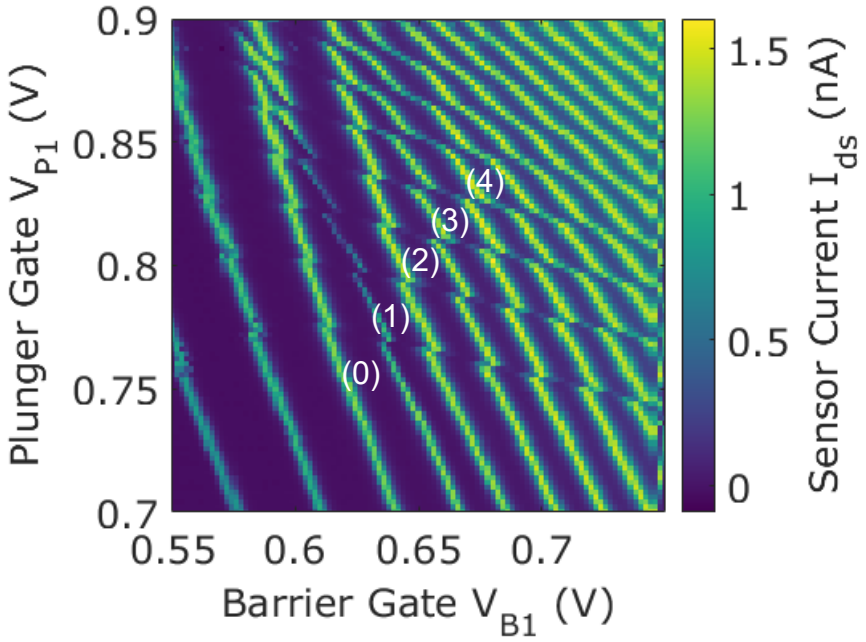
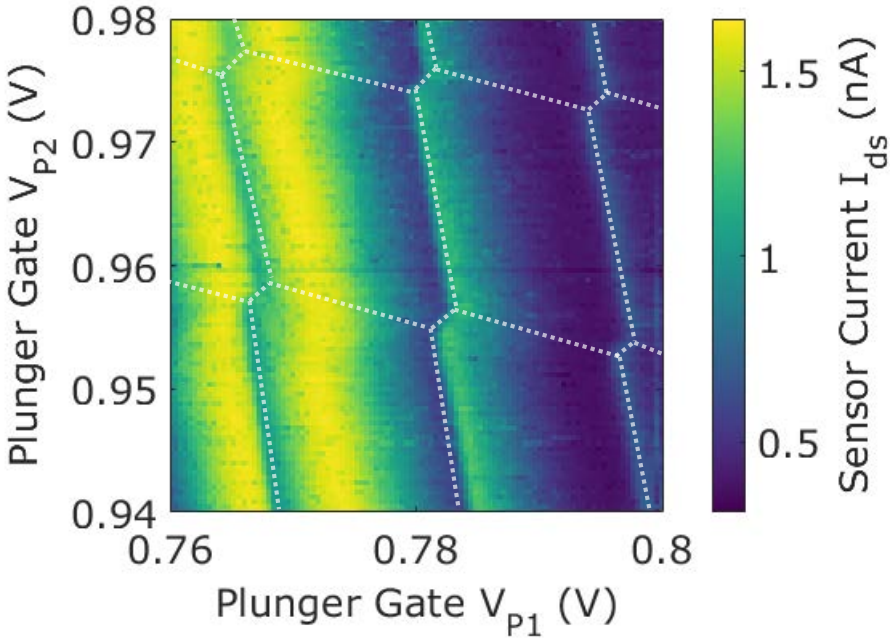
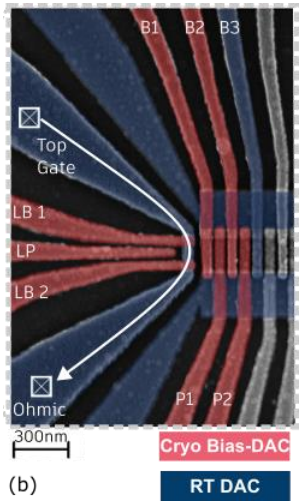
CHARGE SENSING

Single and double Quantum Dot underneath P1 and P2 with DC bias of Cryo-DAC







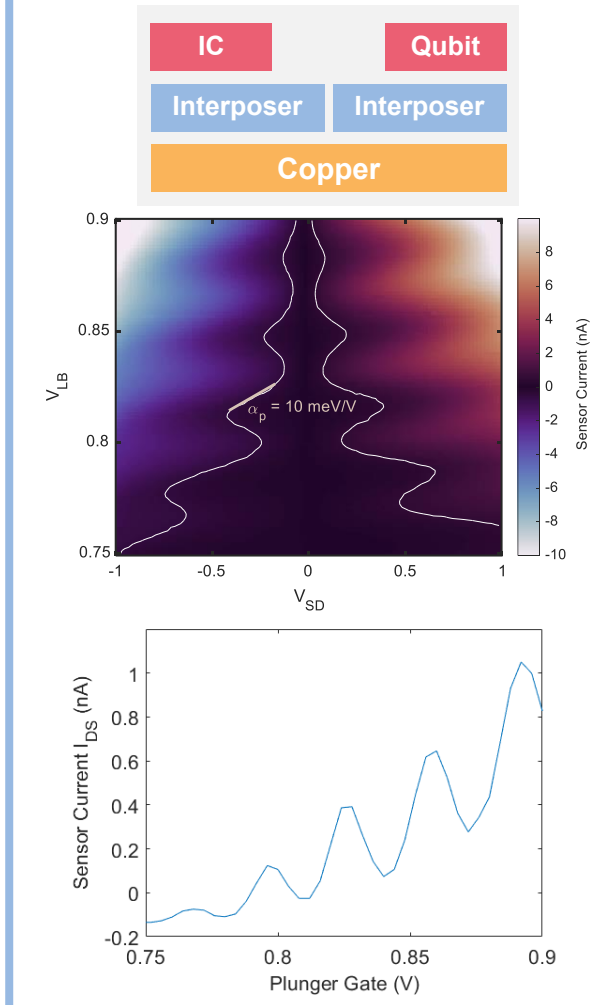
Inter-dot transition and honeycomb pattern is clearly visible

L. Schreckenberg, R. Otten, et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023, pp. 161-164, doi: 10.1109/ESSCIRC59616.2023.10268801.

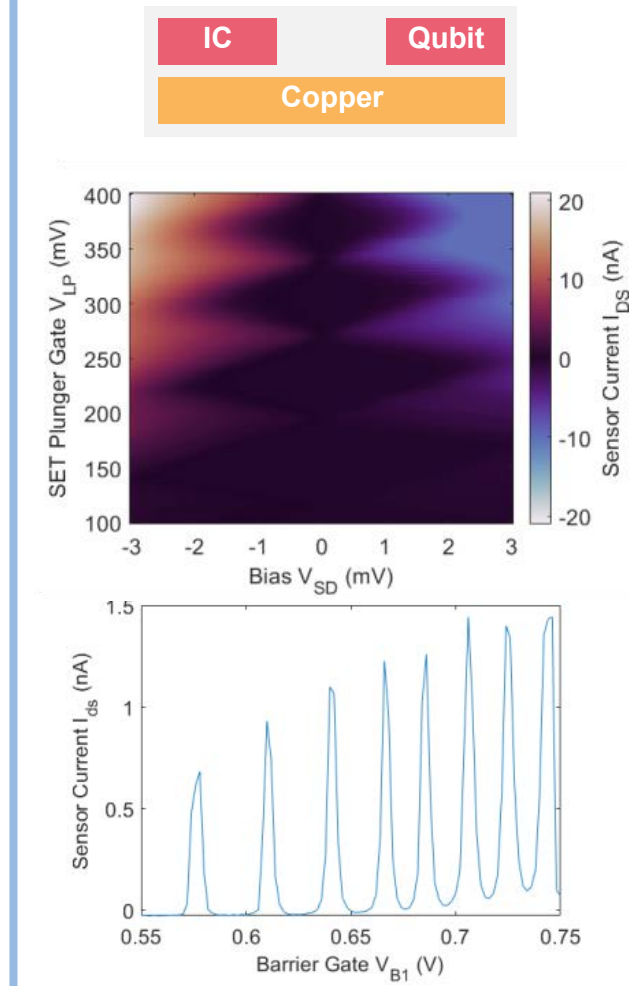
SETUP COMPARISON

	Interposer	Divided Interposer	Direct Copper
Power Consumption	~ 40 uW	30 uW	40 uW
Rox MC		37 mK	44 mK
Cernox Interposer		965 mK	-
Rox Sample Holder		-	180 mK
Electron Temp.	~ 2-3 K	~ 0.5 -1 K	~ 400 mK

Divided Interposer [4]

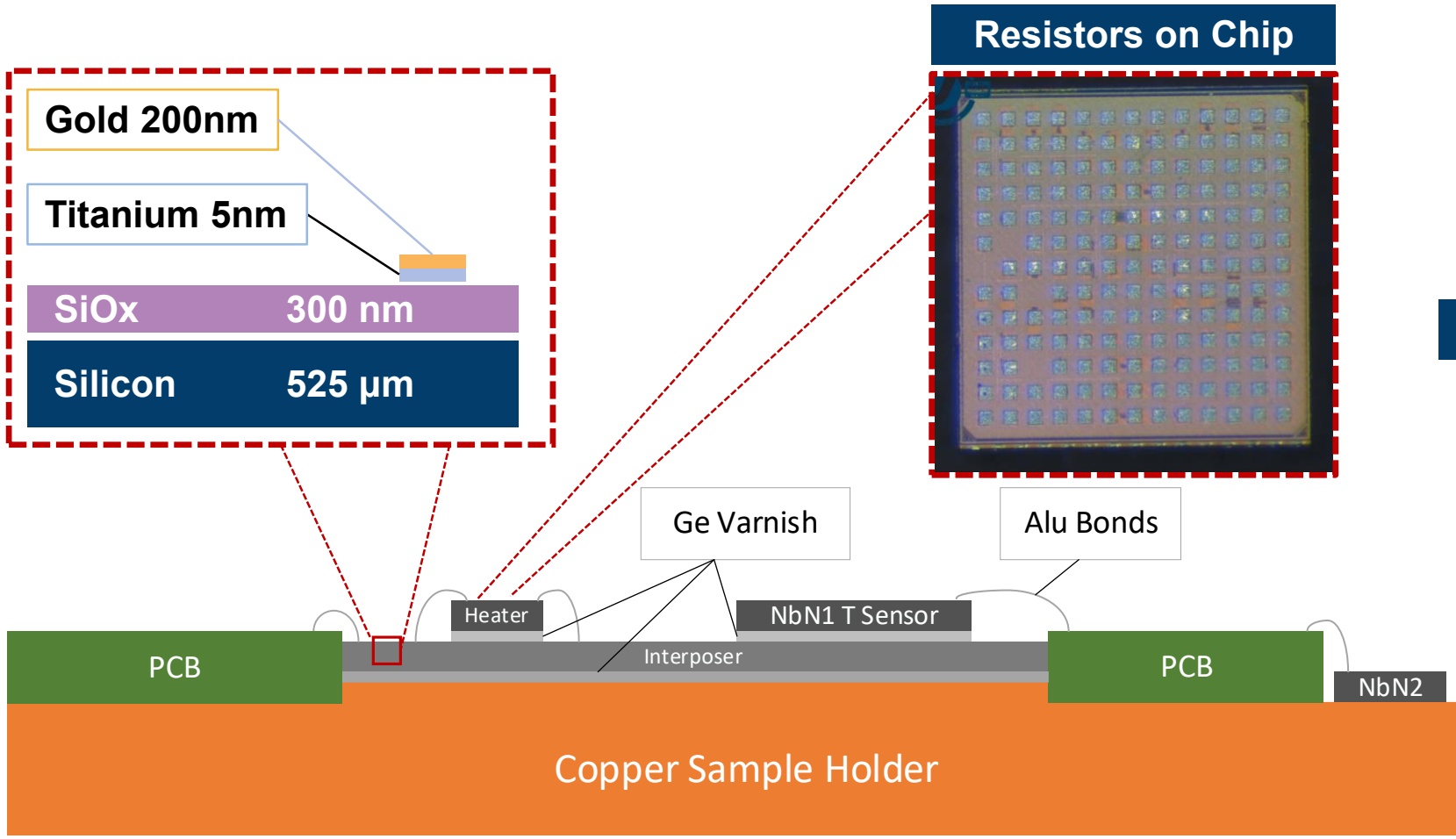


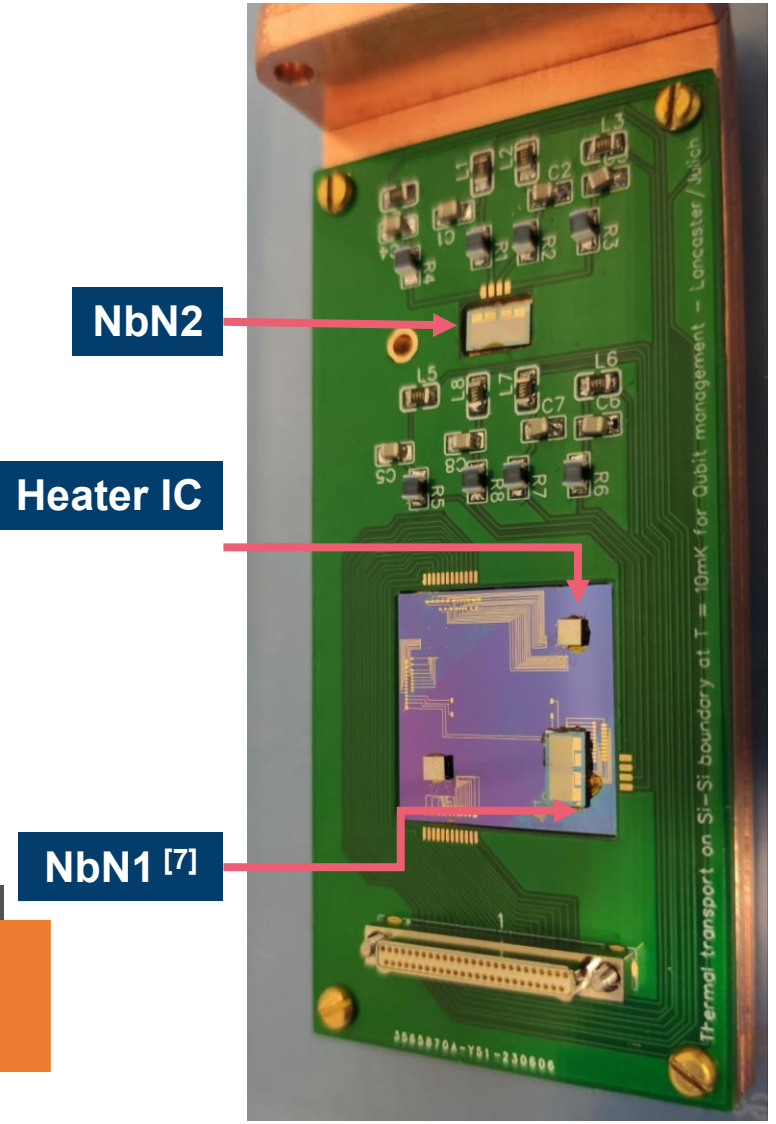
Direct Copper [6]



HEAT DISTRIBUTION MEASUREMENT

EMP Project with University of Lancaster

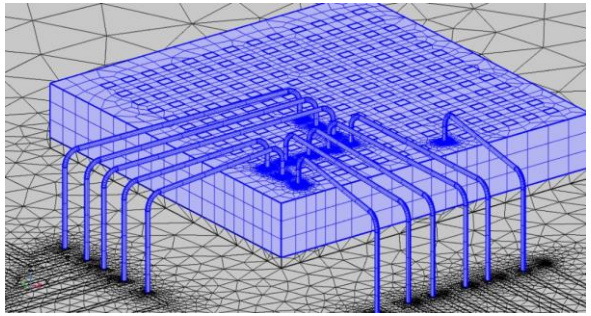




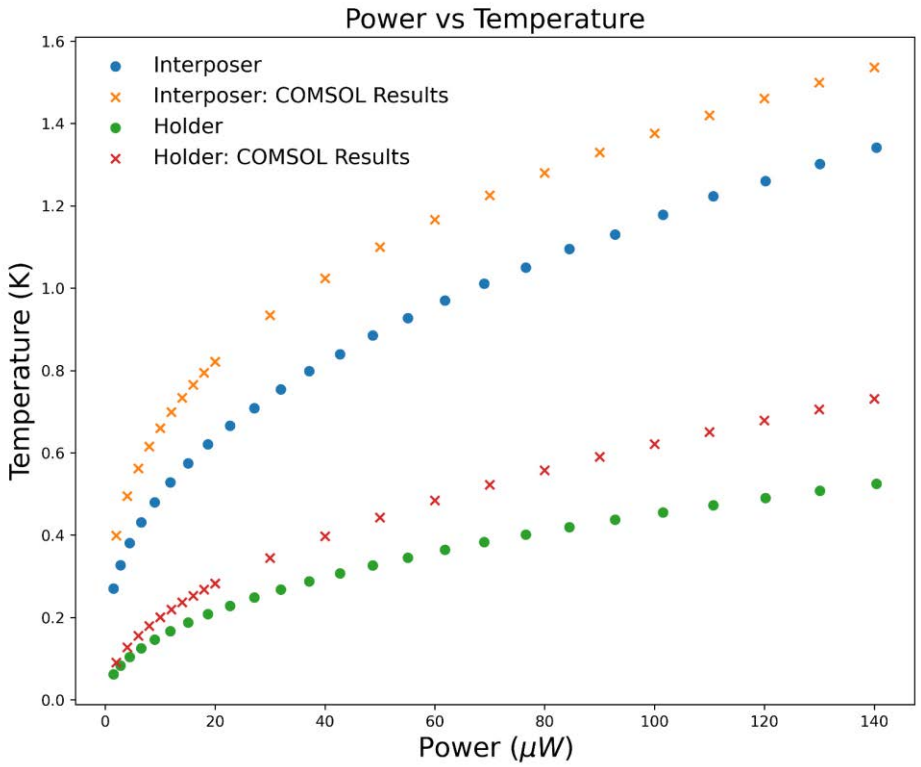
Appreciate funding of EMP Grant for project: Thermal Management of Cryogenic Electronics for Quantum Applications. See: https://emplatform.eu/

MODELLING AND SIMULATIONS

Proof-of-concept of using a FEM engine to solve PDEs in cryogenics

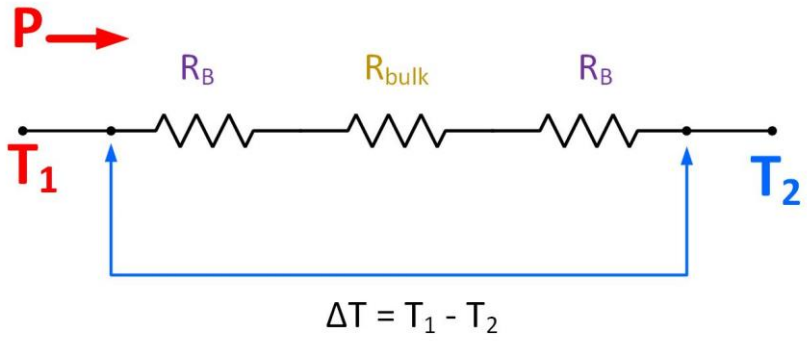


- COMSOL Model with Data from measurement and literature
- Thermal conductivity is temperature dependent
- Fit functions of thermal resistance from measurements obtained at cryogenic environment



THERMAL BOUNDARY RESISTANCE

Resistance between Interfaces due to surface effects

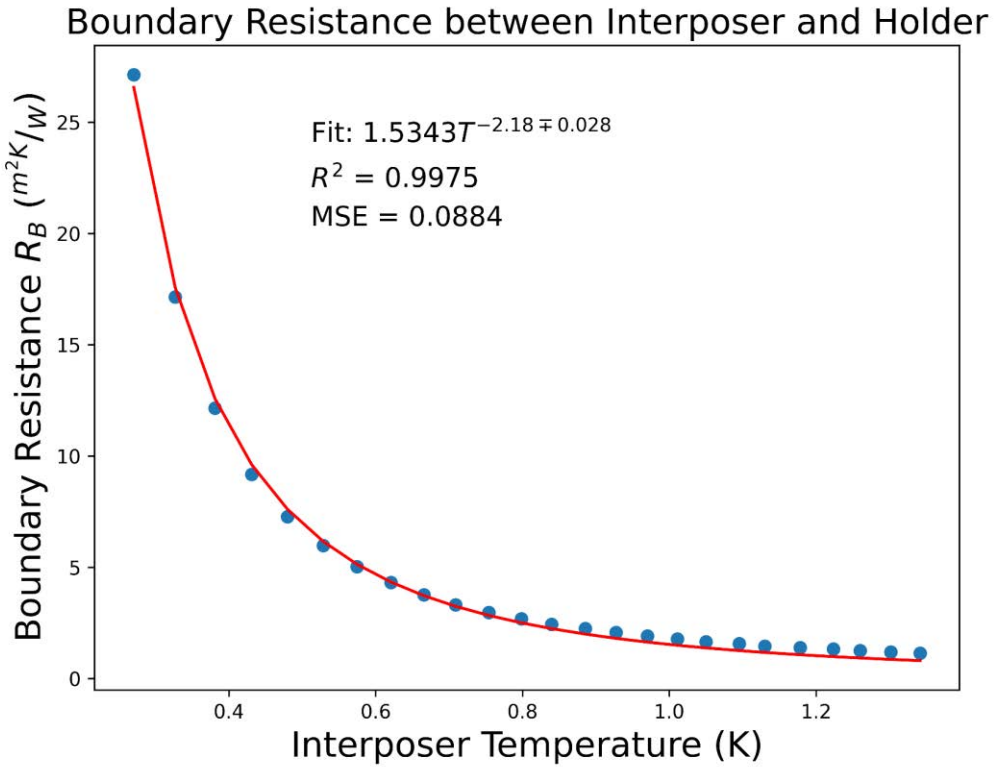


Bulk properties like defects or thickness do not affect TBR

TBR for dissimilar materials[8,9]:

$$T \ll 1K: \; R_B = \alpha T^{-3}$$

$$T \approx 1K: \; R_B = \alpha T^{-2}$$



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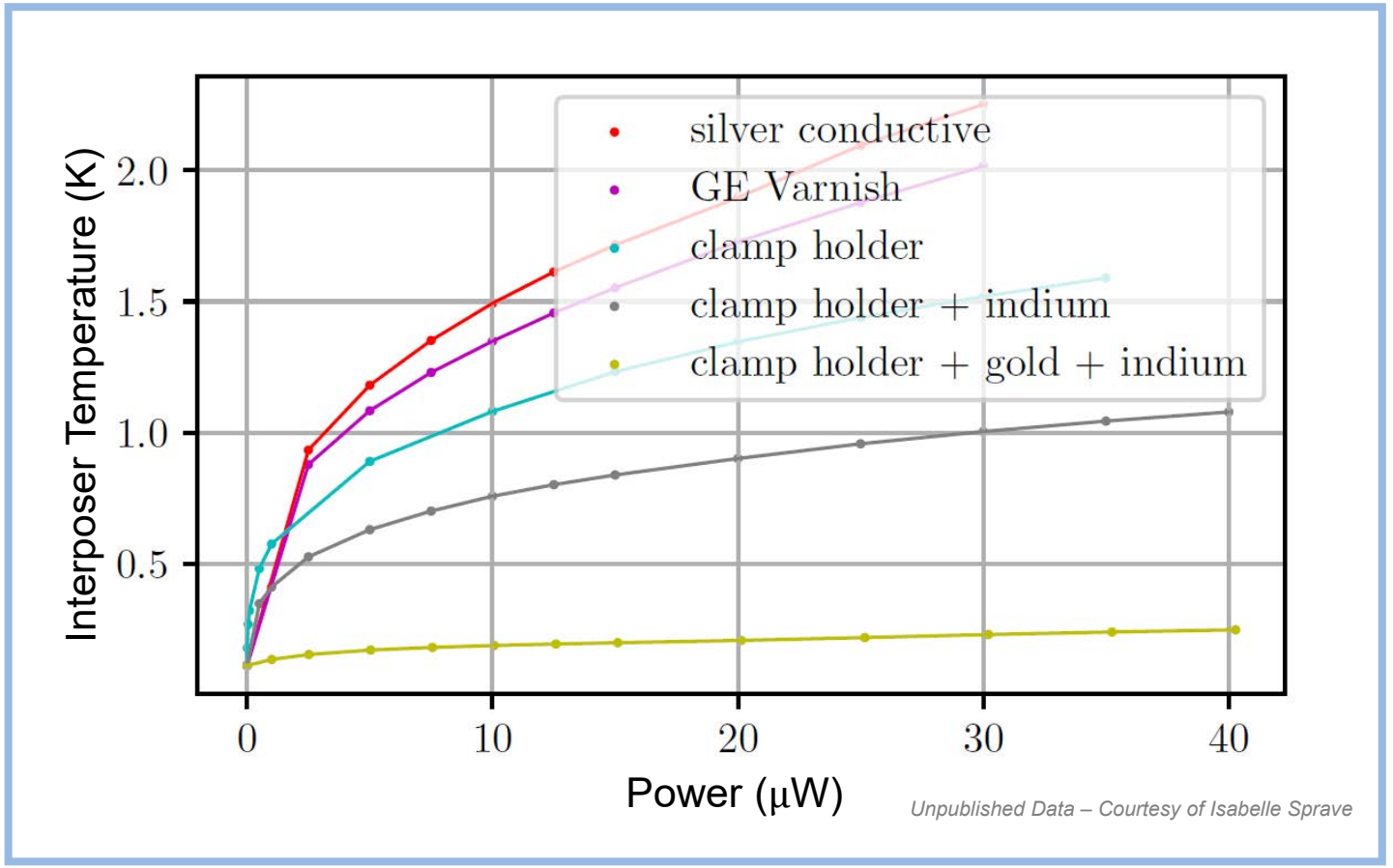
CONCLUSION AND OUTLOOK

- Successful co-integration at 44 mK MC temperature
- Presented a DC qubit bias with charge sensing of electrons in the quantum dot
- Cryogenic modelling and heat distribution measurements to understand the material behavior at cryogenic temperatures
- Packaging and thermal management is an underestimated topic but very important for cryogenic ICs



THANK YOU!

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George Ridgard
Mike Thompson
Jon Prance

Institut NEEL, Univ. Grenoble Alpes
Olivier Bourgeois
Victor Doebele

Helmholtz Nano Facility (HNF), Forschungszentrum Jülich:
Ran Xue
Stefan Trellenkamp

JARA Institute for Quantum Information, RWTH Aachen University & Forschungszentrum Jülich:
Rene Otten
Isabelle Sprave
Hendrik Bluhm

REFERENCES

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[2] Pauka et al. “A cryogenic CMOS chip for generating control signals for multiple qubits,” Nature Electronics, Springer Science and Business Media LLC, 2021, 4, 64-70

[3] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

[4] R. Otten et al. "Qubit Bias using a CMOS DAC at mK Temperatures,“ 2022 29th IEEE International Conference on Electronics, Circuits and Systems ICECS, IEEE, 2022

[5] I. Seidler, T. Struck, R. Xue et al., ”Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture,” npj Quantum Inf 8, 100, 2022.

[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023, pp. 161-164, doi: 10.1109/ESSCIRC59616.2023.10268801.

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