NARLabs
National Applied Research Laboratories

A Member of NARLabs
Taiwan Semiconductor Research Institute

Challenges of Cryogenic CMOS Controller for Qubits

Chia-Hsin Lee

Oct. 25th 2023

NARLabs

Outline

- System Specs and Process Selection
- Device Behavior
- Problems on Design
  - Digital Circuits
  - Analog/RF Circuits
- Current Progress
- Measurement Environment
- Summary

NARLabs

System Specs and Process Selection

To control spin qubits [1]:

- High performance RF signals for 99.99% fidelity
  - Frequency: ~18 GHz
  - Pulse duration: < 100 ns
  - SFDR: > 44 dB
  - SNDR: > 44 dB (in 25 MHz bandwidth)
- Low power budget
  - < 10 mW/channel

NARLabs

System Specs and Process Selection

Need an integrated cryogenic digital controller

→ **CMOS**:

- scalable integration (++)
- Function at 4 K (+)
- Not optimized for cryo-operation (−)
- No mature cryo-models (−−−)

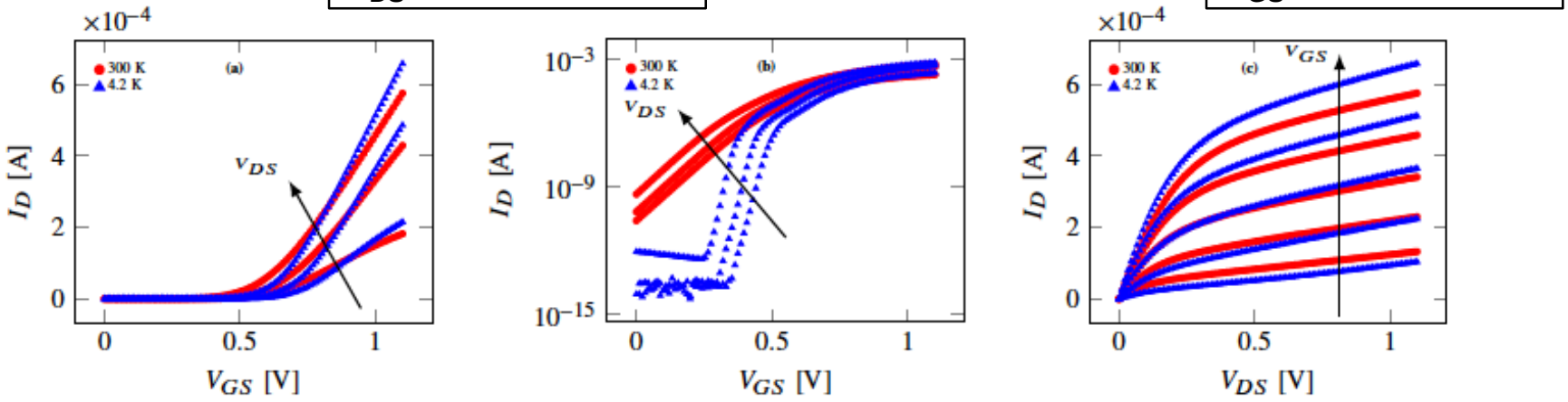
Device Behavior — Transistor IV

At 4 K [2]:

- V_{th} ⬆
- $I_{D(sat)}$ ⬆ when V_{GS} > 0.9 V
  ($I_{D(sat)\text{-}4\ K}$ ~ $I_{D(sat)\text{-}RT}$ when V_{GS} ~ 0.8 V)
- I_{sub} ⬇, and steeper subthreshold slope

V_{DS} = 0.1, 0.4, 1.1 V

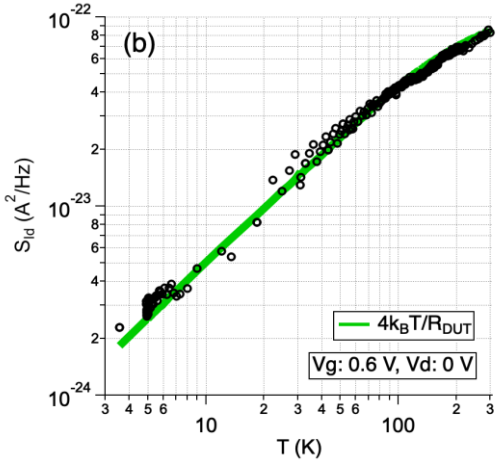
V_{GS} = 0.7:0.1:1.1 V



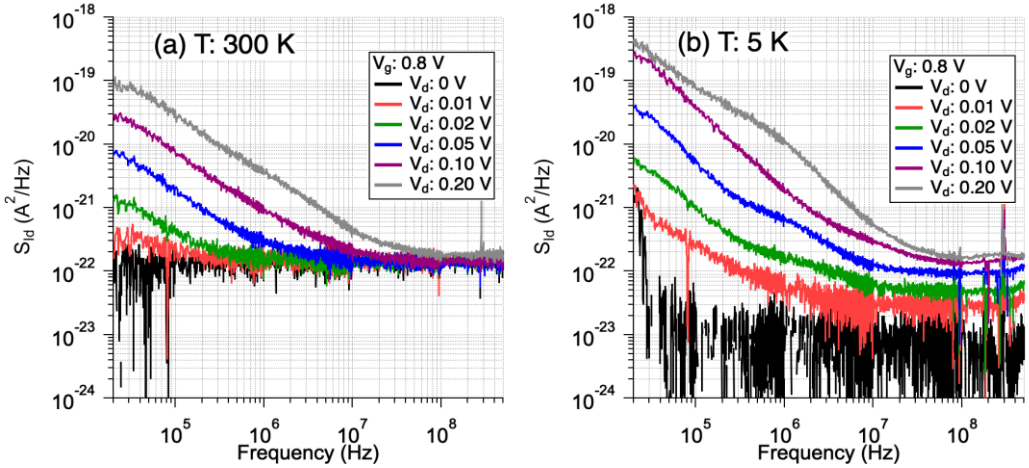
Device Behavior — Transistor Noise

- Thermal noise decreases at 4 K
- The effect of flicker noise increases at 4 K

Ref: [3]



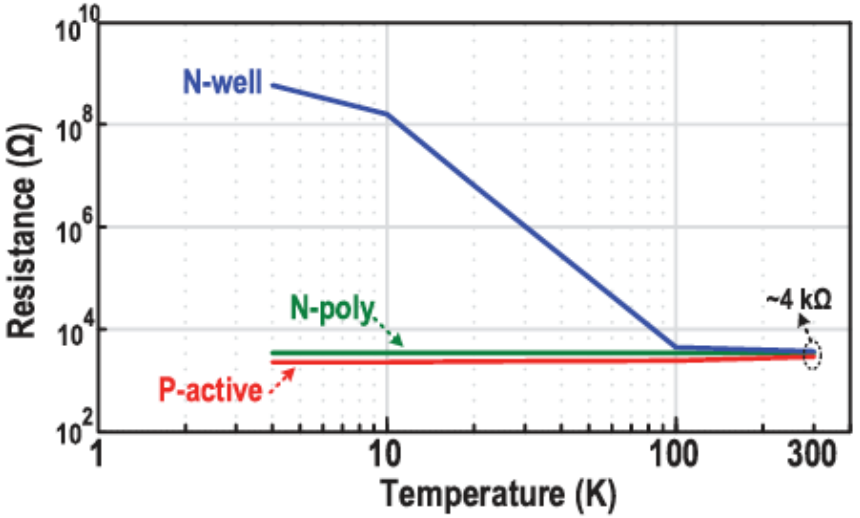
Average S_{Id} v.s. T
→ consistent with $4k_BT/R$

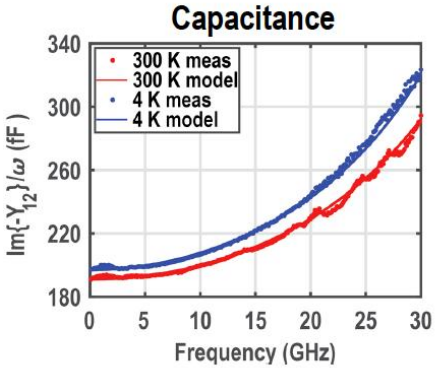


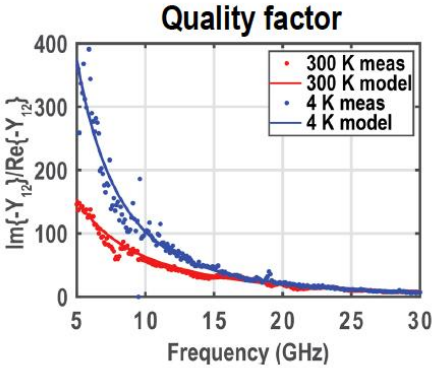
S_{Id} at (a) 300 K and (b) 5 K
→ 1/f noise increase at 5 K

Device Behavior — Resistor & Capacitor

- Resistors [4]
  - N-well: increase by several orders of magnitude
  - N-poly & P-active: have better temperature stability (~ 20%)
- MOM capacitor [5]
  - Slight increase (~5%), with better Q value below 10 GHz



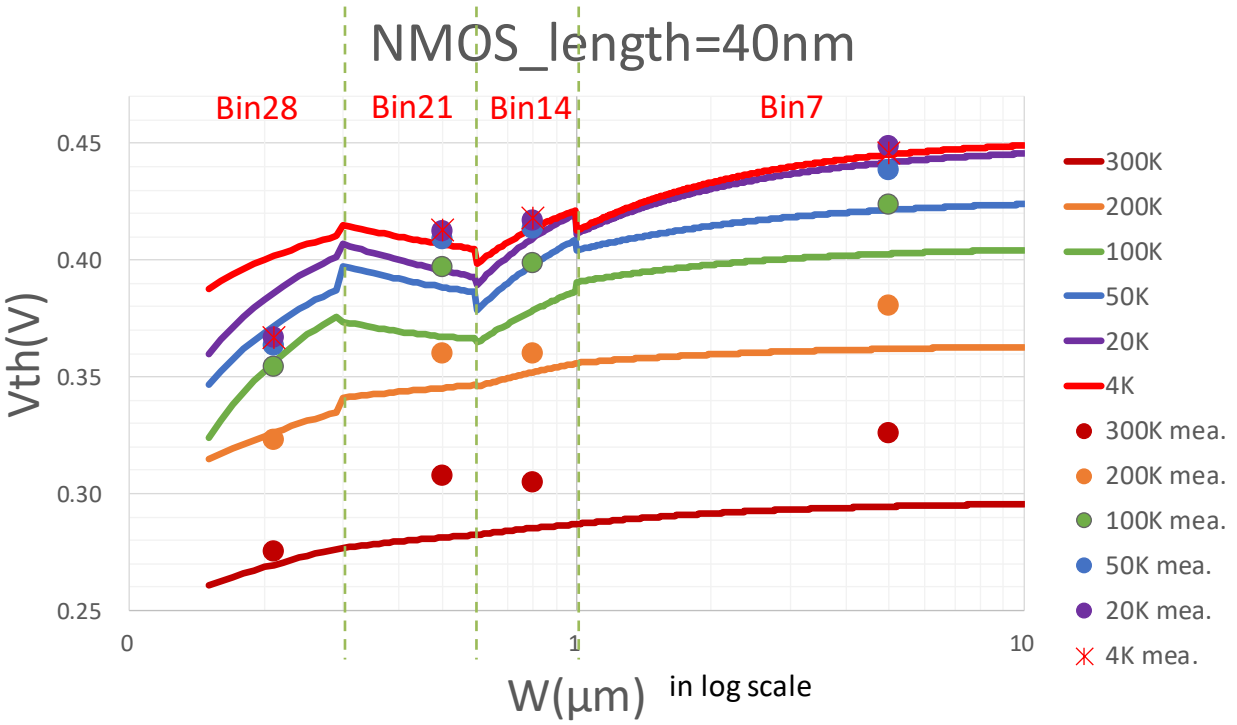




Device Behavior — Modeling Issue

4 K device model fitting

→ Current BSIM4 model is not adequate for 4 K model fitting at small length/width



NARLabs

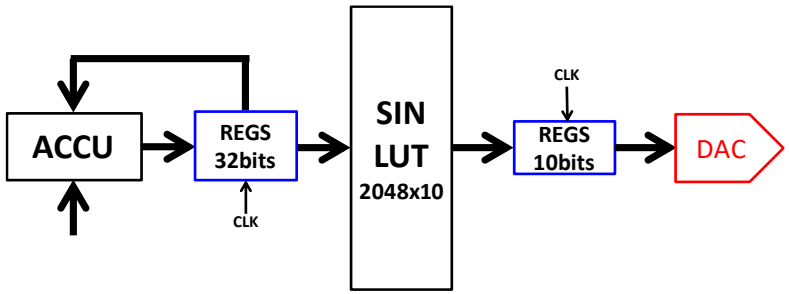
Problems on Design

- Digital Circuits
- Analog/RF Circuits

Digital Circuits — Issue

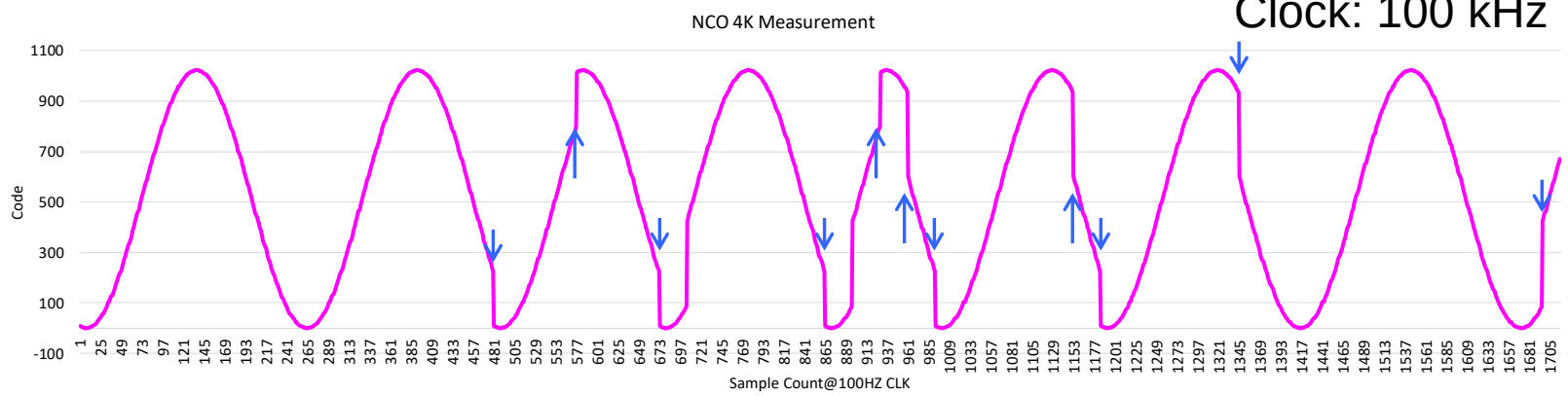
At 4 K, timing is a big issue for digital circuit due to

- Transistor I_{on} ⬆ → gate propagation delay t_{PD} ⬇
- Routing resistance ⬇ → RC delay t_D ⬇



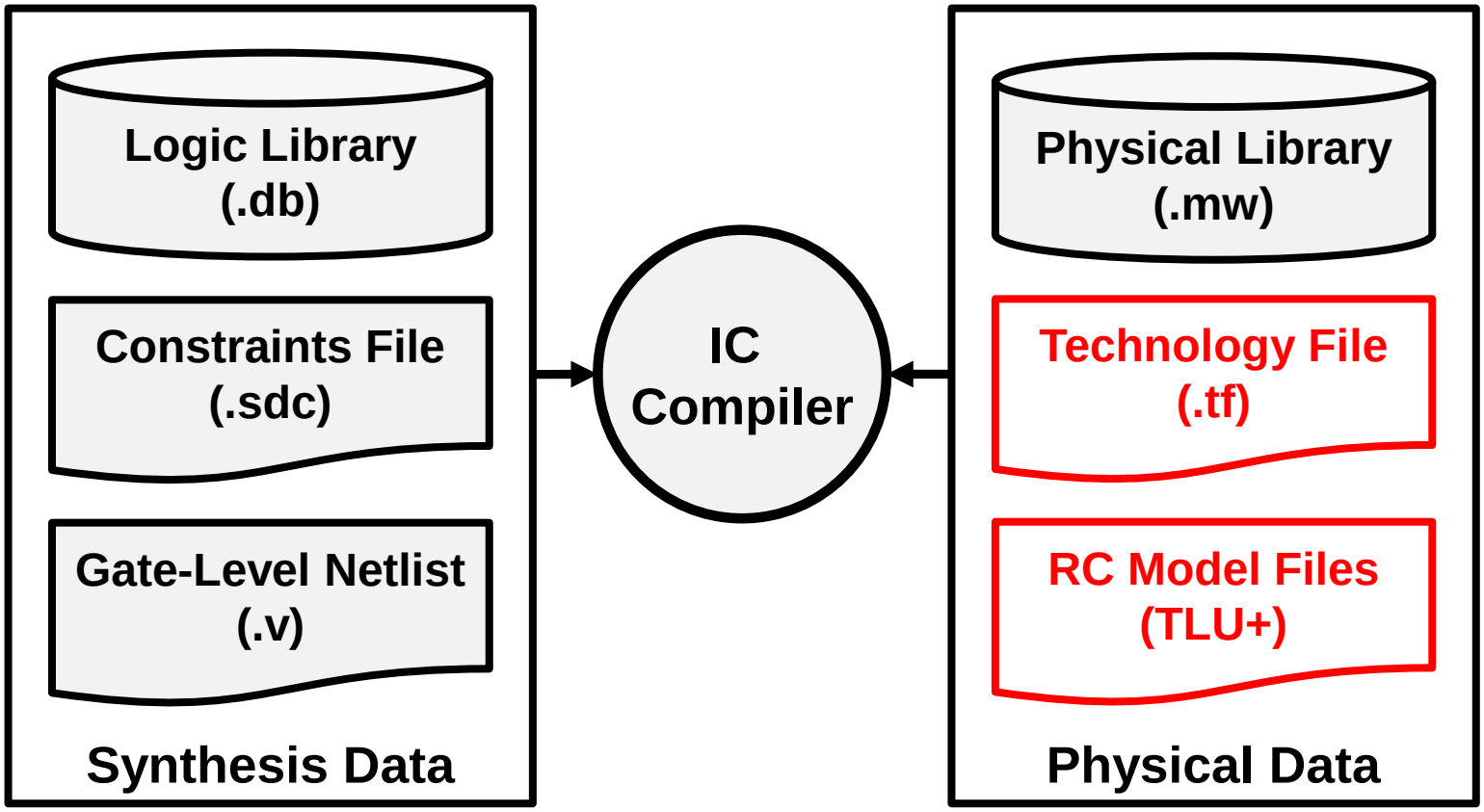
Hold-time violation!

Clock: 100 kHz



Digital Circuits — Solution (1)

Modify physical design input files



Digital Circuits — Solution (1)

- Technology file: two approaches
  - 134 categories, 1024 cells, and 1,583,077 data points

- RC Model file: modify TSMC iRCX → TLU+ conversion
  - R: ~4.3x ↓ from 300 to 4 K
    (Refer to measured M1~M5 testkey data)
  - C: little change at 4 K

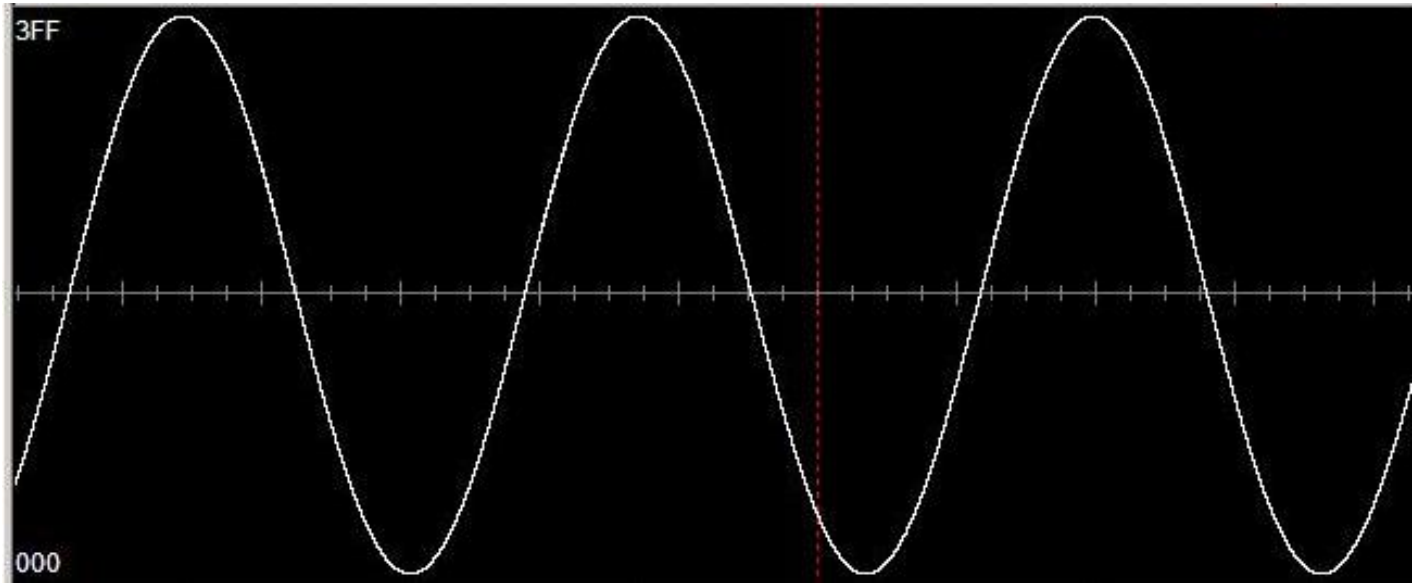
  → Estimated t_D: 4.6x faster from 300 to 4 K

Digital Circuits — Solution (2)

Pipelined design: reduce accumulation of t_{PD} and t_D

→ Relax accumulated timing error between 4 K and 300 K

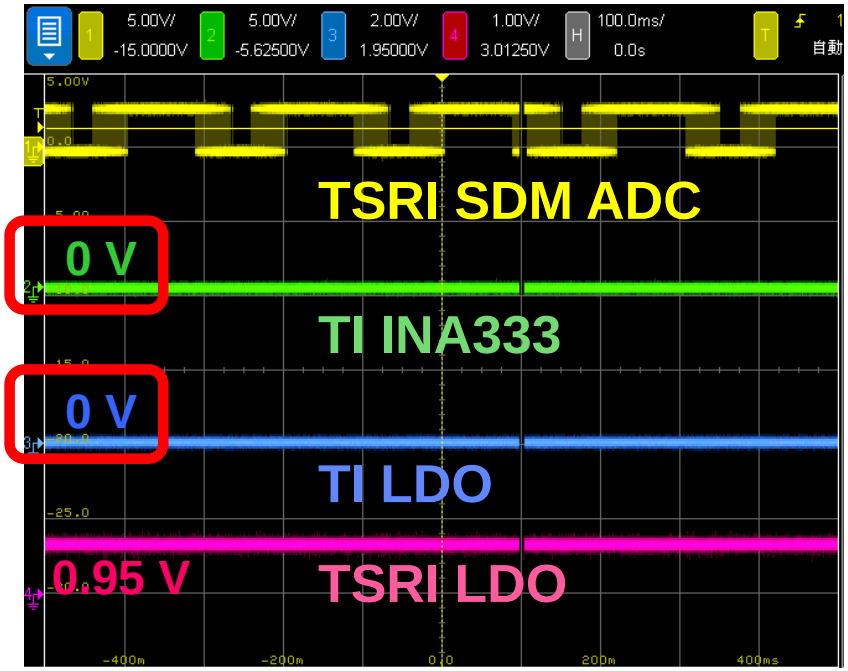
Clock: 100 kHz



Analog/RF Circuits — Issue

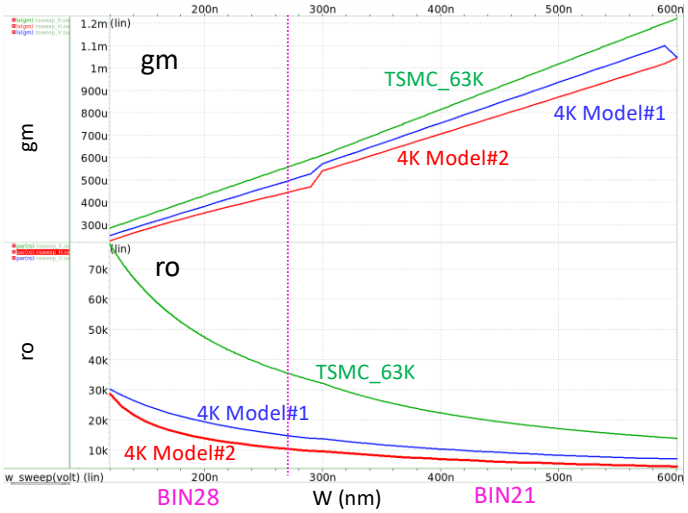
- Biasing
- Performance estimation
- Latch-up
- Power management

Chip malfunction due to
PMIC (BJT) fail at 4 K



Analog/RF Circuits — Solution

- DC biasing
  - Set simulation ***T*** = -200°C for TSMC 40 nm process (before 4 K model ready)
  - 4 K device modeling (IV curve fitting)
- AC performance
  - Set RC extraction ***T*** = -269°C
  - External tuning in prototype chips
  - 4 K device modeling (AC parameters)

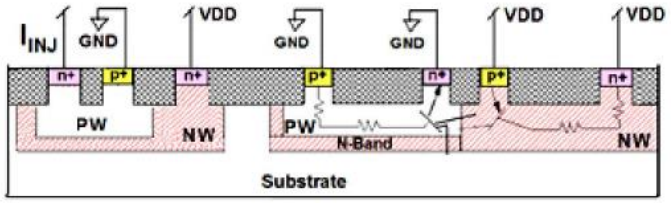


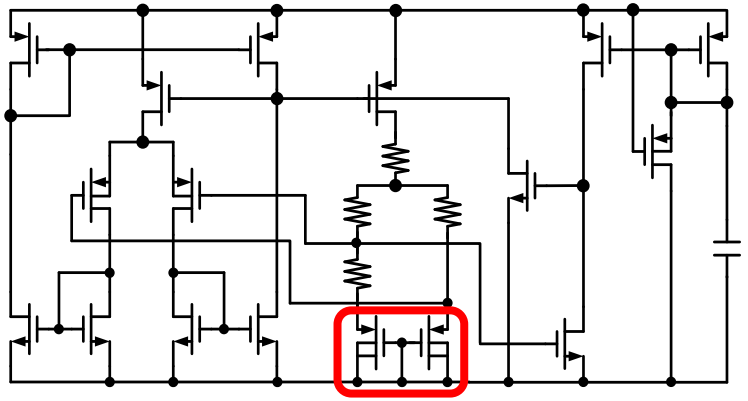
4K device Modeling (gm, ro)

Analog/RF Circuits — Solution

- Latch-up and PMIC design
  - Increase device spacing/guard ring width to lessen latch-up hazard [6]
  - Be aware of the area size of multiple wells
  - Never use bipolar devices (bandgap reference circuit)

Ref: [7]



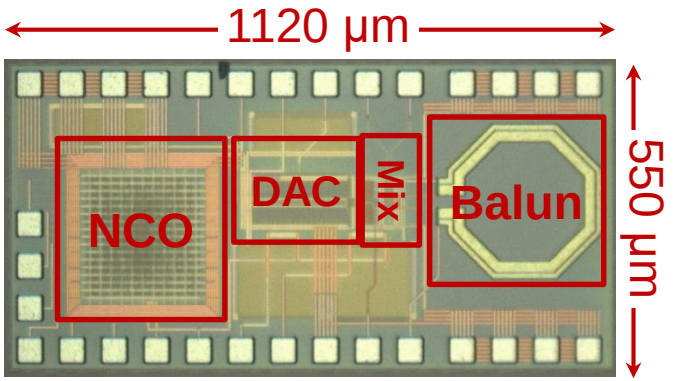


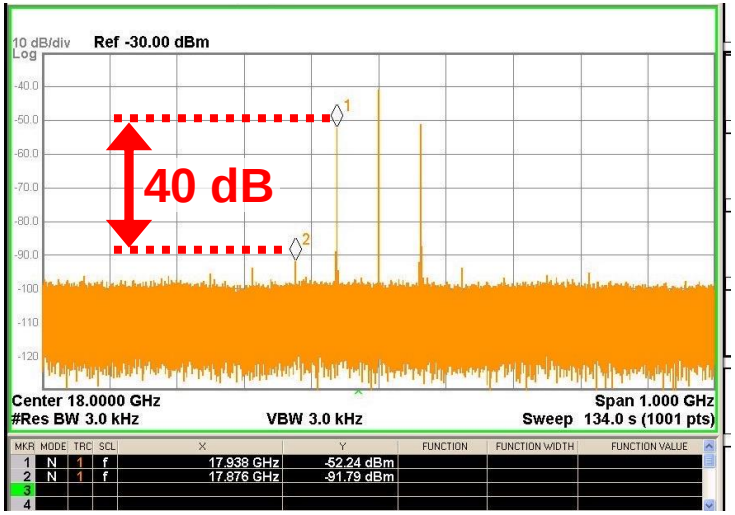
CMOS BGR Circuit

Current Progress

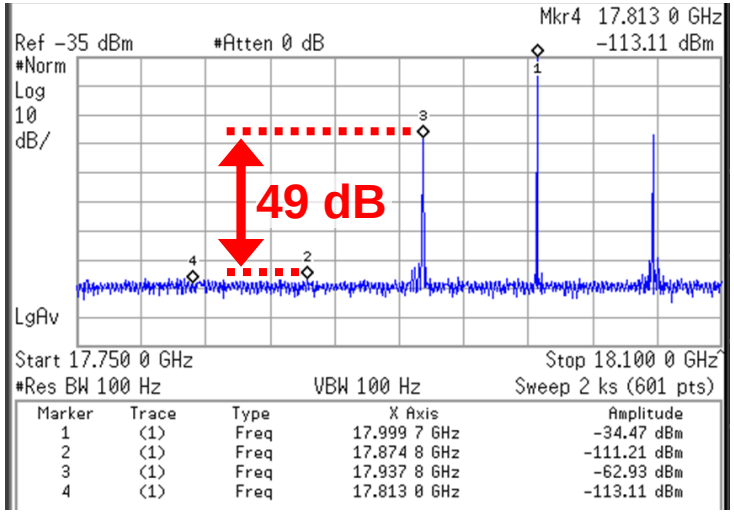
Prototype: NCO + DAC + mixer

f_{LO}	18 GHz
SFDR	40 dB @ 300 K
	49 dB @ 4 K
Area	0.616 mm^2





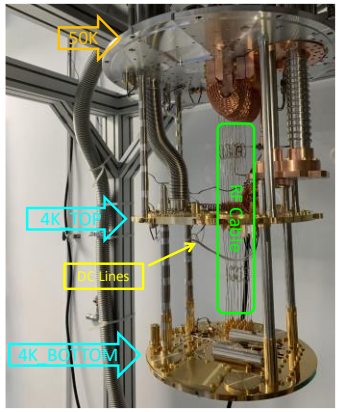
300 K

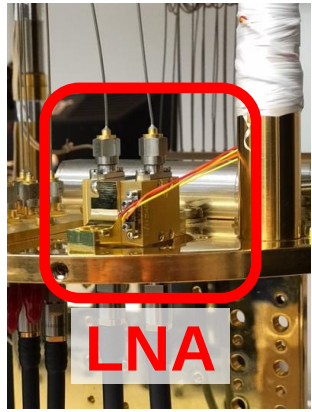


4 K

Measurement Environment

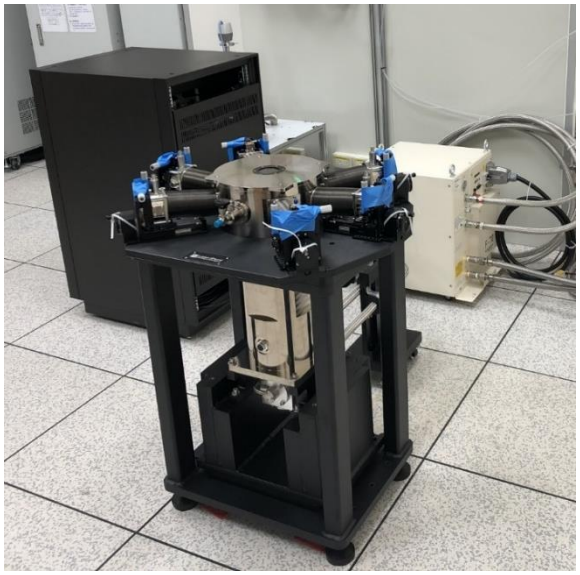
- Cryo-fridge setup: system
  - Min. temperature: 3.2 K
  - Sample holder size: 28×16 cm^2
  - Twist-pair DC lines: 48
  - RF coaxial cables: 32
    (18 GHz ×16, 40 GHz ×16)
  - Temperature sensor:
    System/PCB/Chip
  - Electrical equipment:
    - SMU
    - High speed I/O
    - Pattern generator
    - Scope/Spectrum
    - Signal generator
    - Logic analyzer





Measurement Environment

- Cryo-fridge setup: device
  - Temperature range: 6.5 ~ 350 K
  - sample space: 2”
  - 6 probes (DC×4, RF×2: up to 67 GHz)



NARLabs

Summary

- High performance RF signals and low power dissipation are required for a spin qubit controller
- Cryogenic device model is necessary due to significant changes of device behavior at 4 K
- Problems on design
  - Timing error in digital circuits is relaxed by pipelined design
  - For analog/RF circuits, set simulation temperature to the turning point of transistor variation as a temporary solution
  - Careful layout to prevent latch-up and avoid using BJTs
- Prototype NCO + DAC + mixer chip functions at 4 K (f_{LO} = 18 GHz, SFDR = 49 dB)

NARLabs

Reference

[1] B. Patra *et al*., “A scalable cryo-CMOS 2-to-20 GHz digitally intensive controller for 4×32 frequency multiplexed spin qubits/transmons in 22 nm FinFET technology for quantum computers,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 304–305.

[2] J. Van Dijk *et al*., “Cryo-CMOS for analog/mixed-signal circuits and systems,” in *Proc. IEEE CICC*, Mar. 2020, pp. 1–8.

[3] K. Ohmori and S. Amakawa, “Variable-temperature broadband noise characterization of MOSFETs for cryogenic electronics: from room temperature down to 3 K,” in *7th IEEE EDTM*, Mar., 2023, pp. 1–3.

[4] B. Patra *et al*., “Cryo-CMOS circuits and systems for quantum computing applications,” *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[5] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, “Characterization and analysis of on-chip microwave passive components at cryogenic temperatures,” *IEEE J. Electron Devices Soc.*, vol. 8, pp. 448–456, 2020.

[6] E. Schriek, F. Sebastiano, and E. Charbon, “A cryo-CMOS digital cell library for quantum computing applications,” *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 310–313, Aug. 2020.

[7] D. Kontos *et al*., “Investigation of external latchup robustness of dual and triple well designs in 65nm bulk CMOS technology,” in *Proc. Int. Reliab. Phys. Symp*., Mar. 2006, pp. 145–150.

NARLabs

Thank you for Your Listening

TSRI