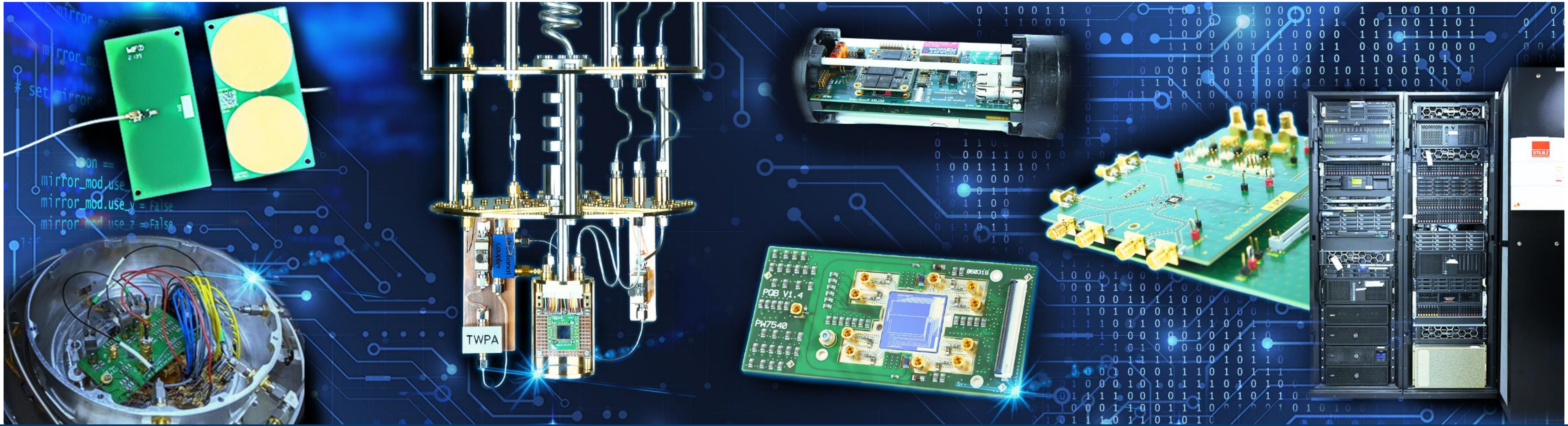


POWER INTEGRITY CHALLENGES IN LARGE SCALE QUANTUM COMPUTERS AND SOLUTIONS

IEEE Workshop on Quantum Computing: Devices, Cryogenic Electronics and Packaging

Milpitas, CA USA

25.10.2023 | A. R. CABRERA-GALICIA, ZEA-2

JÜLICH Forschungszentrum | ZEA-2 Electronic Systems

OVERVIEW

- Motivation
- Power Integrity Challenges for Cryogenic ICs
- Proposed Solution: Cryogenic Voltage Regulation
- Application Case: Voltage References for DAC
- Conclusions

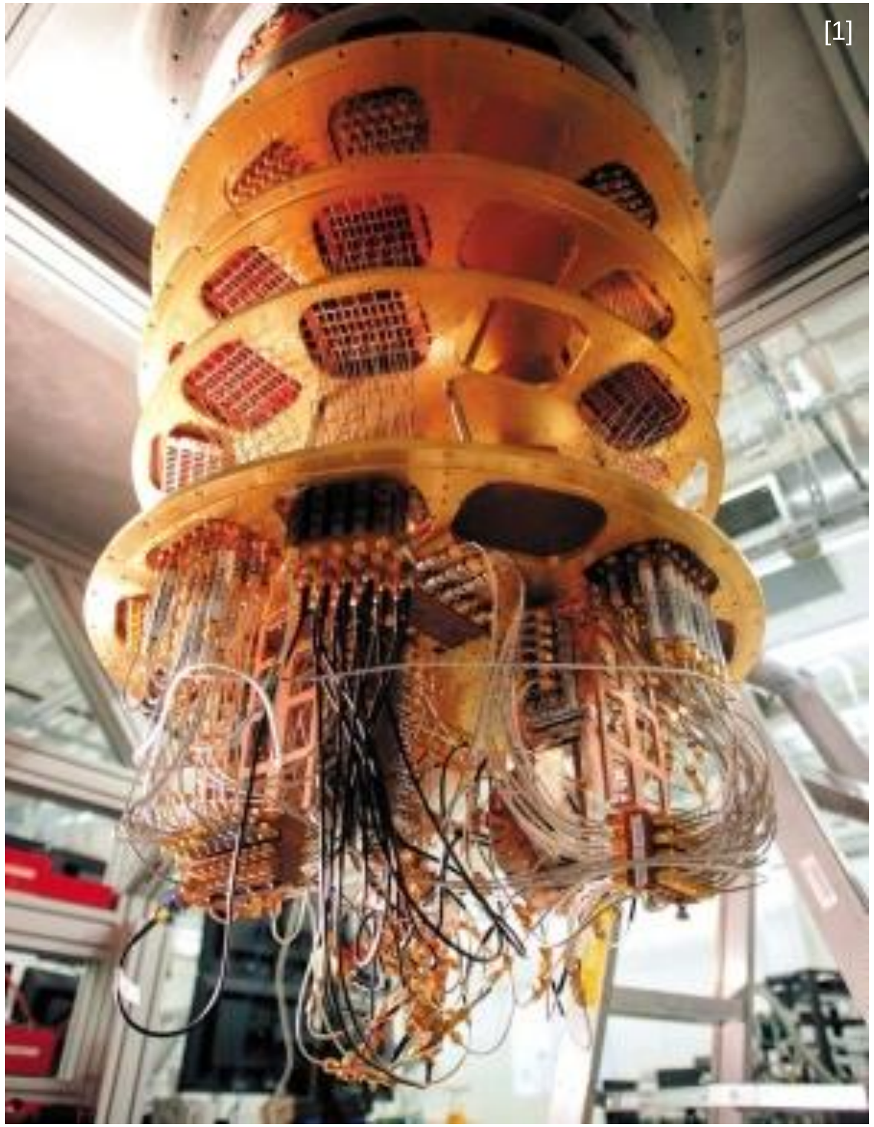
MOTIVATION

Brief summary

- Quantum computing will speed up solution finding in drug design, cryptography, optimization.
- Universal quantum computers needs 10^6 to 10^9 physical qubit, due to non-idealities [1].
- Current RT approaches are not fully scalable [2],[3].

Local cryo-electronics with system integration view is needed!

Regulated and stable supply voltage in situ is required for optimum operation.


[1]

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[1] Mohseni, Masoud, et al. "Commercialize quantum technologies in five years." *Nature* 543.7644 (2017): 171-174.
[2] Charbon, Edoardo, et al. "Cryogenic CMOS circuits and systems: Challenges and opportunities in designing the electronic interface for quantum processors." *IEEE Microwave Magazine* 22.1 (2020): 60-78.
[3] Degenhardt, C., et al. "Systems engineering of cryogenic CMOS electronics for scalable quantum computers." *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019.

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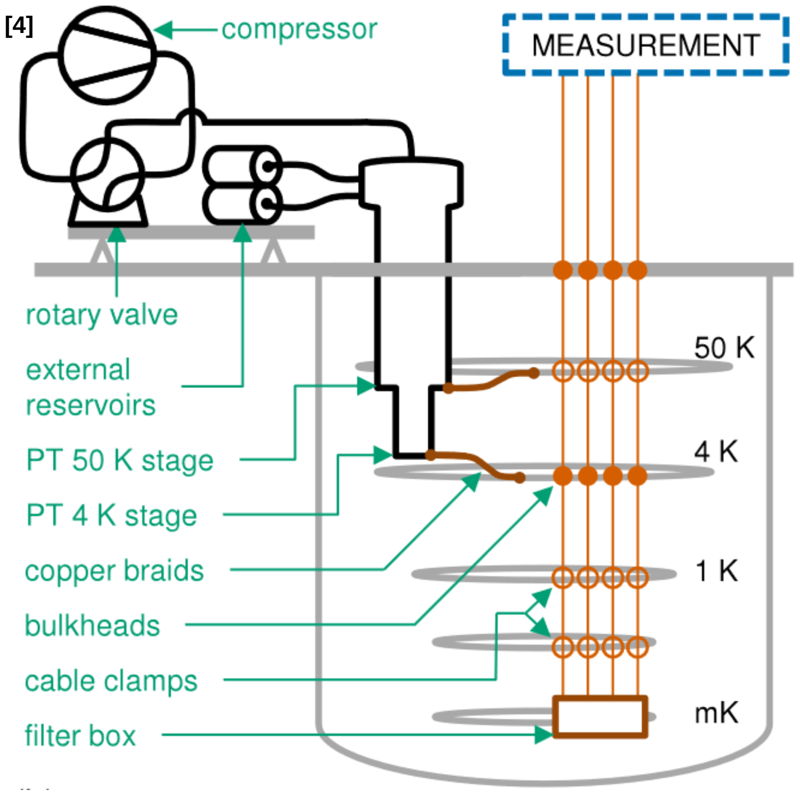
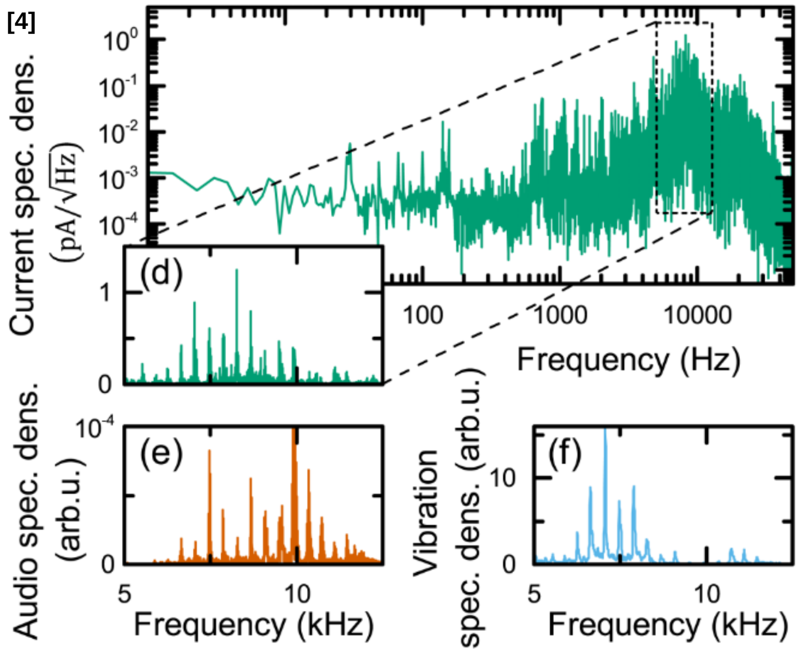
POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Vibration-induced electrical noise



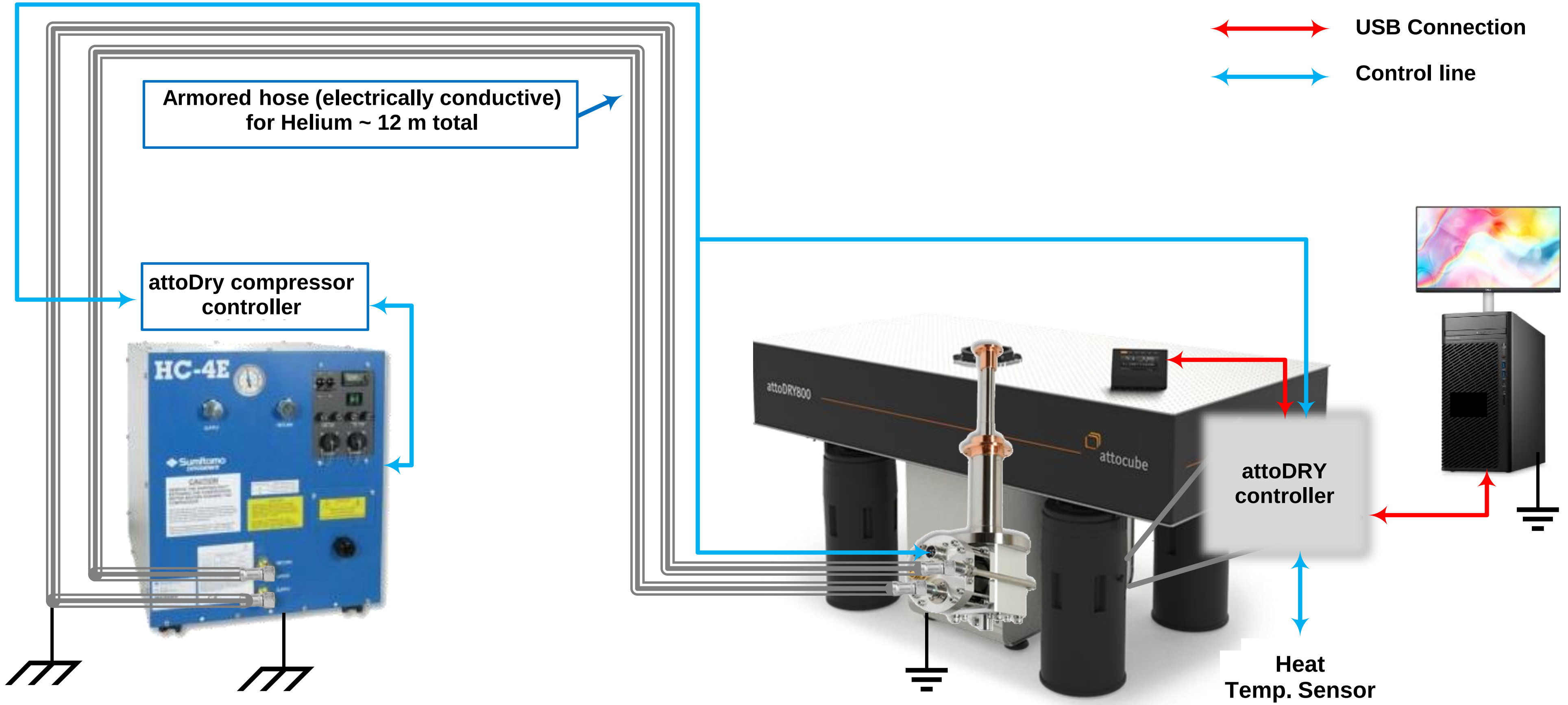


Cryocooler (e. g. pulse tube) in dilution fridge produces vibrations [4],[5].

[4] Kalra, Rachpon, et al. "Vibration-induced electrical noise in a cryogen-free dilution refrigerator: Characterization, mitigation, and impact on qubit coherence." *Review of Scientific Instruments* 87.7 (2016).
[5] Lake Shore Cryoelectronics, "Pulse tube cryocoolers vs Gifford-McMahon cryocoolers," https://www.lakeshore.com/products/product-detail/janis/pulse-tube-cryocoolers-vs.-gifford-mcmahon-cryocoolers.

POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Ground loop in Gifford-McMahon cryocooler (attoDRY800)



Armored hose (electrically conductive) for Helium ~ 12 m total

attoDry compressor controller

attoDRY controller

Heat Temp. Sensor

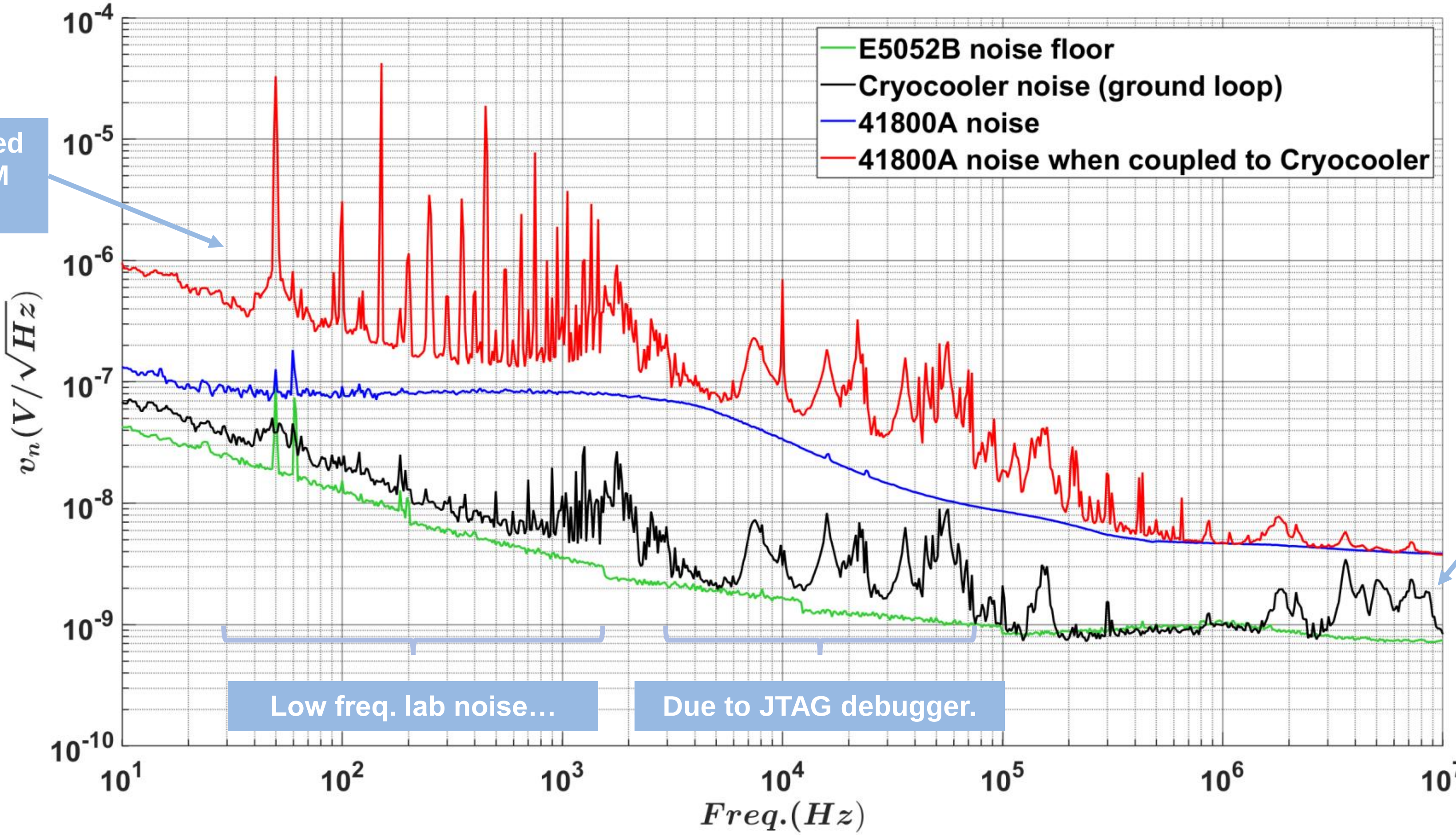
⟷ USB Connection

⟷ Control line

[6] Ott, Henry W. *Electromagnetic compatibility engineering*. John Wiley & Sons, 2011.
[7] Sumitomo Heavy Industries, Ltd., https://www.shicryogenics.com/
[8] attocube systems AG, https://www.attocube.com/en

POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Ground loop impact on active probe (41800A) as example



Active probe connected to passive load in GM cryocooler at 6K

Passive load coupled to GM cryocooler at 6K.

Low freq. lab noise…

Due to JTAG debugger.

POWER INTEGRITY CHALLENGES FOR CRYOGENIC ICS

Power distribution for cryogenic ICs

- Complex ICs for Quantum Computing need local power distribution networks due to:

- **Limited connections between Cryo. stage and RT.**
- **Different power domains needed; Analog, Digital, Mixed Signal.**
- **No commercial DC-DC converters for Cryo. ($4K \leq$ Temp. $\leq 7K$) [9], [10]**

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[9] Homulle, Harald, et al. "Design techniques for a stable operation of cryogenic field-programmable gate arrays." *Review of Scientific Instruments* 89.1 (2018): 014703.
[10] H. Homulle and E. Charbon, “Cryogenic low-dropout voltage regulators for stable low-temperature electronics,” Cryogenics, vol. 95, 2018.

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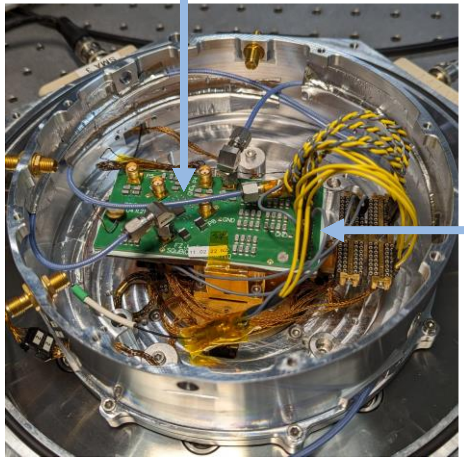
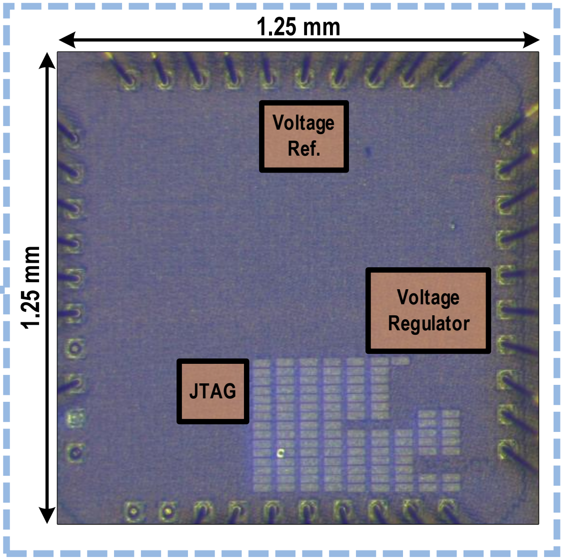
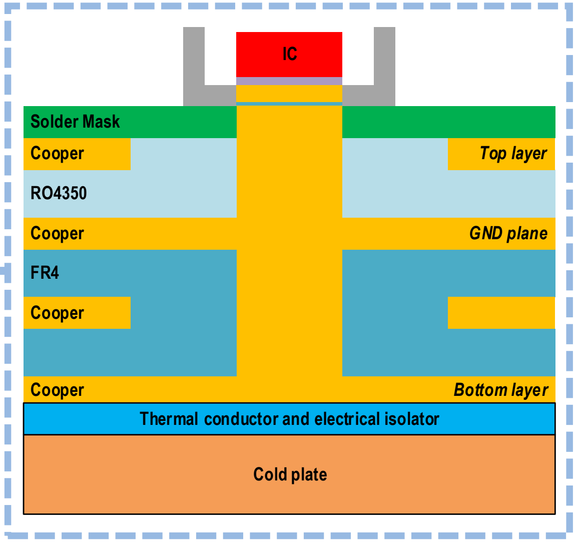
CRYOGENIC VOLTAGE REGULATION

Prototype

- IC (22 nm FDSOI): Voltage Ref., Voltage Reg. and JTAG interface[11].
- PCB for good cryocooler – IC thermal coupling.
- Thermal pad to brake ground loop.
- Test temps.: [300 K, 6 K].







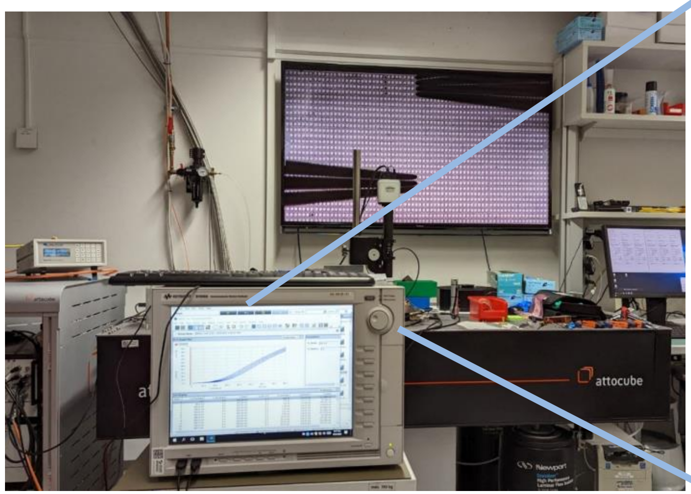
[11] A. R. Cabrera-Galicia *et al.*, " A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology," to be published in *2023 IEEE 19th Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2023.

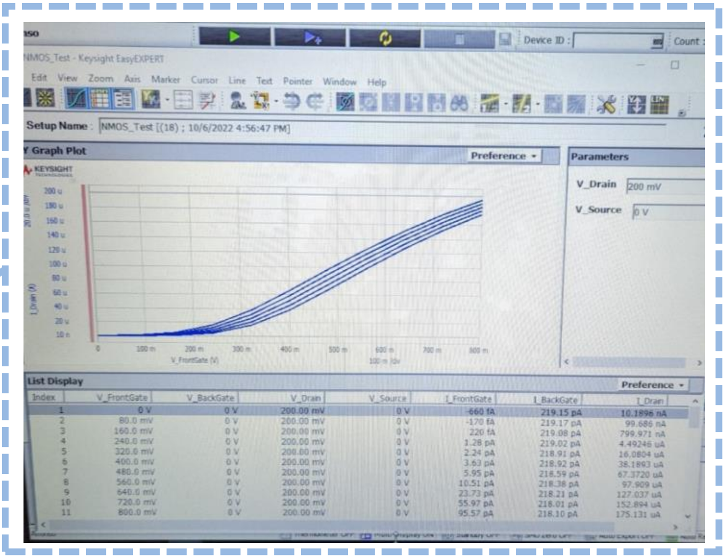
CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Cryogenic electrical characterization of 22 nm FDSOI

- **Setup:**
  - Gifford-McMahon cryocooler (attoDRY800); 7K
    with needle probing station.
  - Semiconductor device analyzer (B1500A).

- **Objective:**
  to develop a cryogenic simulation model for 22 nm FDSOI;
  QSolid collaborative project [12]



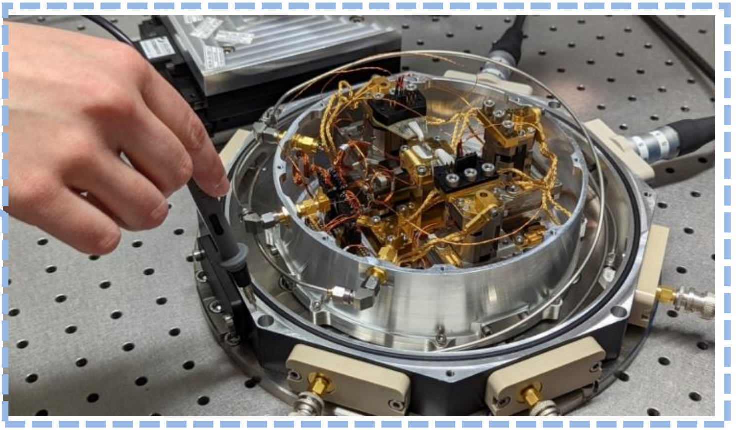


Setup Name : NMOS_Test [(18) ; 10/6/2022 4:56:47 PM]

V_Drain 200 mV

V_Source 0 V

Index	V_FrontGate	V_BackGate	V_Drain	V_Source	I_FrontGate	I_BackGate	I_Drain
1	0 V	0 V	200.00 mV	0 V	-660 fA	219.15 pA	10.1896 nA
2	80.0 mV	0 V	200.00 mV	0 V	-170 fA	219.17 pA	99.686 nA
3	160.0 mV	0 V	200.00 mV	0 V	220 fA	219.08 pA	799.971 nA
4	240.0 mV	0 V	200.00 mV	0 V	1.28 pA	219.02 pA	4.49246 uA
5	320.0 mV	0 V	200.00 mV	0 V	2.24 pA	218.91 pA	16.0804 uA
6	400.0 mV	0 V	200.00 mV	0 V	3.63 pA	218.92 pA	38.1893 uA
7	480.0 mV	0 V	200.00 mV	0 V	5.95 pA	218.59 pA	67.3720 uA
8	560.0 mV	0 V	200.00 mV	0 V	10.51 pA	218.38 pA	97.909 uA
9	640.0 mV	0 V	200.00 mV	0 V	23.73 pA	218.21 pA	127.037 uA
10	720.0 mV	0 V	200.00 mV	0 V	55.97 pA	218.01 pA	152.894 uA
11	800.0 mV	0 V	200.00 mV	0 V	95.57 pA	218.10 pA	175.131 uA



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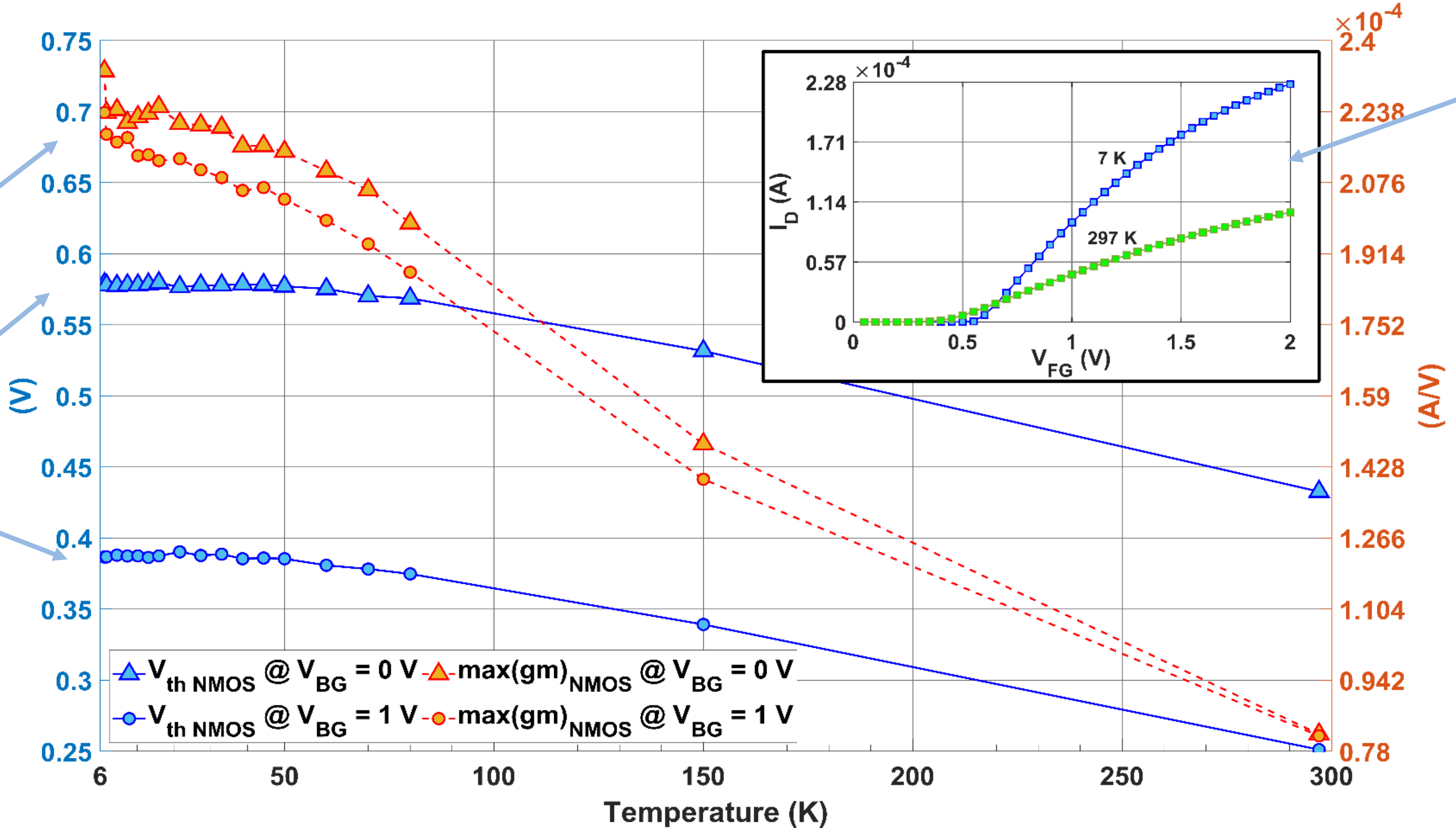
[12] The QSolid consortium, “QSolid, Quantum Computer in the Solid State,” https://www.q-solid.de/

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Cryogenic electrical characterization of 22 nm FDSOI



Transconductance increase with temps reduction.

Vth saturation at temps. lower than 60K

Vth tuning via backgate

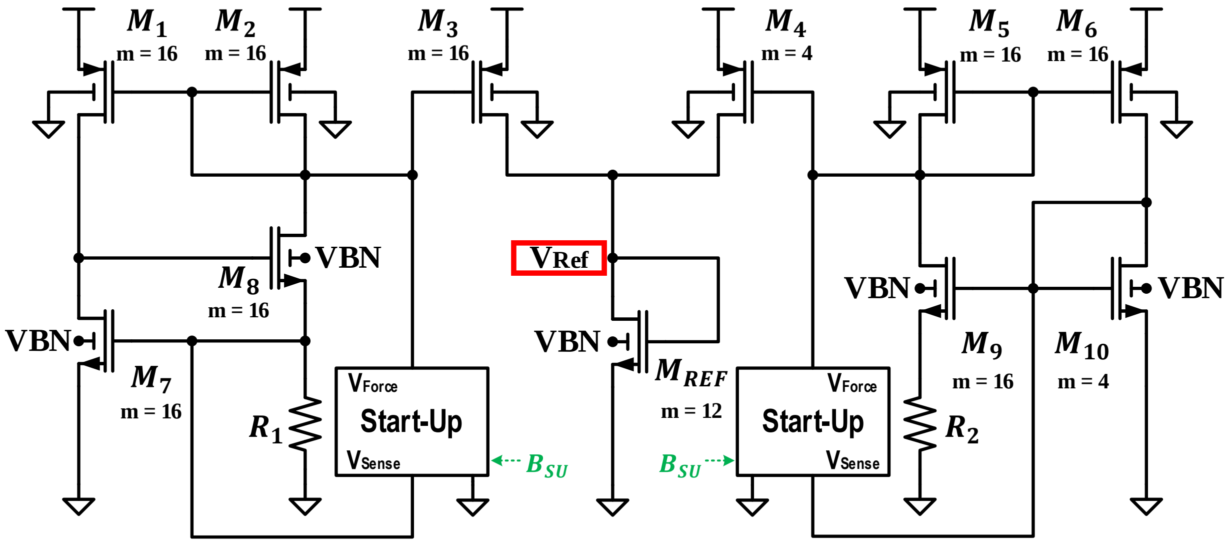
Common electrical behavior at cryo

[13] A. R. Cabrera-Galicia *et al.*, "Towards the Development of Cryogenic Integrated Power Management Units," *2022 IEEE 15th Workshop on Low Temperature Electronics (WOLTE)*.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage reference

- Cryogenic V_{th} saturation as working principle.
- The circuit saturates M_{REF} while in V_{th} saturation temperature region.
- Simple and without post-fabrication correction.



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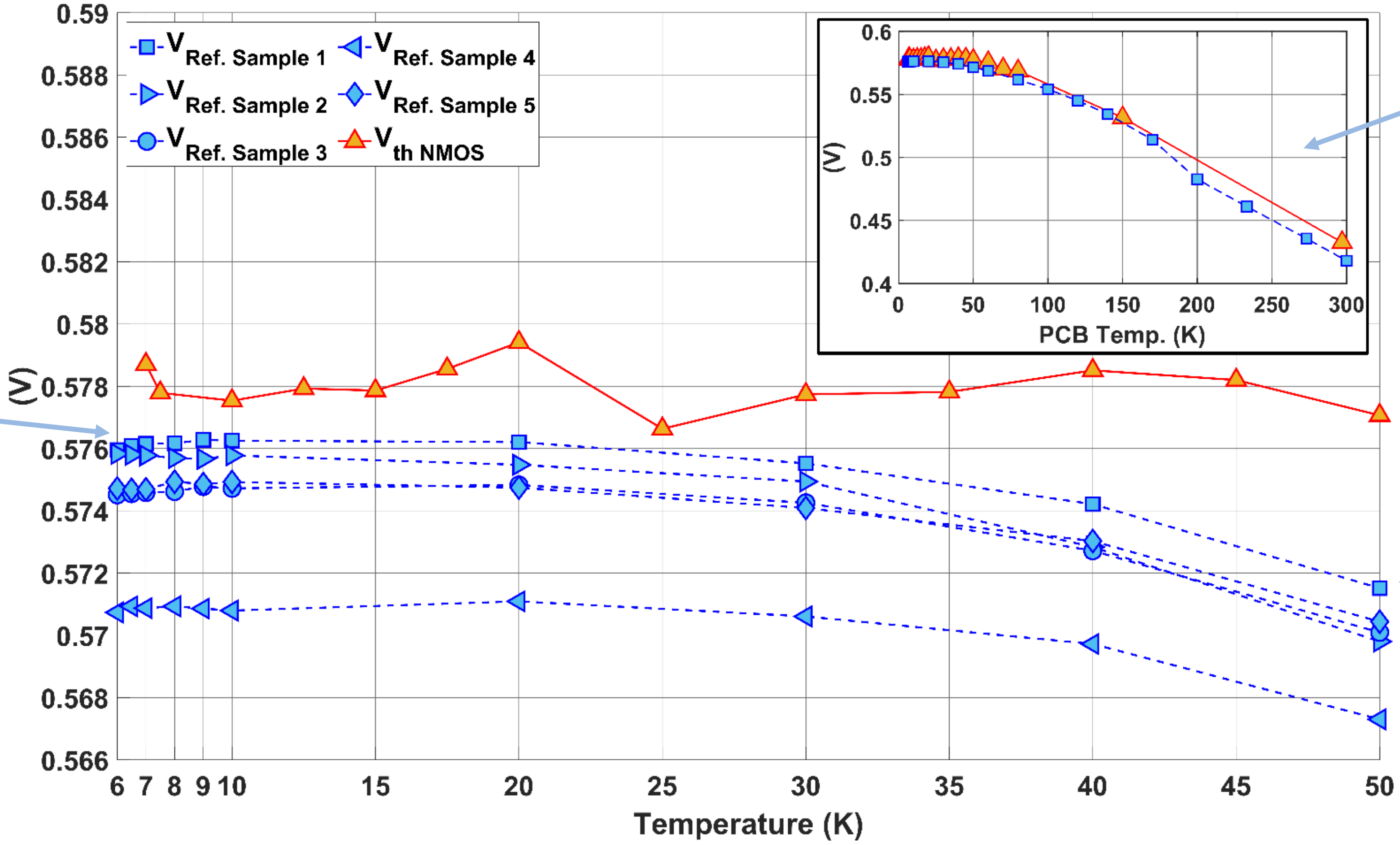
CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage reference cryogenic test



TC = 300 ppm/K
@ Temp = [6 K, 50 K]

$V_{Ref.\ Sample\ 1}$ is compared with V_{th} from I/O NMOS.

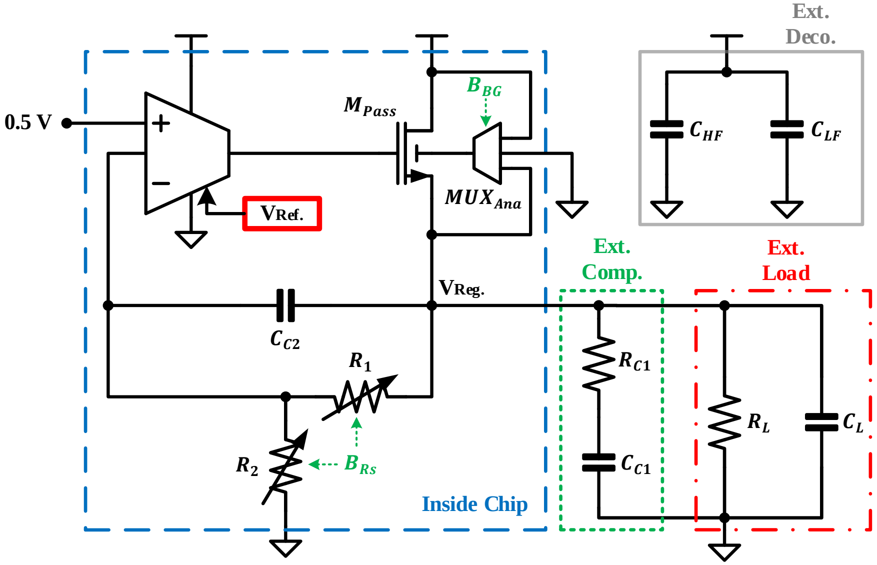
5 sample chips are tested.

[11] A. R. Cabrera-Galicia *et al.*, " A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology," to be published in *2023 IEEE 19th Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2023.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator

- NMOS pass element (M_{Pass}); better PSRR than PMOS [14].
- M_{Pass} V_{th} reduction via backgate for low $V_{Sup.}$ requirement.
- $V_{Reg.}$ tuning via feedback modification with JTAG.
- Cryogenic-stable RC compensation network [10].



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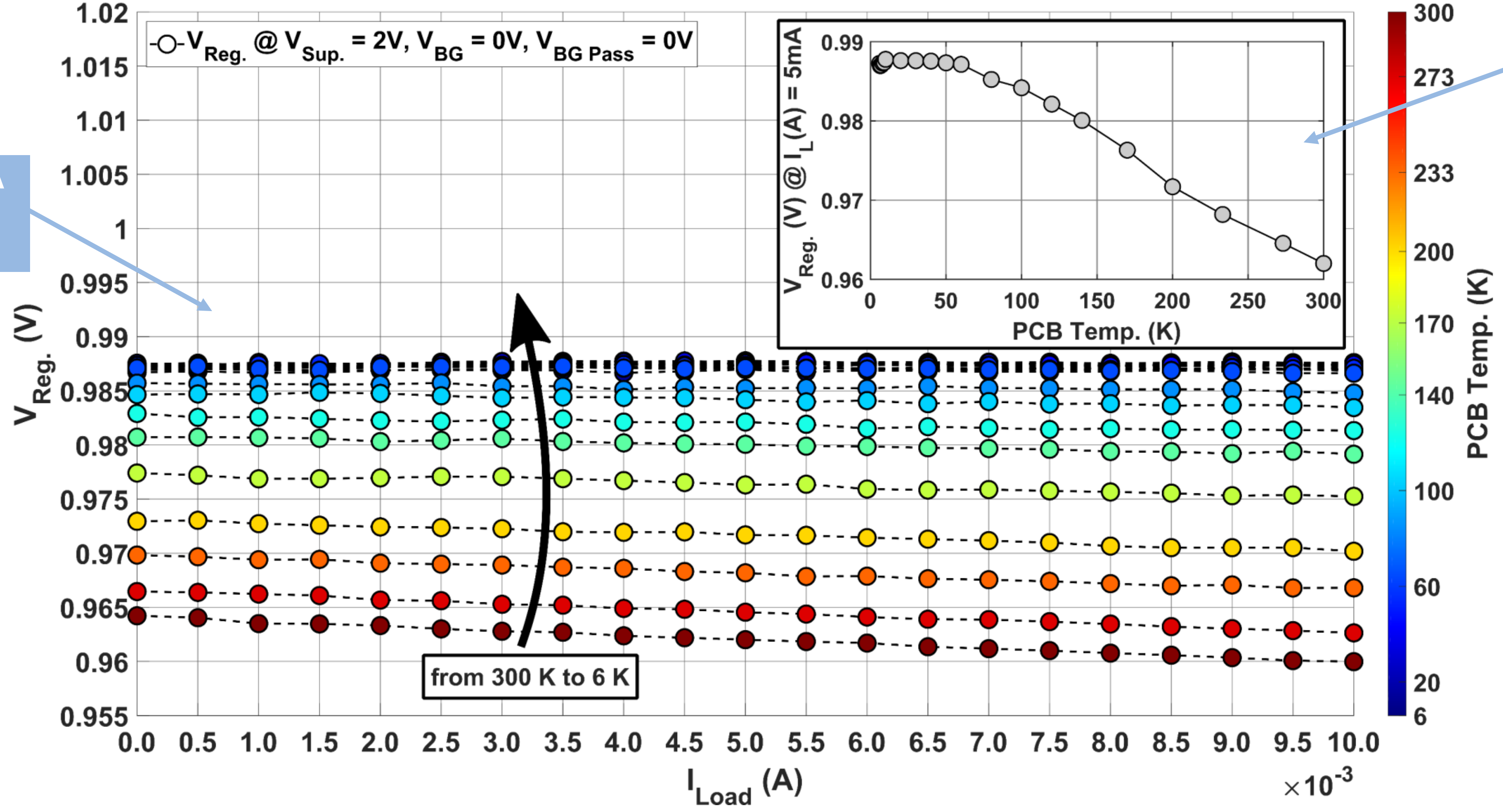
[10] H. Homulle and E. Charbon, “Cryogenic low-dropout voltage regulators for stable low-temperature electronics,” Cryogenics, vol. 95, 2018.
[14] B. Razavi, “The low dropout regulator [a circuit for all seasons],” IEEE Solid-State Circuits Magazine, vol. 11, no. 2, 2019.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator cryogenic test; load regulation



Load Reg. = 22 mV/A @ Temp = 6 K and I_{Load} = [0 A, 10 mA]

$V_{Reg.}$ @ I_{Load} = 5 mA.

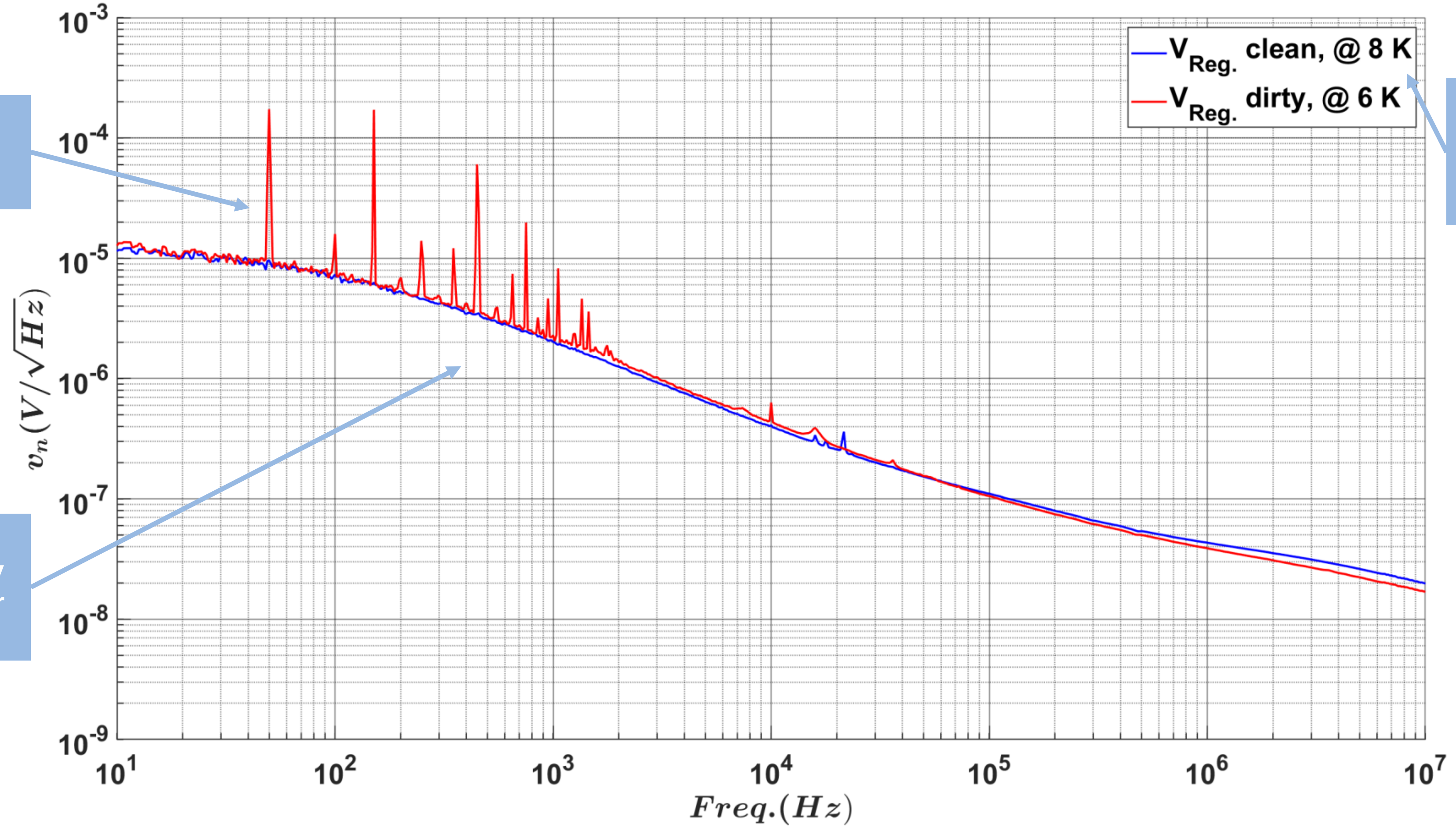
[11] A. R. Cabrera-Galicia *et al.*, " A Cryogenic Voltage Regulator with Integrated Voltage Reference in 22 nm FDSOI Technology," to be published in *2023 IEEE 19th Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2023.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

Voltage regulator cryogenic test; noise spectral density

Ground loop noise is coupled to regulator output via cold plate.

Higher temp. due to thermal pad and imperfect thermalization of cables; improvement on progress.

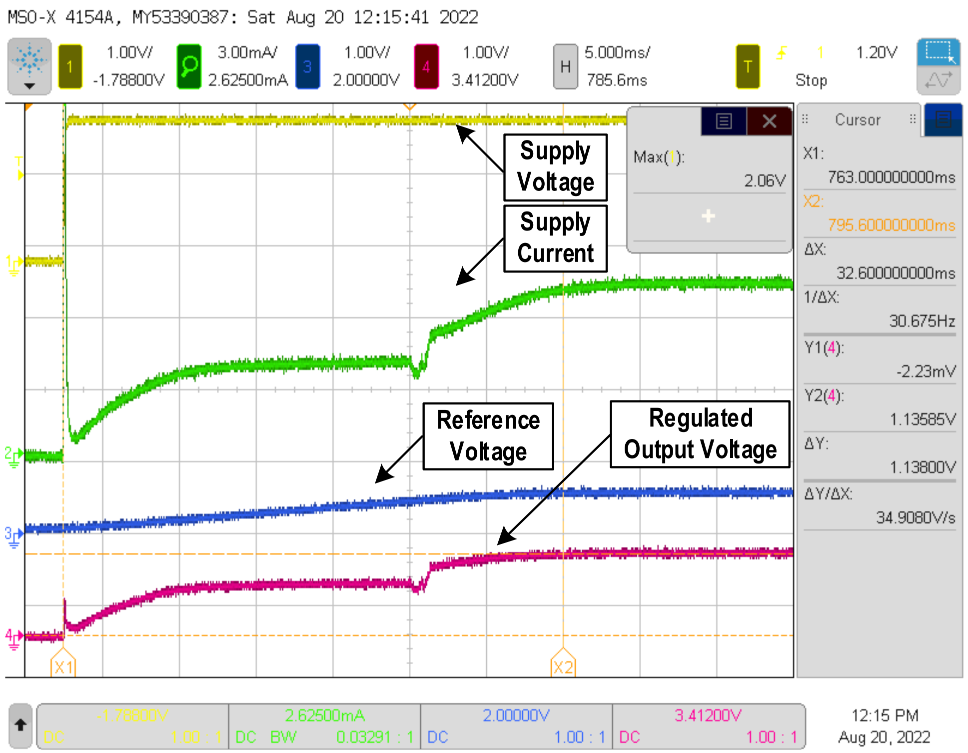


Ground loop noise is removed by electrically detaching the regulator from the cold plate.

CRYOGENIC IC DESIGN FOR VOLTAGE REGULATION

$V_{Ref.} + V_{Reg.}$ cryogenic test

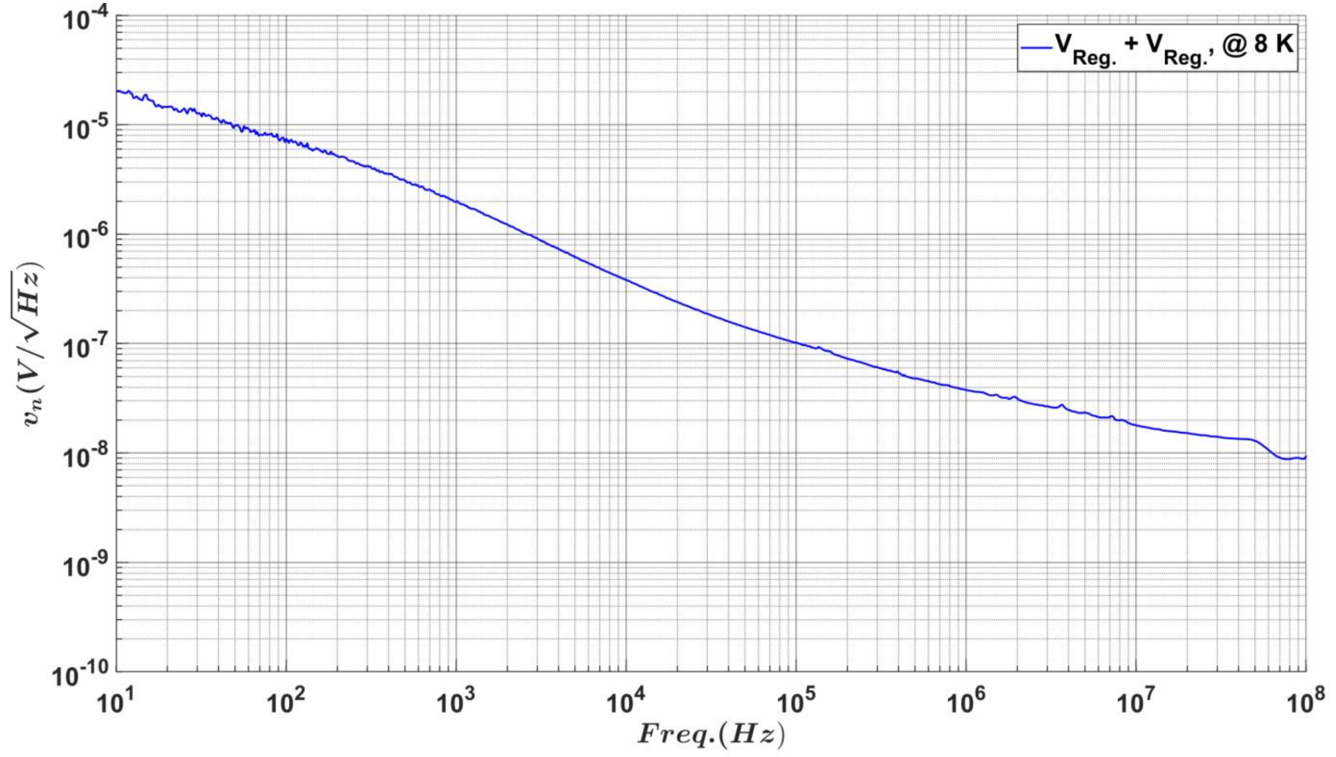
Transient response and spectral noise density measured at cryo.



MSO-X 4154A, MY53390387: Sat Aug 20 12:15:41 2022

Max(1): 2.06V

X1: 763.000000000ms
X2: 795.600000000ms
ΔX: 32.600000000ms
1/ΔX: 30.675Hz
Y1(4): -2.23mV
Y2(4): 1.13585V
ΔY: 1.13800V
ΔY/ΔX: 34.9080V/s



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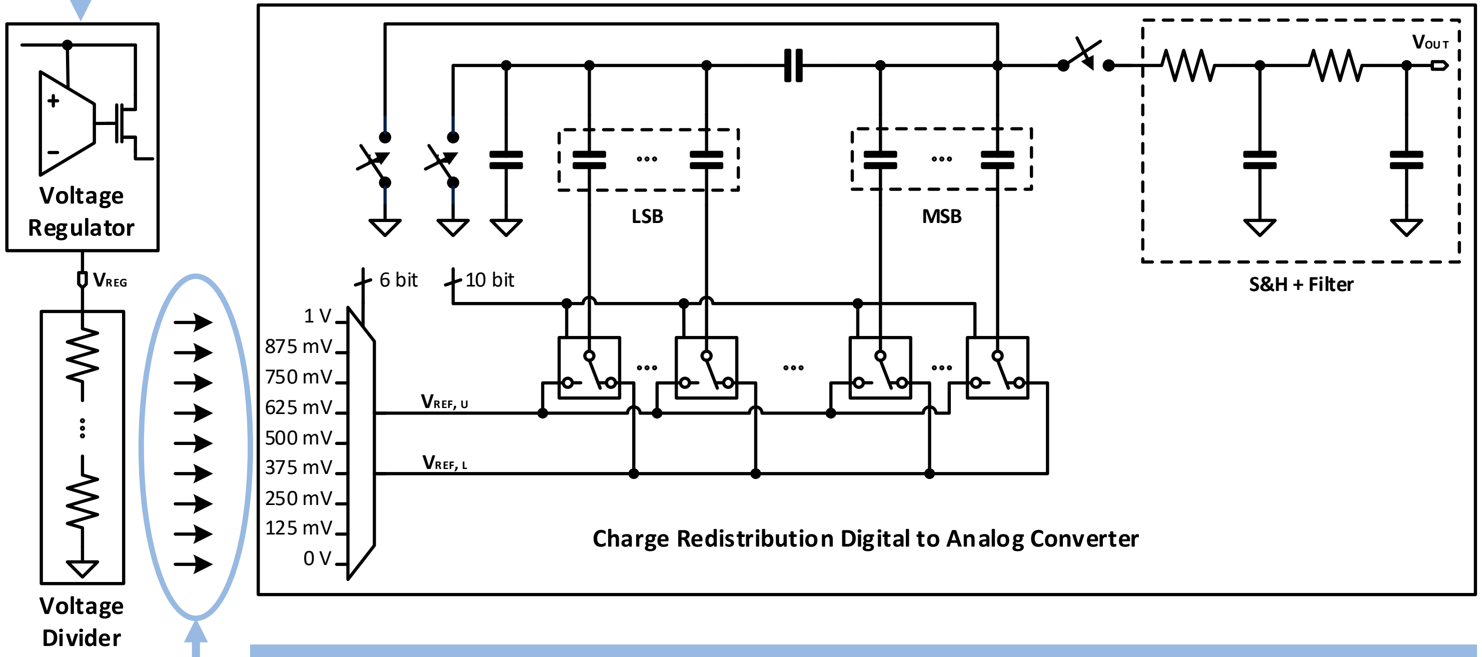
APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{Reg.}$ + DAC at cryogenic temperatures

- **Objective:**
  to showcase the operation of multiple ICs on Cryo.

- DAC (65 nm CMOS) [12]
  $V_{Reg.}$ (22 nm FDSOI).

Energized with one supply.



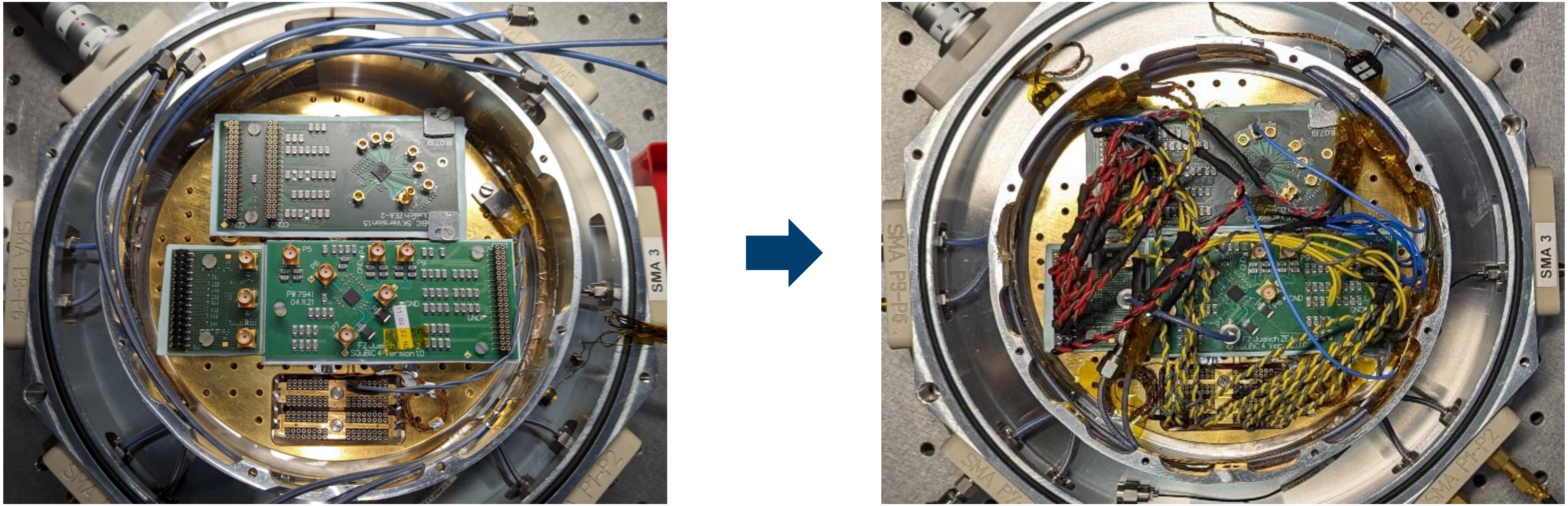
Previously, the DAC voltage references were provided from RT electronics; 8 connections.

[15] Vliex, Patrick, et al. "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications." *IEEE solid-state circuits letters* 3 (2020): 218-221.

APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{Reg.}$ + DAC at cryogenic temperatures

First trial: quick and dirty!



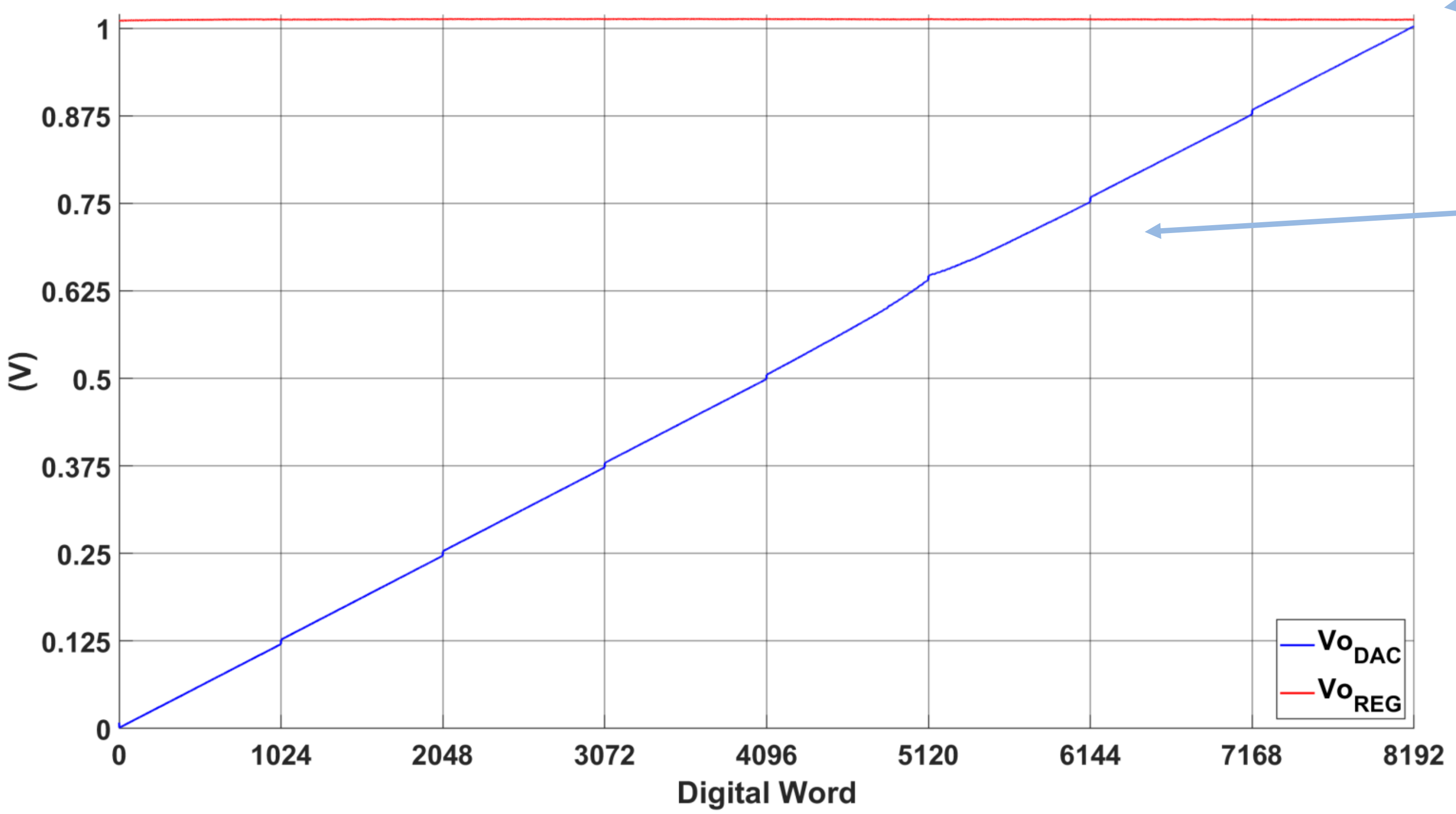
APPLICATION CASE: VOLTAGE REFERENCES FOR DAC

$V_{Reg.}$ + DAC at cryogenic temperatures

PCB temp. is 11 K; optimization on cryocooler cabling is needed.

Dedicated PCB for both ICs will improve the area and connections.

Work on progress; first results.

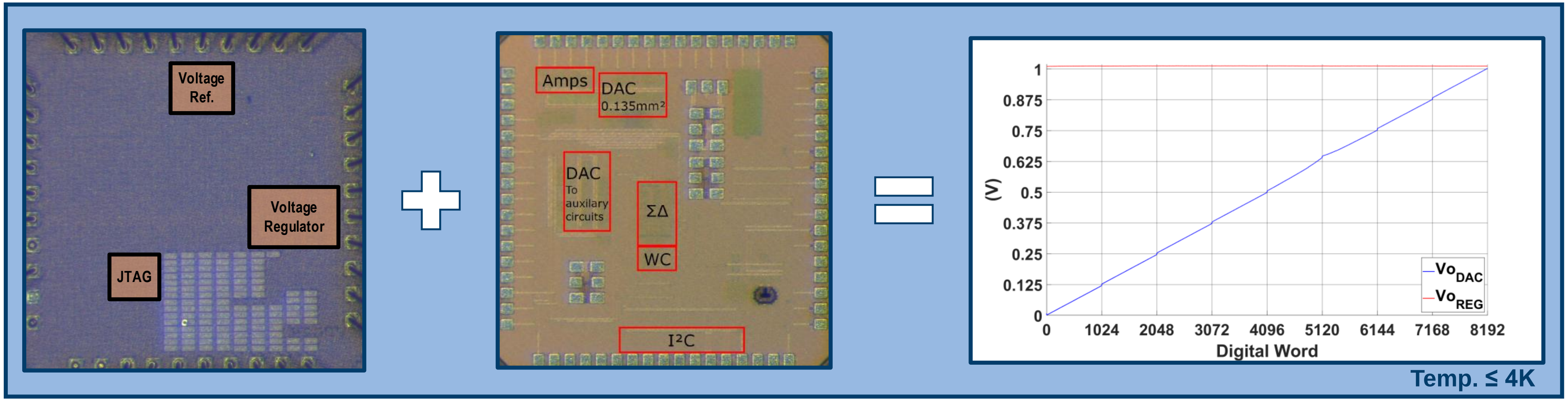


$V_{Reg.}$ set close to 1 V via JTAG.

DAC operates with the reference voltages generated on cryo.

CONCLUSIONS

- Cryogenic ICs need local power distribution network.
- Dilution refrigerators challenges: vibration induced noise, ground loops, limited connections.
- ICs and physical setups are the solution to the challenges.



THANKS FOR YOUR ATTENTION

ZEA-2


**André
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**Stefan
van Waasen**


**Arun
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**Andre
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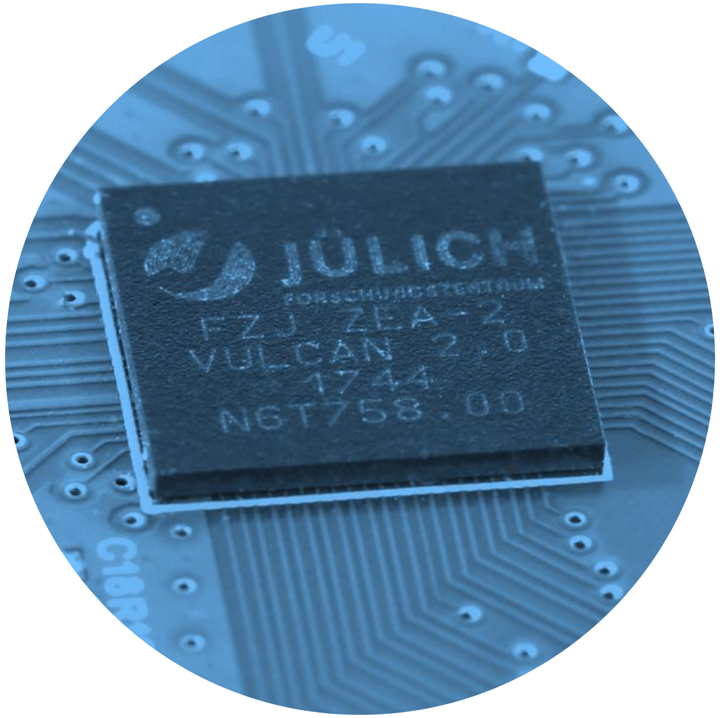
**Patrick
Vliex**


**Alfonso Rafael
Cabrera Galicia**


**Lea
Schreckenberg**


**Phanish
Chava**


**Swasthik
B. S. Bhat**



IC Development Team

REFERENCES

- [1] Mohseni, Masoud, et al. "Commercialize quantum technologies in five years." *Nature* 543.7644 (2017): 171-174.
- [2] Charbon, Edoardo, et al. "Cryogenic CMOS circuits and systems: Challenges and opportunities in designing the electronic interface for quantum processors." *IEEE Microwave Magazine* 22.1 (2020): 60-78.
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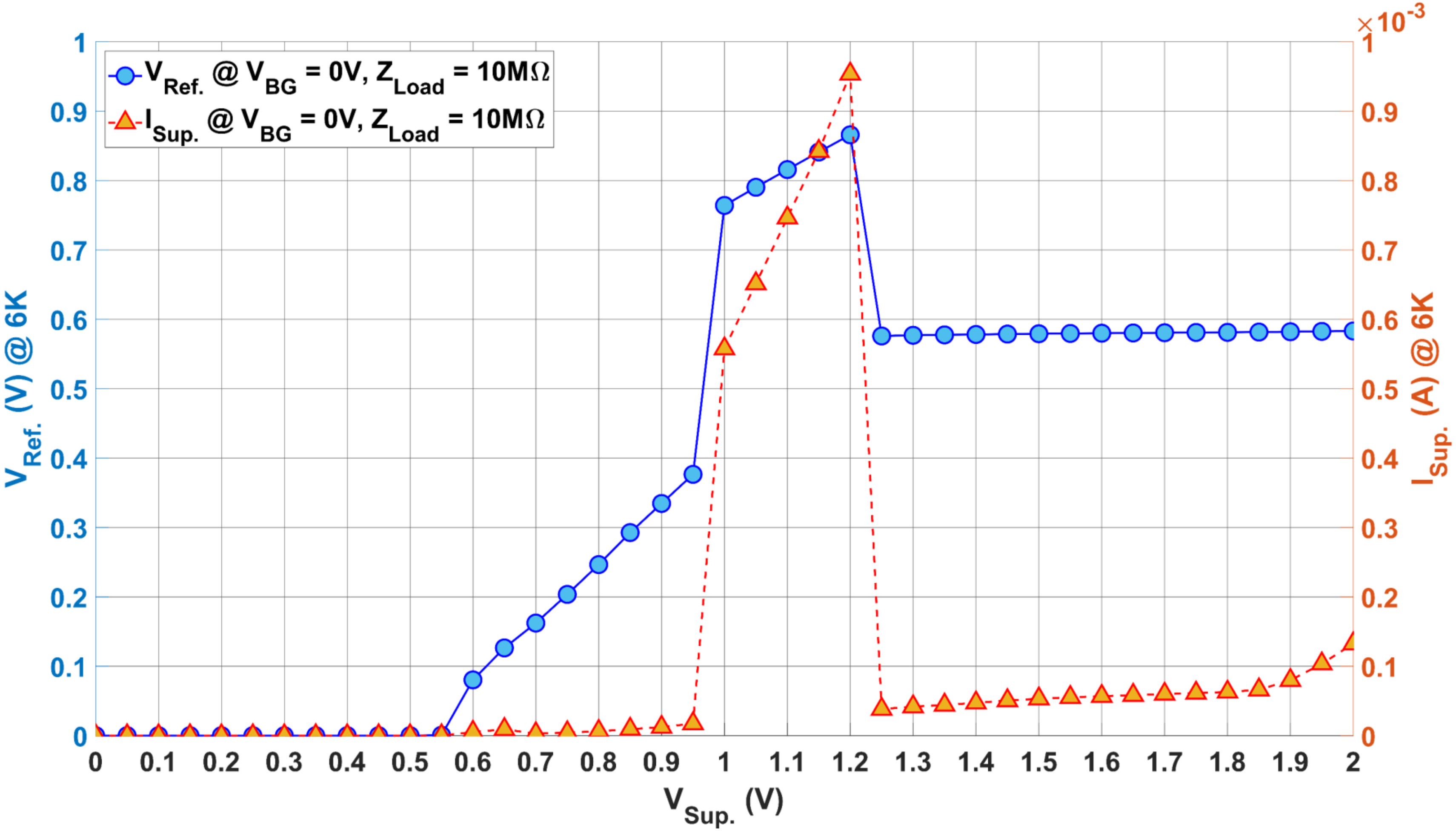
- [15] Vliex, Patrick, et al. "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications." *IEEE solid-state circuits letters* 3 (2020): 218-221.

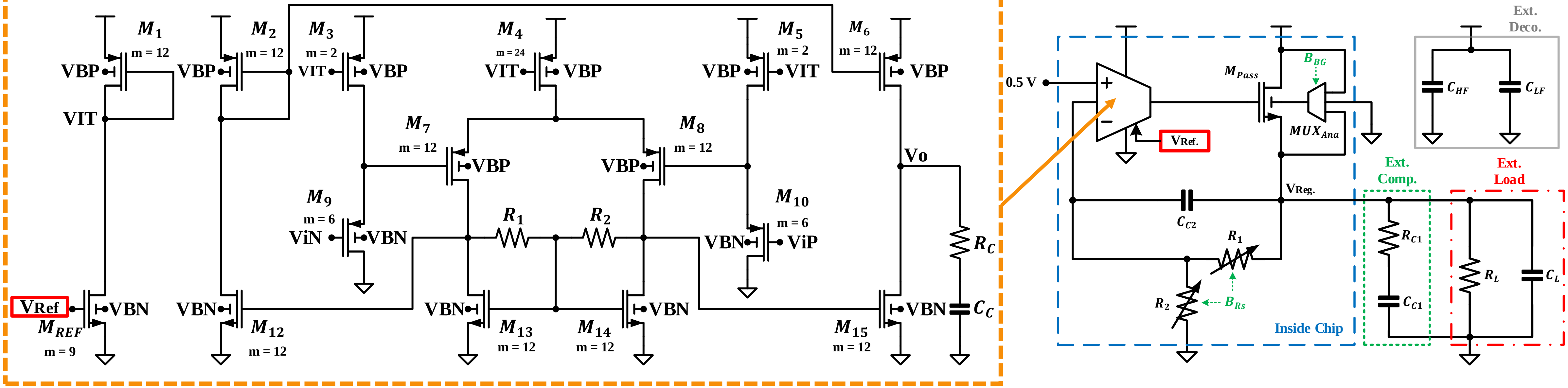
BACKUP

$V_{Ref.}$ with respect to $V_{Sup.}$ at 6K



BACKUP

Differential amplifier used by regulator



$$A_{\mathrm{DA}} \approx g_{m_{7,8}} \cdot (R_{1,2} || r_{o_{7,8}} || r_{o_{13,14}}) \cdot g_{m_{12,15}} \cdot Z_{\mathrm{out}} \quad (1)$$

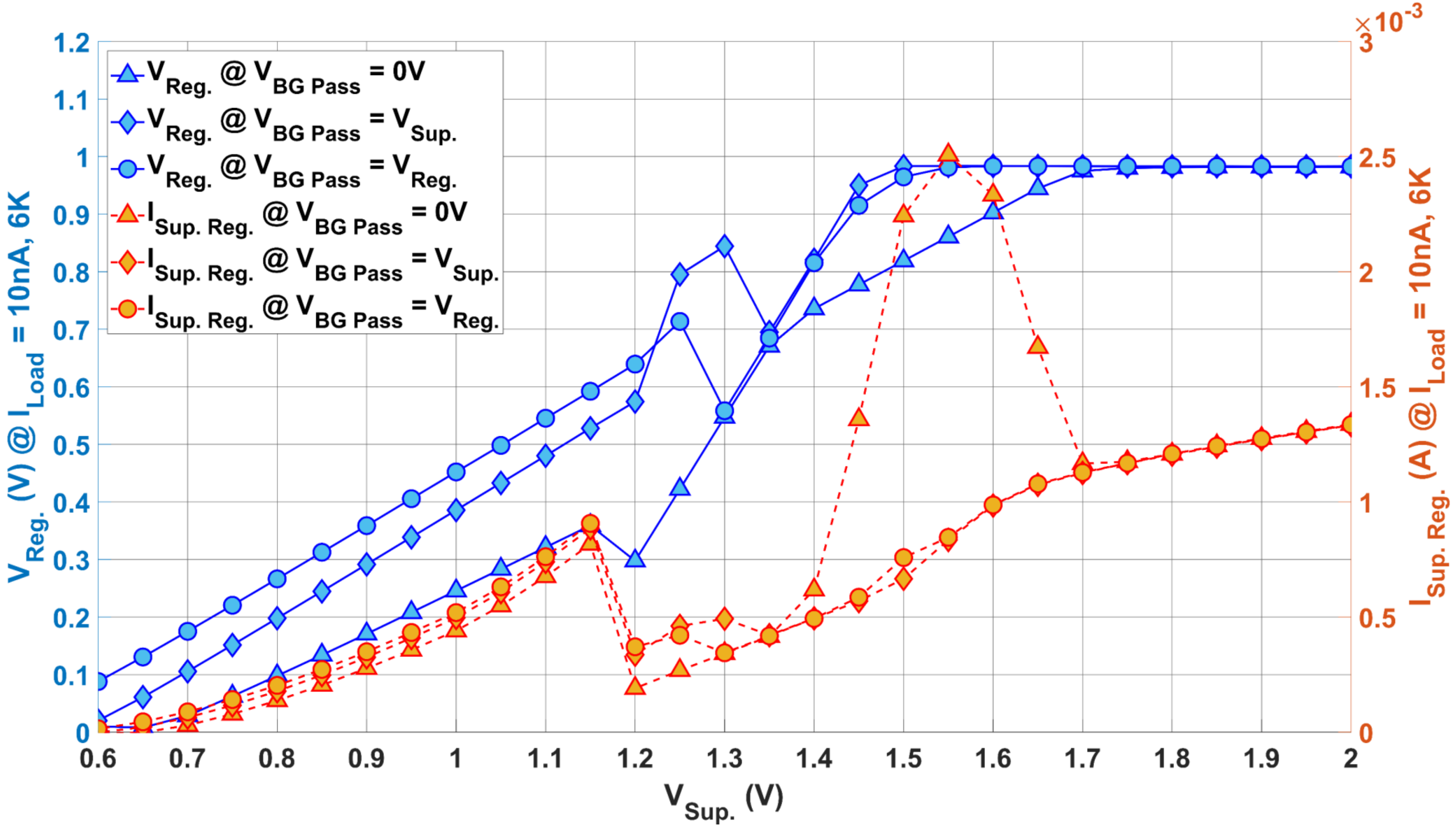
$$A_{\mathrm{LG}} \approx A_{\mathrm{DA}} \cdot \frac{R_{\mathrm{F2}}}{R_{\mathrm{F1}} + R_{\mathrm{F2}}} \quad (2)$$

$$\mathrm{LR} \approx \frac{1}{g_{m_{\mathrm{M\,Pass}}} \cdot A_{\mathrm{LG}}} \quad (3)$$

$$\mathrm{PSRR} \approx \frac{1}{g_{m_{\mathrm{M\,Pass}}} \cdot r_{o_{\mathrm{M\,Pass}}} \cdot A_{\mathrm{LG}}} \quad (4)$$

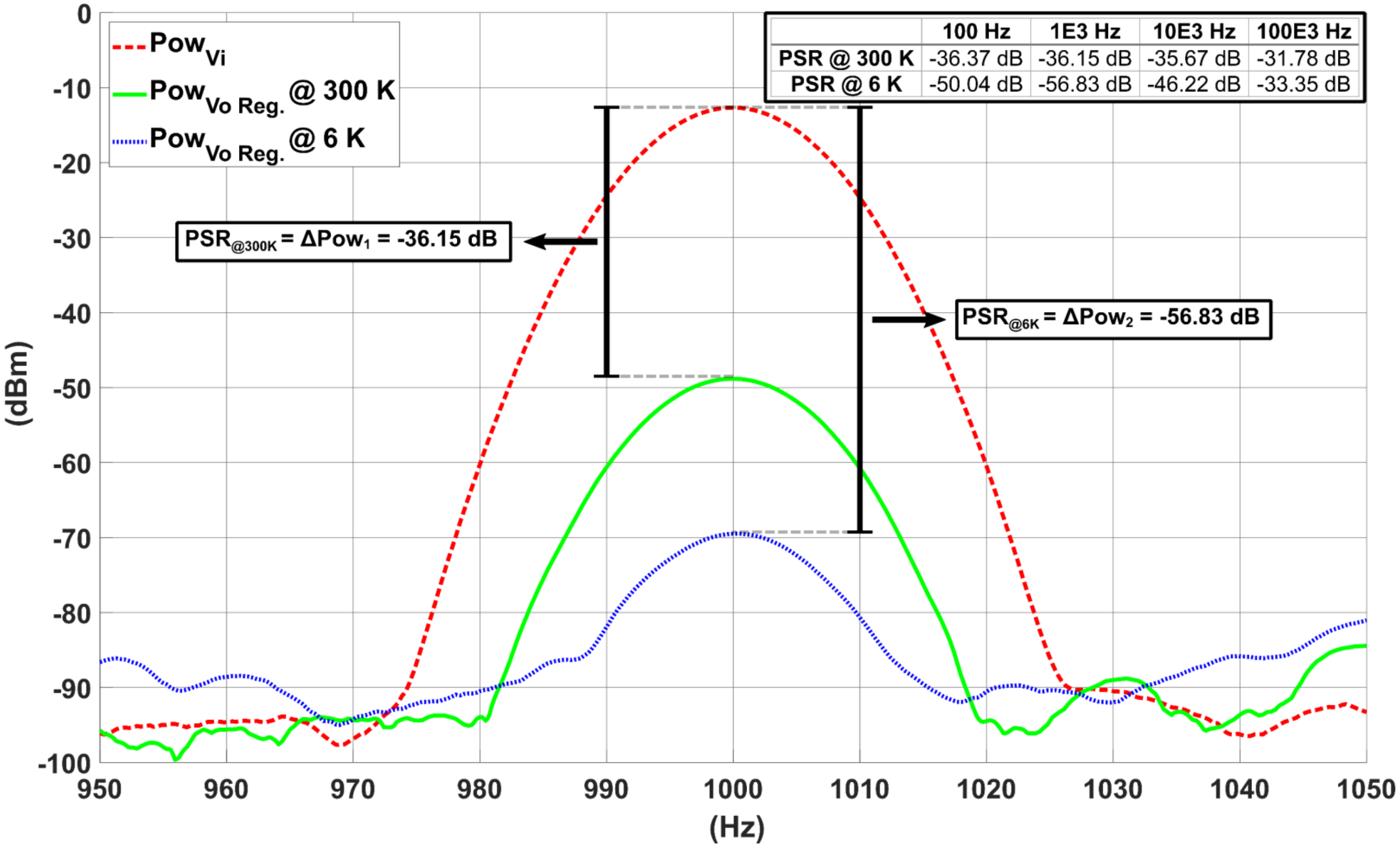
BACKUP

$V_{Reg.}$ with respect to $V_{Sup.}$ at 6K



BACKUP

$V_{Reg.}$ PSRR at $V_{Sup.}$= 2V and Temp. = 6K



	100 Hz	1E3 Hz	10E3 Hz	100E3 Hz
PSR @ 300 K	-36.37 dB	-36.15 dB	-35.67 dB	-31.78 dB
PSR @ 6 K	-50.04 dB	-56.83 dB	-46.22 dB	-33.35 dB