POLITECNICO MILANO 1863

DIPARTIMENTO DI ELETTRONICA INFORMAZIONE E BIOINGEGNERIA

Fully-integrated Cryo-CMOS spin-to-digital readout for spin qubits

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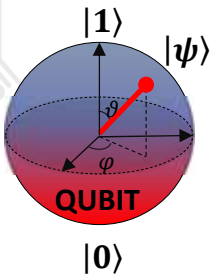
What is quantum computing?



- Novel form of computing which harnesses quantum mechanical effects such as **superposition** and **entanglement.**
- Two distinct states of the particle to store and manipulate data, called **qubit.**

Superconducting loops | **Trapped ions** | **Silicon quantum dots** | **Topological qubits** | **Diamond vacancies**

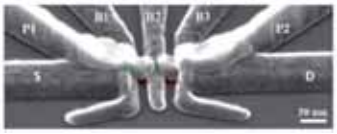
Scaling problem – we're back to silicon

Demonstrating key ingredients on different hardware approaches.

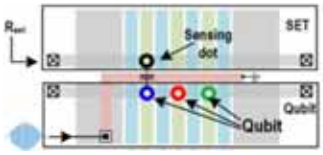
Small prototypes containing tens of qubits.

Large scale error corrected quantum computers.

➡ **Scaling** challenge



[N. LAI et al., *Scientific reports* (2011)]

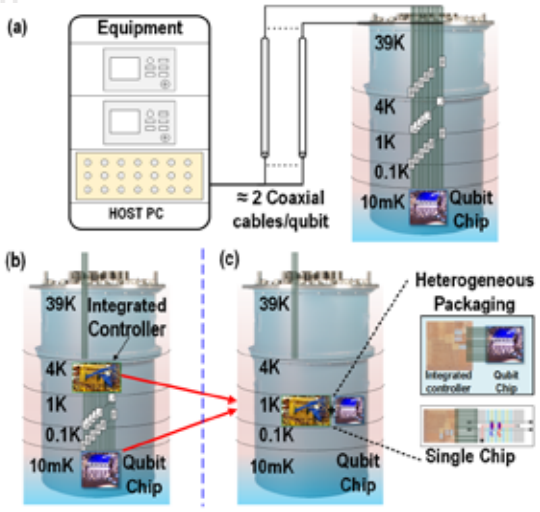


[J. PARK et al., Journal of *Solid-state circuits* (2021)]

Silicon spin qubits seem promising:

- Leverage knowledge and production capabilities of semiconductor foundries by using transistor-like structure to build qubits.
- Good physical properties of silicon for a $T_2^* \approx 100\ \mu s$

Need of the cryogenic electronics



[J. PARK et al., Journal of *Solid-state circuits* (2021)]

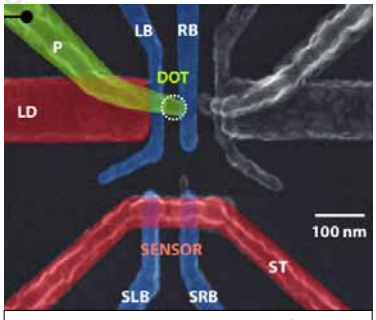
- Long cable
- Complex wiring
- Heat dissipation

- short cable
- simple wiring
- Low heat dissipation

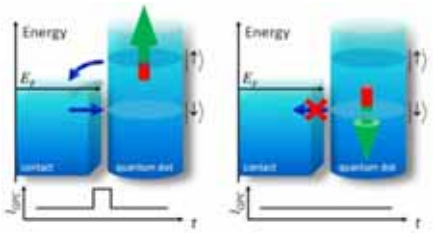
- Cryo-CMOS electronics
- Limited cooling power

Spin-qubit readout: spin-to-charge conversion

Spin qubits in semiconductor quantum dots are formed when an electron is electrostatically confined.



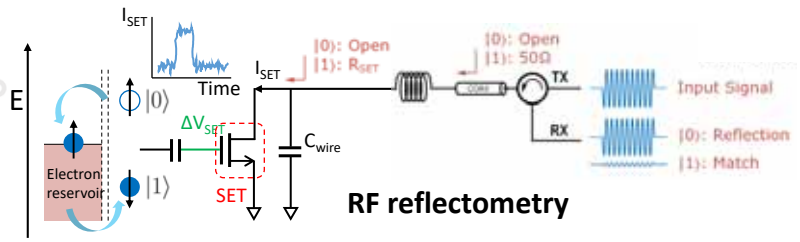
[H. Yang et al., *Physical review B*, (2012)]



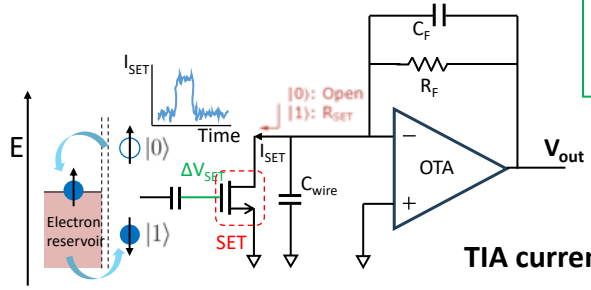
Spin-to-charge conversion readout:

- A spin-selective tunnelling processes changes the electrostatic potential
- The SET gate reacts to this variation by changing its channel conductance.

Spin qubit readout: measurement technique



RF reflectometry

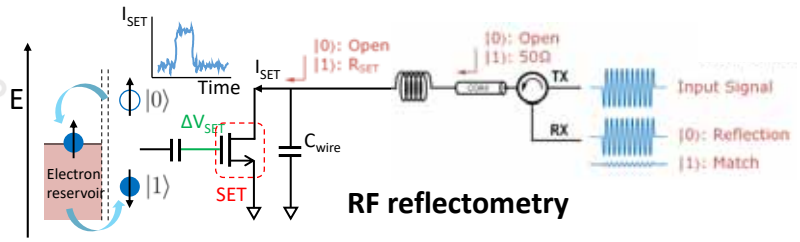


$$BW \cong GBWP\frac{C_F}{C_{wire}}$$

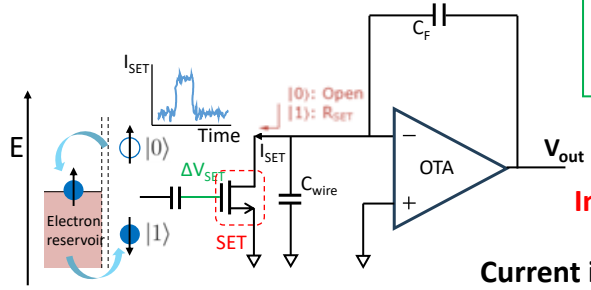
$$S_I(f) = e_n^2(2\pi f C_{wire})^2$$

TIA current measurement

Spin qubit readout: measurement technique



RF reflectometry



$$BW \cong GBWP\frac{C_F}{C_{wire}}$$

$$S_I(f) = e_n^2(2\pi f C_{wire})^2$$

Increase of the SNR

Current integrator

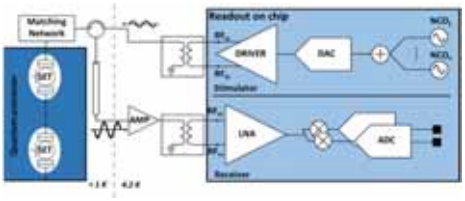
Compact readout based on current measurement

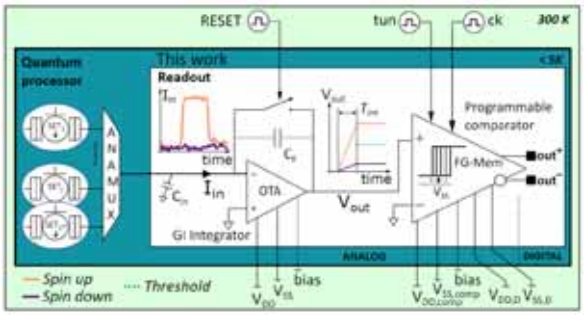
This work

- ✓Fully-integrated 150-nm CMOS technology
- ✓Direct charge-to-digital conversion
- ✓Time division multiplexing architecture
- ✓Low power consumption (1 mW/qubit)

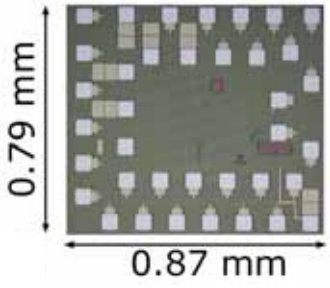
RF reflectometry

- ✓Bulky off-chip components
- ✓Fast analog-to-digital converter / µ-wave signals
- ✓Frequency division multiplexing architecture
- ✓High power consumption (>6 mW/qubit)





150nm bulk CMOS technology



[M. CASTRIOTTA et al., *Solid-state circuits letters* (2023)]

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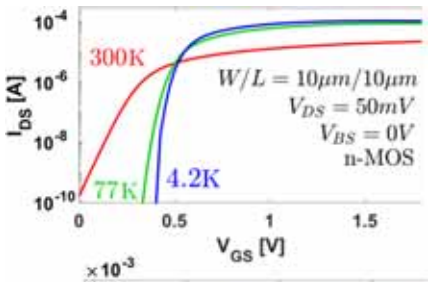
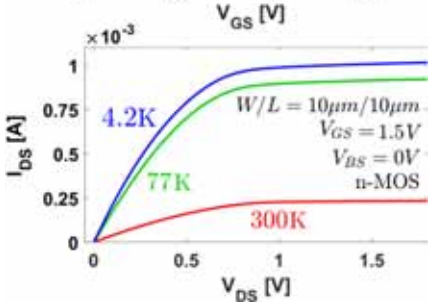
Fully-integrated Cryo-CMOS spin-to-digital readout for spin qubits

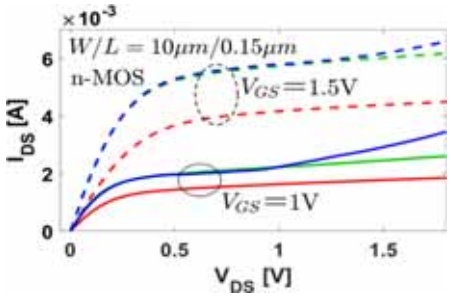
- Introduction to quantum computer and cryogenic electronics
- **Design and characterization of the readout at 4,2 K**
  - **150nm CMOS technology characterization**
  - **Active gated integrator**
  - **Programmable comparator**
  - **Entire readout**
- Conclusion

150nm CMOS technology – DC characterization

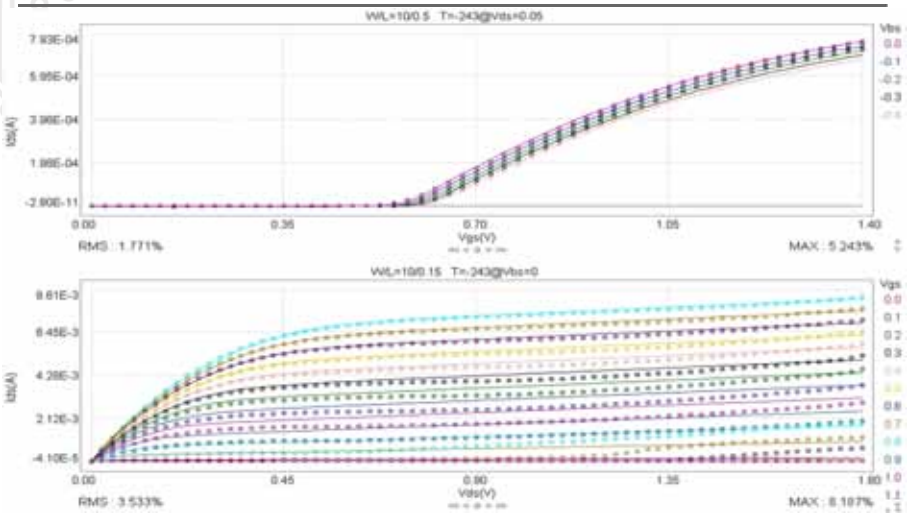


	RT	4.2K	Δ%
V_{Th}	$0{,}4V$	$0{,}56V$	$+40\%$
μ_0	$300\frac{cm^2}{Vs}$	$900\frac{cm^2}{Vs}$	$+200\%$
STS	$70\frac{mV}{dec}$	$7\frac{mV}{dec}$	-90%



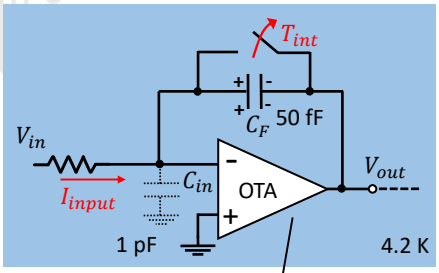


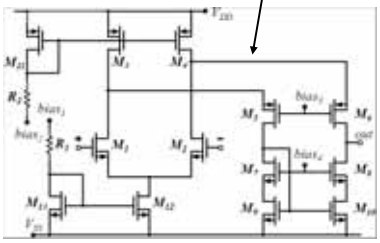
150nm CMOS technology – DC BSIM3v3 model



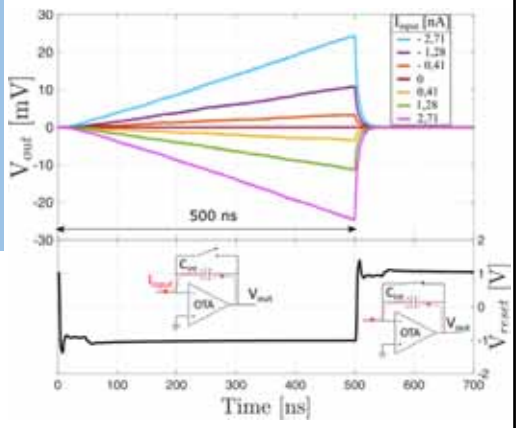
- n-MOS $err_{MAX} \approx 10\%$ $(peak\ 23\%)$
- p-MOS $err_{MAX} \approx 18\%$ $(peak\ 32\%)$

Characterization of the integrator at 4,2 K



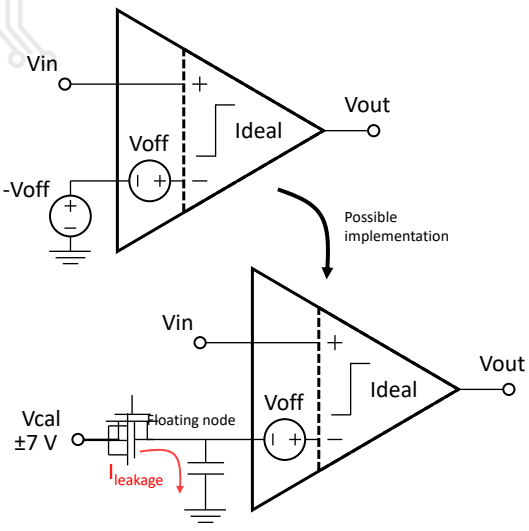


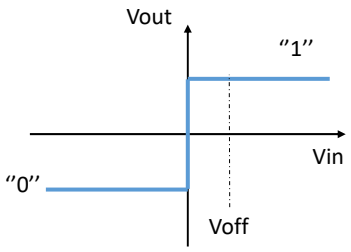
Single stage folded-cascode OTA



- Maximum integration bandwidth: **5 MHz**
- Power consumption: **500 µW**
- Output noise: **700 µVrms**

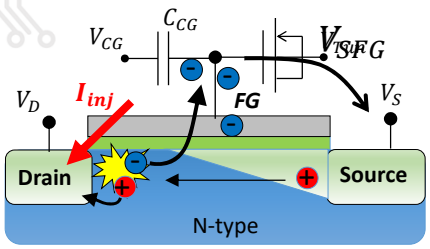
Programmable floating-gate comparator





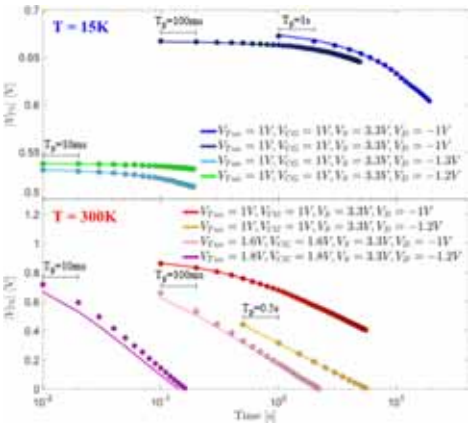
- Compact, low power and permanent solution.
- ~~It requires high voltages to~~ It requires electron injection to enable tunneling.
- It requires calibration.

Hot electron injection in p-type FG transistor



$$I_{inj} = C(V_{SD} - \gamma V_{ov})^3 I_d e^{-\frac{B}{V_{SD}-\gamma V_{ov}}}$$

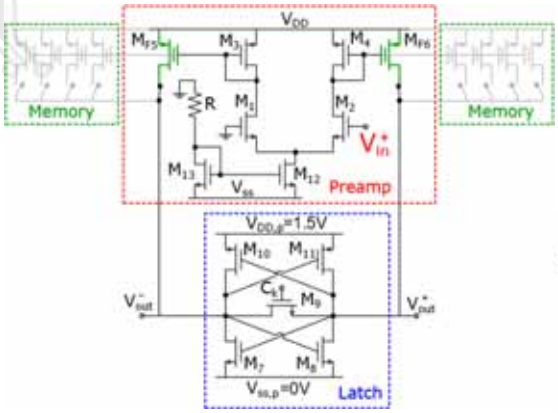
C, B *and* γ are fitting parameters



[M. CASTRIOTTA et al, Solid-state electronics (2022)]

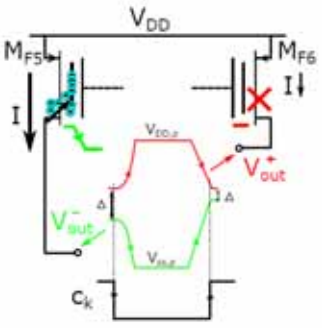
Programmable latched comparator based on FG-transistor

Standard 150-nm CMOS Technology



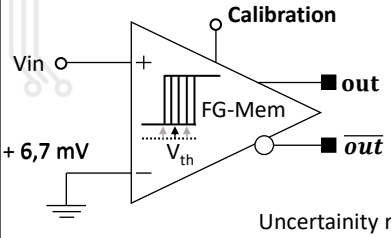
❑ **Programming phase**:

- $V_{DD,p}, V_{ss,p}$ and C_k shift down by 2.3V
- Differential charge injection
- V_{Th} of M_{F5} decreases and its curent increases
- The offset is reduced after each clock cycle

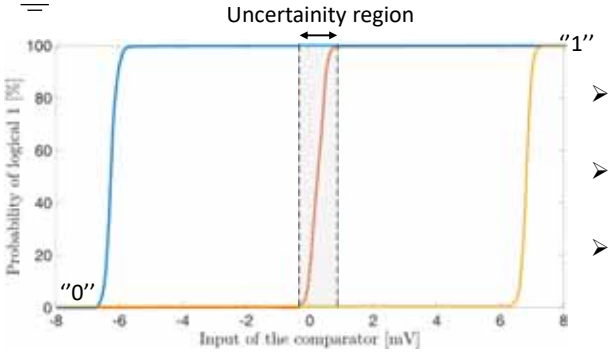


❑ **Evaluation phase:**
Standard latched comparator with threshold storage in a pair of FG-transistor M_{F5} and M_{F6}

Characterization of the FG comparator at 4,2 K

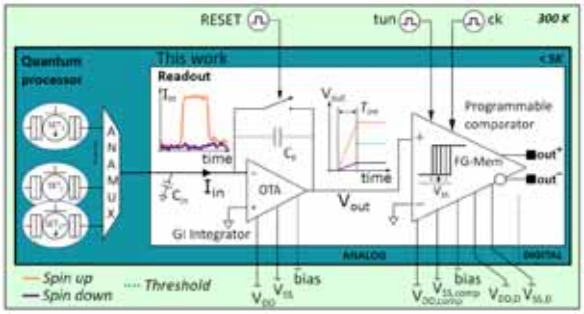


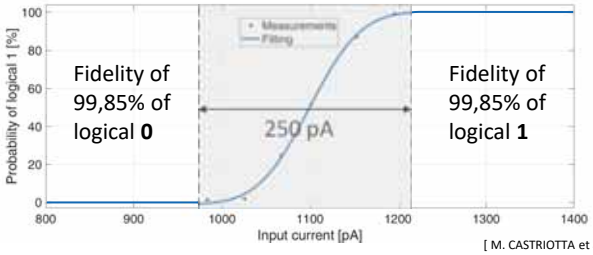
Programming accuracy: **300µV**
Sigma: **840 µV**
Calibration time**: 175 ms**
Fall/rise time**: 2 ns**



- Self-programmable threshold voltage
- Internal permanent FG memory
- Zero power dissipated by the memory

Characterization of the readout at 4,2 K





Threshold current: **1.1 nA**
6 Sigma: **250 pA**
Calibration time**: 175 ms**
Readout time**: 500 ns**
Power consumption: **1,2 mW**

[M. CASTRIOTTA et al., *Solid-state circuits letters* (2023)]

Conclusions

- A fully-integrated CMOS readout operating at 4.2K for semiconductor spin qubits has been developed, implementing a direct charge-to-digital conversion: the SET current is integrated and compared to a specific threshold to output a 1-bit digital signal.
- The architecture does not require RF signals, offchip components, or fast ADCs, as required by readouts based on RF reflectometry.
- BSIM3v3 parameters for the 150-nm CMOS technology have been extracted at 4,2K to design the readout
- The tunnelling current and hot electron injection in a FG transistor have been characterized and modelled at 15K to design the programmable comparator.
- The readout has been characterized at 4.2 K, showing the possibility of resolving spin-dependent current variations greater than 250 pA in 500 ns, well below the decoherence time of semiconductor qubits, with a total power consumption of 1.2 mW

Thanks for the attention