Waferscale Superconducting MCM

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Superconducting Electronics For High-Performance Computing
S-MCM Flip-Chip Approach
Objectives
S-MCM packaging
Large MCM with single mask exposure
Snitched MCM
Waferscale MCM
Summary
Superconducting Electronics For High-Performance Computing

Candidate Beyond-CMOS Technologies

- High speed and ultralow switching energy
- Lossless data transmission
- Waferscale integration
Superconducting Multi-Chip Module (S-MCM)

- 50-ohm clock line
- 10-20-ohm data line
- μ-bump pitch: 35 μm

**Advantages of MCM Process:**
- μ-bump on MCM side
- Known good chips
- Combine multiple technologies
16 Chip MCM

16-chip MCM: 32mm X 32mm
SFQ Chip: 5mm X 5mm
Objectives

Develop a cryogenic package with the following attributes:

- Large MCM
  - Single mask exposure (>32mmX32mm)
  - Stitched mask (Stitched MCM)
  - Combined lithography (Waferscale MCM)

- Large scale integration
  - Accommodate multiple size chips

- Reliable

- Compatible with SFQ, CMOS and Qubit packaging
S-MCM Packaging

Bumped S-MCM

- Superconducting MCM wafer
- Spin resist
- Expose & Develop
- Plasma clean
- Metal deposition
- Resist lift off
- Bumped S-MCM

Flip-chip bonding to daisy chain chip

Packaging

Electrical Characterization

Flip-chip S-MCM attached to PCB for 4K testing

I-V curve of flip-chip S-MCM daisy-chain tested at 4K
Solder Coated μ-Bump

Demonstrate flip-chip packaging of 20 x 20 mm\(^2\) chips on MCM

Representative I-V curves of 20X20mm\(^2\) flip-chip daisy chains at 4K
Resistance: 50-100 μΩ/bump @4K
Large MCM

- Demonstrate 0.8-mm lines around periphery for 48 x 48 mm² MCM with single mask exposure
- Demonstrate MCM bonding with two 20 x 20 mm² chips
Large Superconducting Chip

MCM: 32mm X 32mm
16 (5mm X 5mm) chips

MCM: 48mm X 48mm
2 (20mm X 20mm) chips
Stitched S-MCM

Stitched MCM (70mmX70mm)

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2 MCMs/wafer

0.8μm line at stitch boundary with 0.25μm overlap

MCM439 RT Resistance Data

Wafer Map

Number of RT tested Structures/wafer: 288
RT tested stitched structures/wafer: 96

Stitched MCM(96mmX96mm)

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1 MCM/wafer
200mm MCM Wafer Map

MCM (35mmX35mm)

16 MCMs/wafer
(62.3% wafer area)

Stitched MCM (70mmX70mm)

2 MCMs/wafer
(31.2% wafer area)

MCM (48mmX48mm)

6 MCMs/wafer
Reticle:48mmX48mm
(44% wafer area)

Stitched MCM (96mmX96mm)

1 MCM/wafer
Largest MCM for 4masks/layer
(29.3% wafer area)

Quantum Computing: Devices, Cryogenic Electronics and Packaging│ October 24 – October 25, 2023
Combination of i-line and direct write lithography can reduce total number of masks
Only critical layers containing 0.8-1µm lines can use i-line lithography
Direct write lithography suitable for wider (>1µm) lines
Utilize full wafer real estate
Full Wafer MCM

- 48mmX48mm reticle
- 48mmX48mm reticle
- 96mmX96mm stitched reticle
- 200mm Wafer-scale routing

48mmX48mm MCM
- 96mmX96mm stitched MCM

- 200mm full wafer MCM

- 10-50Ω line
- Stitched MCM 10-50Ω line
- Waferscale MCM 10-50Ω line
Full Wafer MCM Packaging Development

Stitched i-line patterning (96 x 96 mm² on MCM)

Heidelberg direct-write patterning for fan-out wiring (> 1 μm)

Key fabrication processes demonstrated for full-wafer S-MCM’s with lossless superconductive interconnects
• Evaluated large MCM (48 x 48 mm\(^2\)) with single i-line mask exposure
• Demonstrated flip-chip packaging of 20 x 20 mm\(^2\) SFQ chips on MCM
• Developed sequential exposure of two photomasks (A and B), with small overlap (stitched), to realize larger combined MCM (up to 96 x 96 mm\(^2\)) circuit
• Combination of i-line and direct write photolithography demonstrated full wafer MCM fabrication capability
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