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Workshop on

Call for Abstracts – CASS Seasonal School   (Deadline: **August 30**)

Quantum Computing Devices, Cryogenic Electronics and Packaging

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October 24-25, 2023   SEMI Hdqtrs, Silicon Valley, CA USA

*QC-DCEP is planned to be a **hybrid event**, with both in-person and WebEx participation*

Quantum computing technology will revolutionize the high-performance computing landscape by solving complex algorithms with exponential speed-up compared to a classical computer. Those applications will require highly integrated and fault tolerant solutions with potentially millions of qubits. In order to achieve that goal, a number of quantum computing architectures have been proposed in which qubits are realized using superconductors, semiconductors, trapped ions, and neutral atoms. Each technology has a unique set of features and challenges. In addition, a critical part of the solution is the low power and high-fidelity cryogenic control electronics that must be integrated with the physical qubit layer. The task of integrating the physical qubit layer with control electronics requires advanced packaging solutions that are cognizant of the fundamental limitations of the cryocooler in which the entire quantum core resides. Finally, a practical quantum computer requires a software stack to translate the algorithm designed by the Quantum Information Scientist into the physical hardware.

In summary, each layer of the system requires a unique set of skills and knowledge. Therefore, the lectures in this workshop aim to give the audience a brief overview in all of the aforementioned technology sectors including the physical qubit, the cryogenic electronics, packaging and integration, and software compilers. In addition, the material is designed to cover practical use cases and the application space as of today. The intent of this workshop is to bring together engineers of electrical, mechanical, materials and computer science disciplines and physicists to describe the state-of-the-art in all the interconnected fields and the opportunities and challenges for future generations of quantum computers.

Proposals for presentations in the aforementioned fields are solicited, for either in-person or remote presentation, addressing the following technical areas:

> Up to three travel grants of $1,000 each are available for in-person presentations.

Quantum Computing Overview:
- Introduction to Quantum computing
- architecture, devices, survey of the state-of-the-art

QuBits – State of the Art and Roadmap:
- Supercomputing and semiconductor QuBits
- Neutral atoms
- Trapped ions
- Photonics

Cryo-Electronics:
- CMOS detectors and drive electronics
- Charge sensing & direct current detection using TIAs
- Reflectometry based read out apparatus

Software Compilers / Application overview:
- Compilers and compilation techniques
- Software stack challenges and applications
- Quantum Error Correction
- Quantum circuit simulators/emulators
- Hybrid applications, tool-chains and libraries

Packaging/ Assembly:
- Challenges and solutions in heterogeneous integration, scalability, materials, etc.
- 2.5D/3D Packaging with superconductive components, interposers, TSV etc.
- State-of-the-art interfaces and materials in both superconducting and silicon spin qubit platforms

Abstracts or proposals should include a title and a summary of **200⁺ words** with one or two optional figures or diagrams, clearly showing the relationship of the talk to the topics of the Workshop. Acceptance of proposed presentations will be announced by **September 10, 2023**. Most presentations will be 40 minutes long, supplemented by keynotes. **No formal papers will be due**; however, speakers may submit a PDF suitable for use by attendees. Your proposals may be submitted at **https://attend.ieee.org/QC-DCEP**

You may also email your proposal to Imran Bashir, Workshop Chair, at **Imran.bashir@ieee.org**

Please add your name and email address to our **IEEE ListServ Dlist**