REPP 2021

November 3 , 2021

Heterogeneous Integration Roadmap
An Overview

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WR (Bill) Bottoms & Ravi Mahajan

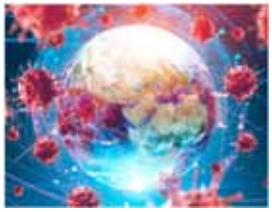
In Collaboration with Heterogeneous Integration Roadmap (HIR) Technical Working Groups Team

Agenda

- REPP Symposium Goal
- Covid 19 & Digital Transformation
- Coming to End of Technology Scaling
- Heterogeneous Integration Roadmap
- Innovations in Heterogeneous Integration Rising Everywhere
- Summary

REPP 2021 Symposium Goals

- This symposium will focus on quantitative methods for reliability, accelerated testing and probabilistic assessment of the useful lifetime of Heterogeneous Integration components including electronic, photonic, and MEMS and sensor packages and sub-systems across different markets & applications.
- Includes failure modes, mechanisms, testing schemes, accelerated testing, stress levels, environmental stresses and machine learning methods for developing and fielding reliable products for the market places.
- The intent is to bring together electrical, reliability, materials, mechanical, and computer engineers and applied scientists from around the world to address the state-of-the-art and future directions in all the interconnected fields of electronic and photonic packaging, with an emphasis on various reliability-related science & technology: design-for-reliability, manufacturing, reliability modeling, accelerated testing, real-time sustainment (prognostics and health management) and digital twins.



COVID-19 Pandemic

- **As we go through the pandemic, we are seeing millions of infections & staggering loss of life, but also incredible heroism, sacrifice, and resilience.**
- **The rapid advancement of vaccine science, and comprehensive vaccines deployment are tremendous achievements in global collaboration**
- **While the Delta Covid Variants are surging, we are hopeful in rapid growth of vaccination. We are optimistic to meet face to face once more not too far into the future**

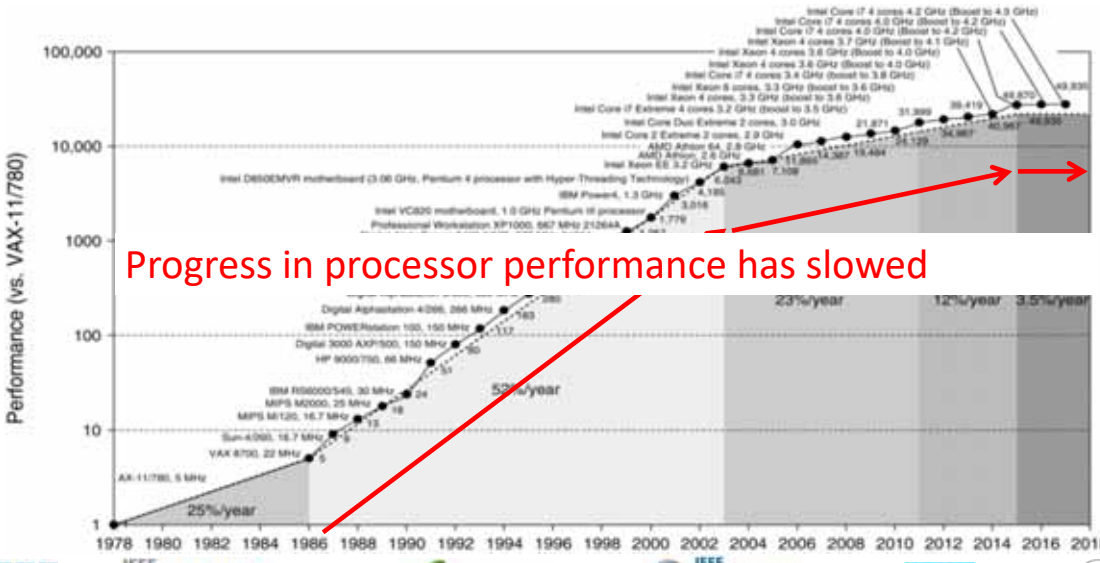
2006 Dec 31	2021 May
Exxon Mobil	Apple
General Electric	Microsoft
Gazprom	Saudi Arabia Oil
Microsoft	Amazon
Citicorp	Alphabet
Bank of America	Facebook
Royal Dutch Shell	Tencent
BP	Alibaba
PetroChina	Berkshire Hathaway
HSBC	TSMC

Source 2006 & 2020: Statista & FXSSI

Technology Companies are leading the digital transformation of the global economy and fueling the AI & ML revolution

40 Years Of Progress In Computing

Source: John Hennessy (Chairman Alphabet) Plenary presentation at DARPA ERI Conference July 23 2018



Moore's Law Economics meeting Headwinds

Source : AMD Lisa Su "Delivering Future of High Performance Computing" Plenary Presentation DARPA ERI Conference July 15, 2019.

Technology Scaling Trends: Exascale in 2021… and then what?

John Shalf (LBNL) "Computing Beyond Moore's Law" International Supercomputer Conference June 18 2019

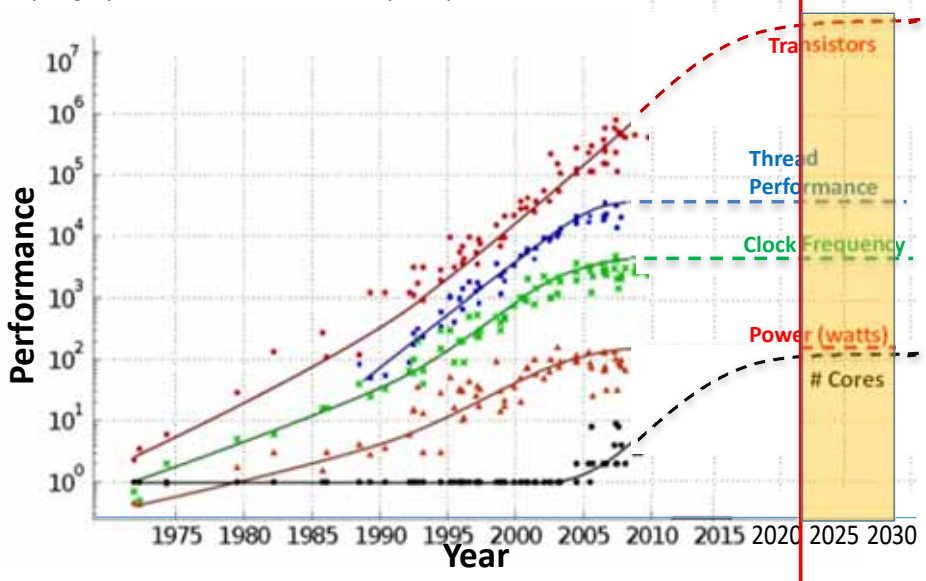


Figure courtesy of Kunle Olukotun, Lance Hammond, Herb Sutter, and Burton Smith – extended by John Shalf

Technology Roadmapping History

1991

World's first Open Source Technology Roadmap, the National Technology Roadmap for Semiconductors (NTRS) sponsored by the US Semiconductor Industry Association (SIA).

1998

NTRS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Technology Roadmap for Semiconductors (ITRS).

2014

The benefits of Moore's Law scaling diminishing and decision was made to end ITRS.

2016

The last edition of the ITRS was published July 8, 2016

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

IEEE Press Release 10-10-2019

PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the **Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines**

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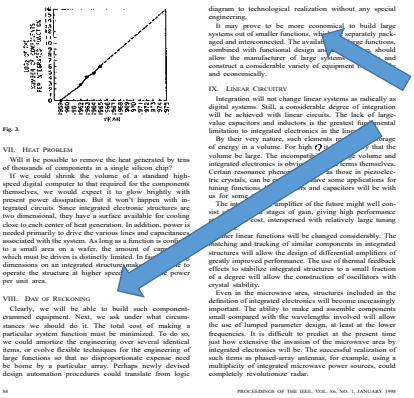
Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

- **Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division**
- **Comprehensively covering microelectronics technology ecosystem**
- **Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions**
- **HIR is the Knowledge Roadmap & Knowledge Supply Chain for the Heterogeneous Future**
- **The 2021 HIR Edition will be launched December 2021**

"Cramming More Components onto Integrated Circuits," *Gordon Moore, Electronics,* pp. 114–117, April 19, 1965.



"VIII. DAY OF RECKONING
----------The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array."

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

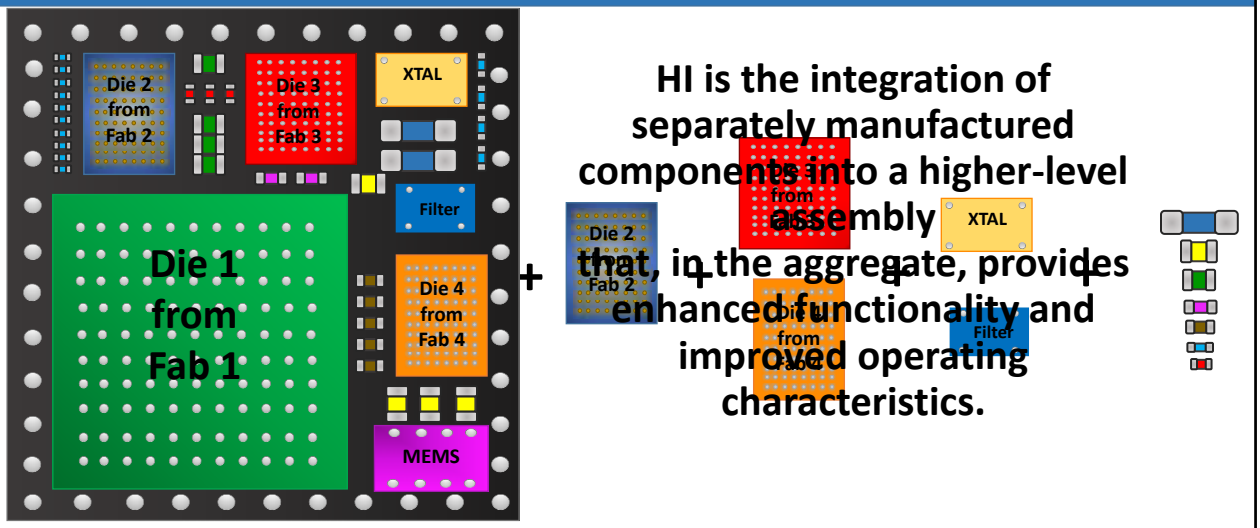
Revisiting Dr Godon Moore's words today.

HI is the integration of separately manufactured components into a higher-level assembly (including SIP & Chiplets) that, in the aggregate, provides enhanced functionality and improved cost, performance & time to market

A visionary message for Chiplets, System-in-Package & Heterogeneous Integration

Heterogeneous Integration:

Heterogeneous by material, component type, circuit type, node and bonding/interconnect method & sources



HI is the integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics.

Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (new chapter for 2021)

Heterogeneous Integration Components

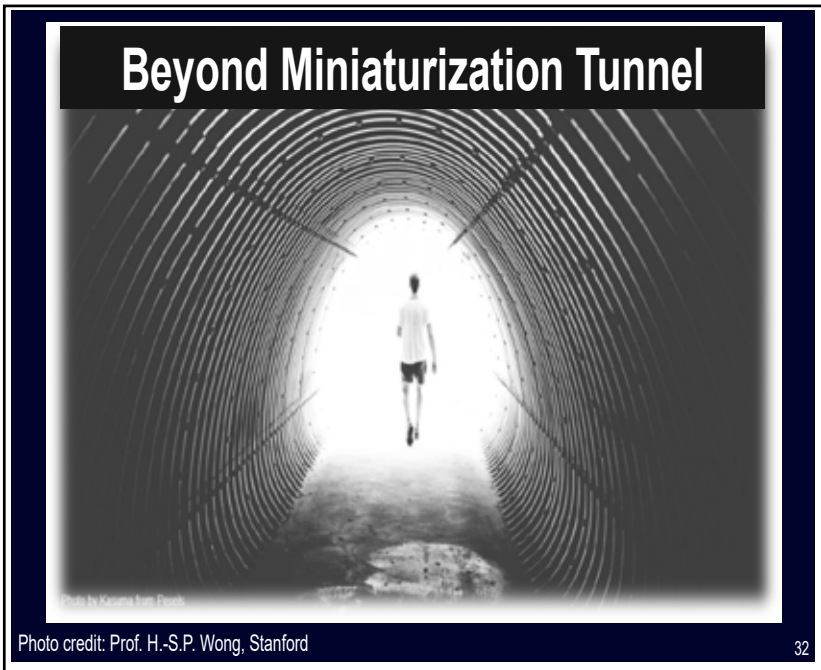
- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communications & Beyond

Integration Processes

- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Co-Design & Simulation

- Co-Design & Simulation – Tools & Practice



At 2020 ERI Conference the Plenary Speaker, (Prof Philip Wong, Stanford University, and TSMC Chief Scientist) gave talk "Future is System Integration. He illustrated semiconductor research near the end Moore's Law like a person walking out of a long tunnel seeing green field & sun light.

During Moore' s Law time the single focus is miniaturization towards the next set of nodes.

As one emerges from the miniaturization tunnel, opportunities for research outlook & innovations becomes infinitely brighter and broader.

Photo Source: S. Mitra, HIR Symposium Feb 24, 2021

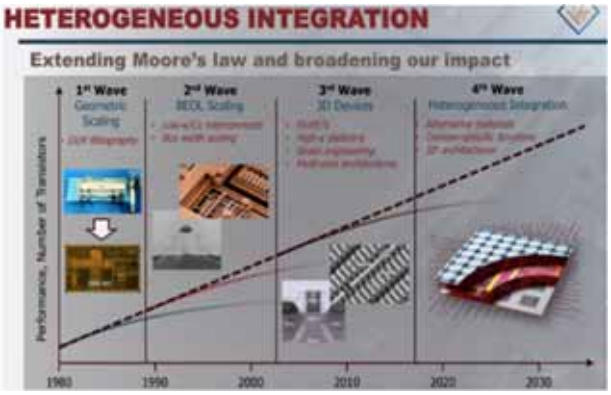
Innovations Rising everywhere!!

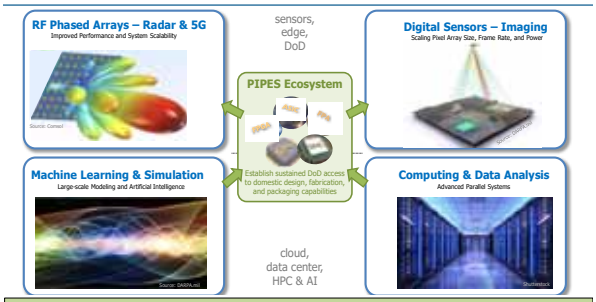
Explorations of new system & package architectures, new materials & new devices, and innovative solutions to design, cost, security, time to market

Virtual Reality
AI & ML for everything
Integrated Photonics
Si Bridge & 3D
WL & PL Fan Out
Brain wave control of complex systems
Nanotube transistors
Qbits
AI + Co-Design & Co-Simulation
Photon Computers
materials design
Implantable sensors for health care
Robotics everywhere
Plasmonic Devices

Presentation: "Accelerating Electronics and Photonics Innovation for Revolutionary Microsystems" Dr Gordon Keeler DARPA, Heterogeneous Integration Roadmap Annual Conference 02-24-2021

Heterogeneous Integration in DARPA Electronics Resurgence Initiative (ERI)





Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.

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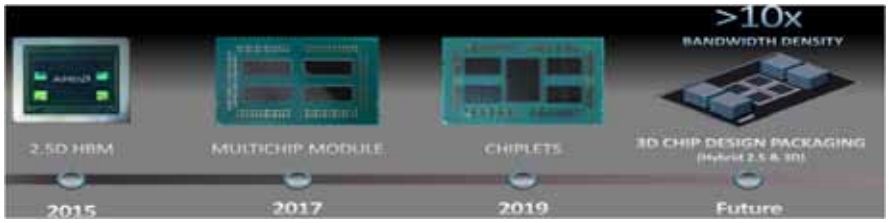
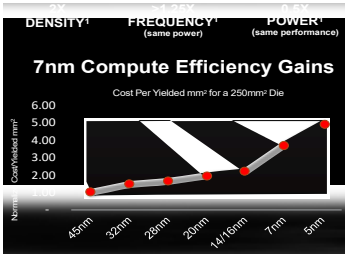
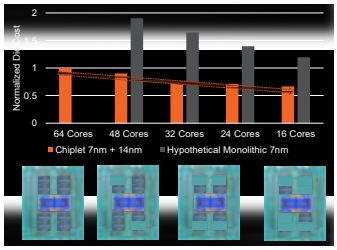
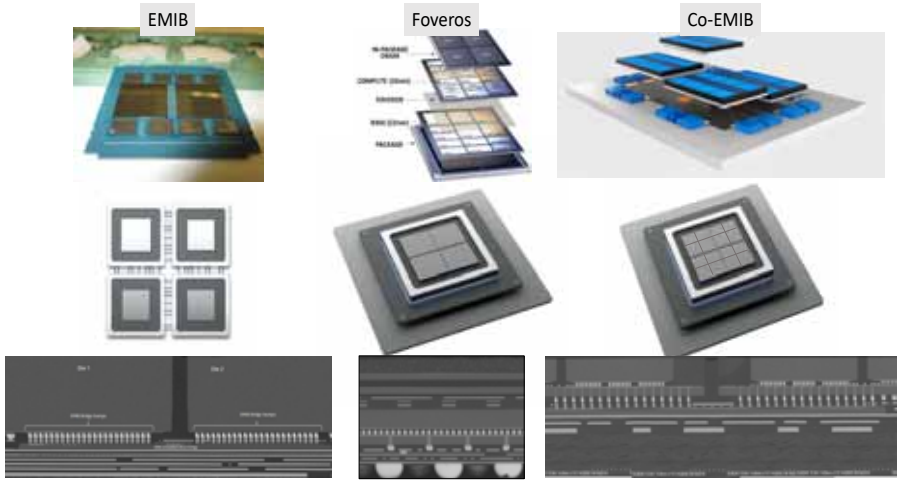
Adv Package Integrations at AMD : 2nd Gen EPYC Chiplets

Source: "Chiplets, How to utilze them, what can they do." Bryan Black: IMAPS keynote October 5-8, 2020









Advance Package Chiplet Integration Technologies at Intel:
EMIB, Foveros & Co-EMIB

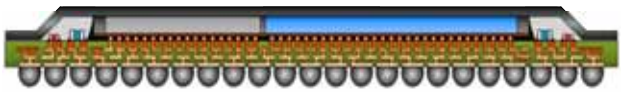
Source: "Adv Package Architecture for Heterogeneous Integration" Ravi Mahajan , Next Gen Electronic System Workshop Binghamton Univ. 10-8 2020.

FOCoS – Fan Out Chip on Substrate

Acknowledgement: :HIR Wafer Level Packaging Chapter John Hunt (ASE)

APU + Memory
GPU + Memory
Networking
SiP/ Modules
AI
Chiplets

Fan Out Compound Die

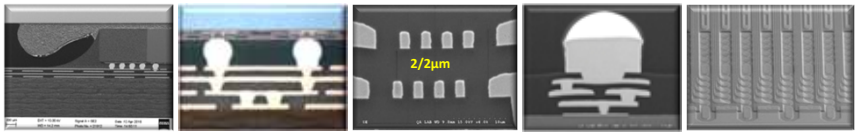


Fan Out Hybrid BGA Package

Capabilities:

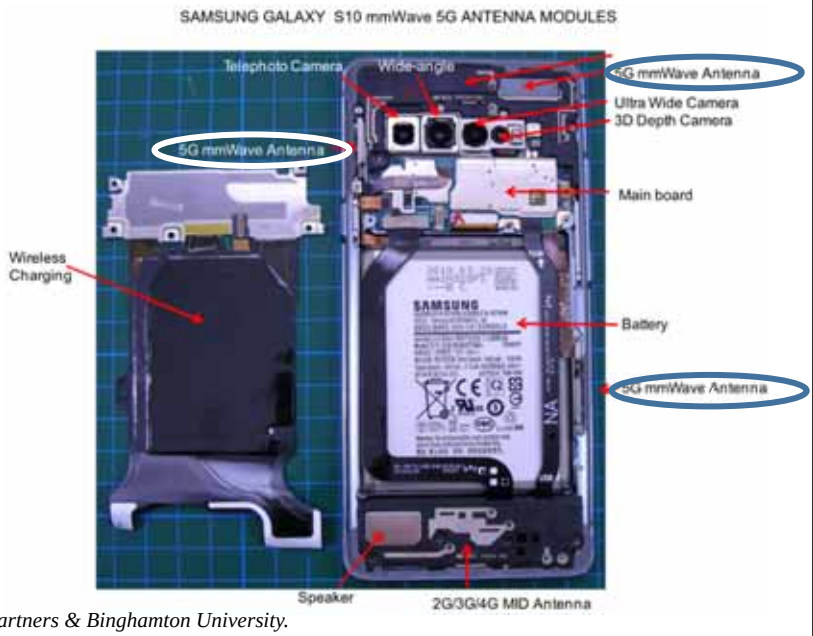
- 2/2µm L/S
- 6 Metal Layers
- 33x38mm FO
- 74x74mm Pkg

- Hybrid solution: FO & BGA
- High density 2D & 3D interconnection in RDL Layers
- HD Fan Out & FlipChip



Multiple products examples since January 2016

Two 5G mmWave Antenna Modules



Source: Prismark Partners & Binghamton University.

Acknowledgement: HIR Mobile Chapter

Semiconductors used in Automotive Industry

Acknowledgment : T Meyer Keynote HIR Workshop IMAPS SiP Conference 08092021

Infotainment	Communication	Safety	Body Electronics	Chassis	Electronic System	Power Train
Dashboard	Comm Systems	Airbag	Control Module	ABS	Alternator	Engine Control
Audio	Local Network	Collision Avoidance	Seat, Window Control	Power Steering	Battery	Transmission
Entertainment	Bluetooth	Parking Assistance	Mirror	Traction Control	Starter	...
GPS	...	Rear Camera	Wiper	Active Suspension	Lightning	
Navigation Display		TPMS	Lightning Control	...	...	
...		...	...			

- Increasing semiconductor content & value in Automotive Future
- 80% of Innovations in automotive enabled by semiconductors
- Envisioning Heterogeneous Integration – System, Function, Reliability, time to market?
- How would Adv Packaging Innovations in Mobile (5G & Smart Phonee) & High Performance Computing & Data Centers be made “applicable” to Automotive Future Applications
- Contributing to global sustainability, climate change & carbon neutral goals.

Summary

- **We are at a unique period in time where the global convergence of technology chaos & business disruption are suddenly joined by the Covid 19 Pandemic still spreading around the world.**
- **There is immense need for a pre-competitive technology roadmap addressing future vision, difficult challenges, potential solutions.**
- **Heterogeneous integration (e.g SiP & Chiplets) is a powerful technology direction for system/subsystem integration.**
- **Reliability is essential while complex for all market applications from Iot, automotive, 5G communications to data centers, advanced aerospace & defense products.**
- **We are looking forward to collaborations & innovations in reliability Science empowered by AI & M L, in this important area for the Heterogeneous Integration Roadmap.**

IEEE REPP Symposium, *HIR Workshop*, Nov 11, 2021

Heterogeneous Integration Systems: Ensuring Reliability

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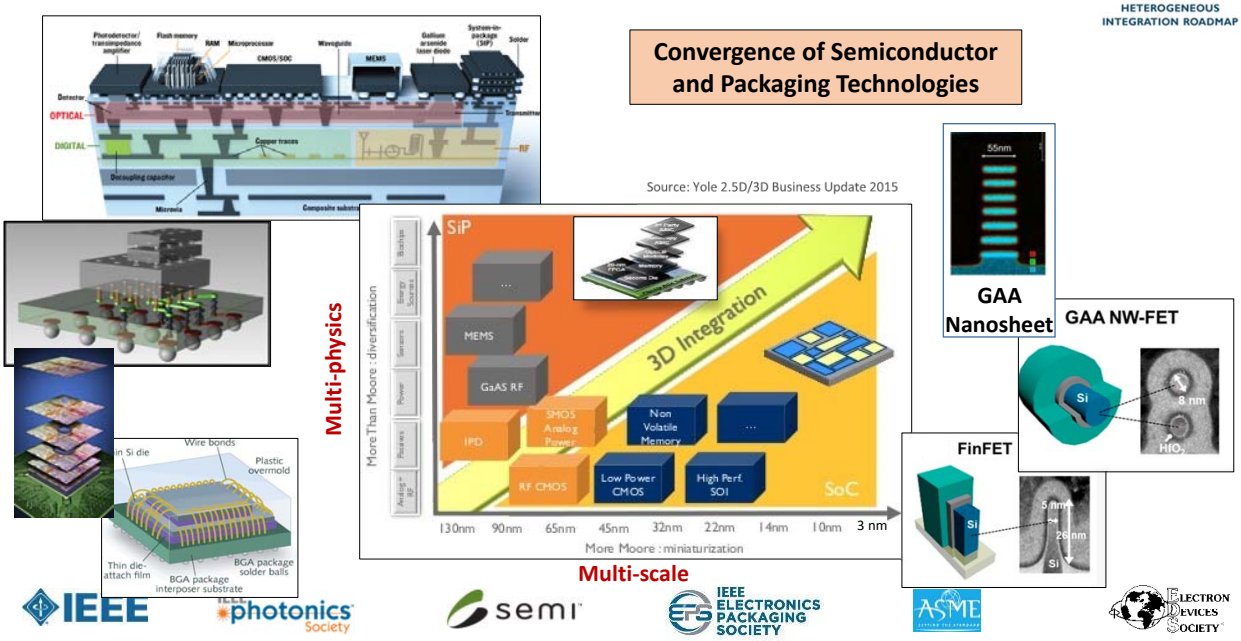
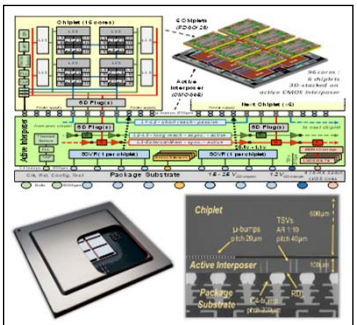
Acknowledgment:
Richard Rao (Marvell Corporation), Shubhada Sahasrabudhe (Intel)

Heterogeneous integration: SysMoore ('More than Moore')

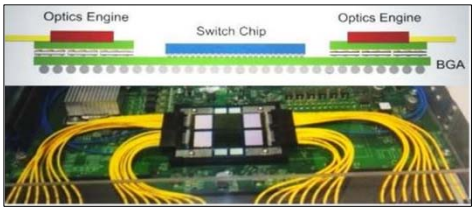


Heterogenous integration

- Electronic (Passive/Active)/Photonic/MEMS/Sensor devices
- Digital; Analog; Logic; Memory; Power; RF
- System, Package (Chiplets) and Wafer levels, including Interconnects and Substrates
- 2.5D and 3D Packaging technologies

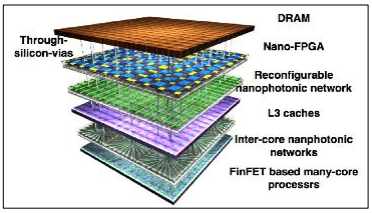


Source: 2020 ISSC



Photonic switching devices and SIP concepts

https://eps.ieee.org/images/files/HIR_2019/HIR1_ch09_photonics.pdf



HIR Technical Working Groups

3-8-2018

HI for Market Applications

- Mobile
- IoT
- Medical, Health & Wearables
- Automotive
- High Performance Computing & Data Center
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- RF and Analog Mixed Signal

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain
- Security
- Thermal Management

Integration Processes

- SiP
- 3D +2.5D
- WLP (fan in and fan out)

Design & Reliability

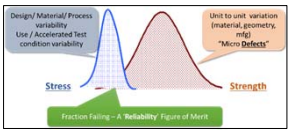
- Co-Design
- Modeling and Simulation
- Reliability

Reliability is a cross-cutting TWG: Cross-TWG interactions

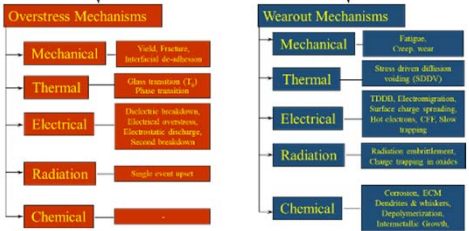
	Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability	Qualification for Reliability	Sustaining for Reliability	Supply Chain	Life Cycle Economics & Cost
Applications	Mobile; IoT; MHW; Automotive; HPC; Aerospace		Electromigration; Materials; Co-Design and Simulation; SCMCI; WLP; 2.5D/3D; Interconnects; SIP; Photonics; MEMS/Sensors; Power; RF/Analog; Test	Mobile; IoT; MHW; Automotive; HPC; Aerospace	Mobile; IoT; MHW; Automotive; HPC; Aerospace	Mobile; IoT; MHW; Automotive; HPC; Aerospace	Supply Chain TWG	No TWGs yet ??
Package Integration				WLP; 2.5D/3D; Interconnects; SIP; SCMCI; Test	WLP; 2.5D/3D; Interconnects; SIP; SCMCI	WLP; 2.5D/3D; Interconnects; SIP; SCMCI; Security		
SiP Technologies				Photonics; MEMS/Sensors; Power; RF/Analog; Test	Photonics; MEMS/Sensors; Power; RF/Analog; Test	Photonics; MEMS/Sensors; Power; RF/Analog; Security		

HI System reliability

Prognostics and Health Management



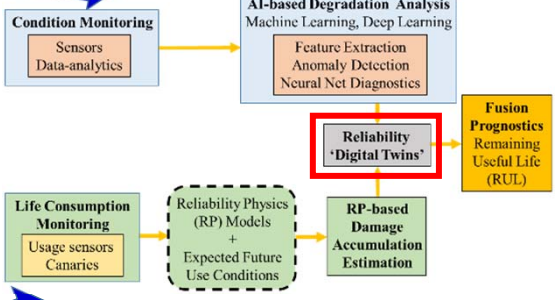
Degradation and Failure Mechanisms



Fusion of bottom-up physics and top-down AI approaches

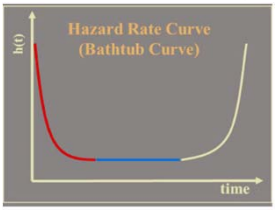
Machine Learning & Artificial Intelligence

Reliability Physics

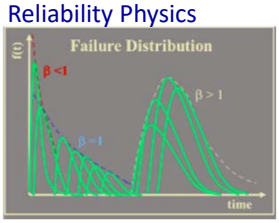


Reliable HI systems: Approach

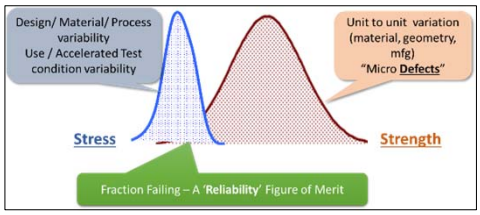
Top down:
Artificial Intelligence and Machine Learning



Bottom up:
Reliability Physics



Reliability Assurance Activities



Multi-physics/multi-scale HI systems require holistic cradle-to-grave methodology

- Reliability Targets
- Life Cycle Conditions
- Design for Reliability
- Manufacturing for Reliability
- Knowledge based Testing for Qualification
- Product Health Management
- Supply chain Integration

Reliability functions in product lifecycle

Proof of Concept	Technical Feasibility	Development/ Design	Product Qual	HV Production	PHM
▪ New Si and Packaging Technology Understanding ▪ Feature/performance ▪ Reliability data collection ▪ Anticipate new failure modes/mechanisms ▪ Identify Reliability Risks/FMEA	▪ Usage stress conditions ▪ Reliability targets ▪ Customer engagement ▪ Reliability/CPI/BLR Risks Evaluation ▪ Test Vehicle Design and Corners ▪ Eng Verification DOE ▪ Deliver Reliability Design Rule and aging model ▪ IP Reliability ▪ Soft errors	▪ Design Verification ▪ Implement reliability solutions in the design flow ▪ Review and assess any violations/trade offs	▪ Optimize assembly process and materials ▪ Reliability hardware/dynamic vector/models ▪ Stress based Qualification ▪ Knowledge based qualification	▪ Early failure rate ▪ Reliability monitoring ▪ Solve field reliability fails ▪ Track field failure rate	▪ Monitor the health of products in field ▪ Adapt voltage to compensate aging ▪ Replace failed interconnect
		Design for Reliability Qualification for Reliability	Manufacturing for Reliability Qualification for Reliability		Sustainment for Reliability

Designing for reliability: Reliability-physics process

INPUTS

Hardware configuration
materials, geometry, architecture

Life Cycle Loading

Operational Loads
Power dissipation, voltage, current, frequency, duty cycle

Environmental Loads
Temperature, relative humidity, pressure, shock. The life cycle includes transportation, storage, handling and Application environments

ANALYSIS

Modeling & Simulation TWG

Multiphysics "Stress" Analysis
Stresses at failure sites
- Electrical
- Thermal
- Mechanical – Vibration & shock
- Diffusion
- Thermo-hygro-mechanical
- Electromagnetic & Quantum fields

Reliability TWG

Reliability Margins
Design margins for relevant failure mechanisms due to stresses at each failure site:
- stress margin for overstress mechanisms
- life margin for wearout mechanisms

Aggregation to the System Level
Reliability block diagrams
Monte Carlo simulations
Bayesian updates with field/test data (if any)

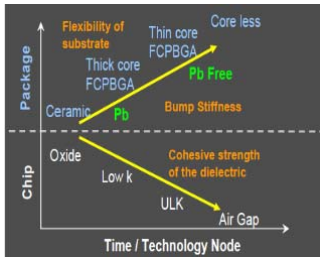
Sensitivity Analysis
Sensitivity of the product durability to changes in: application, design, manufacturing window, life-cycle support methodologies

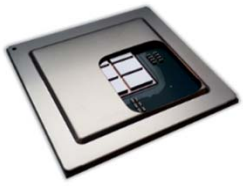
OUTPUTS

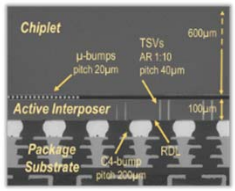
- Ranking of potential failure mechanisms and sites
- Design tradeoffs
- Risk mitigation solutions
- Accelerated test conditions
- Reliability Assessment
- Health Prognostics

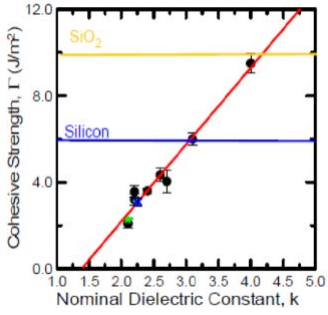
HI systems: CPI challenges

- CPI issues are increasing with newer Si nodes
  - Device and packaging reliability were treated separately in old nodes
  - Advanced Si with low k, CPI requires co-development of device and package
- Low k and Ultra low k introduction
  - Fragile and poor adhesion
- Build up substrate
  - High CTE and warpage
- Pb free or Cu pillar interconnect
  - Higher modulus
- Complex die
  - Big die size
  - Higher power
- Bump on trace
- More advanced packaging induced board-chip-package interaction
  - WLP
  - 2.5D/3D
  - Big FCBGA







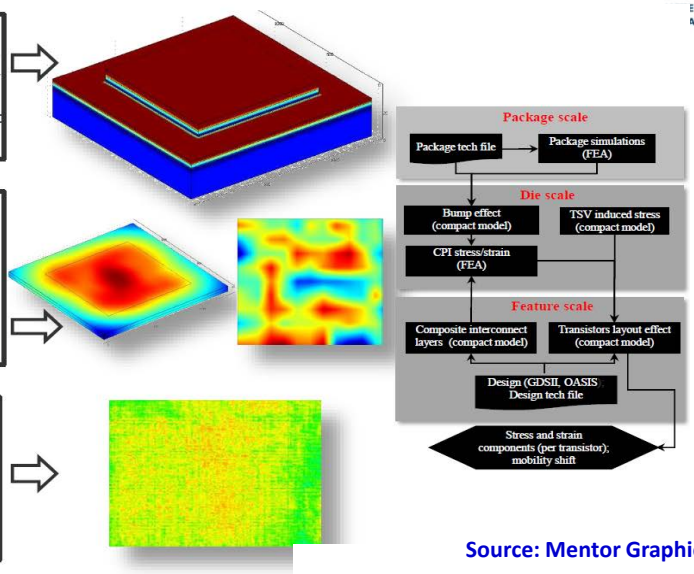


Multi-scale and multi-physics CPI flow

Package-scale simulation (FEA)
Input: geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
Output: field of displacement components on the die faces.

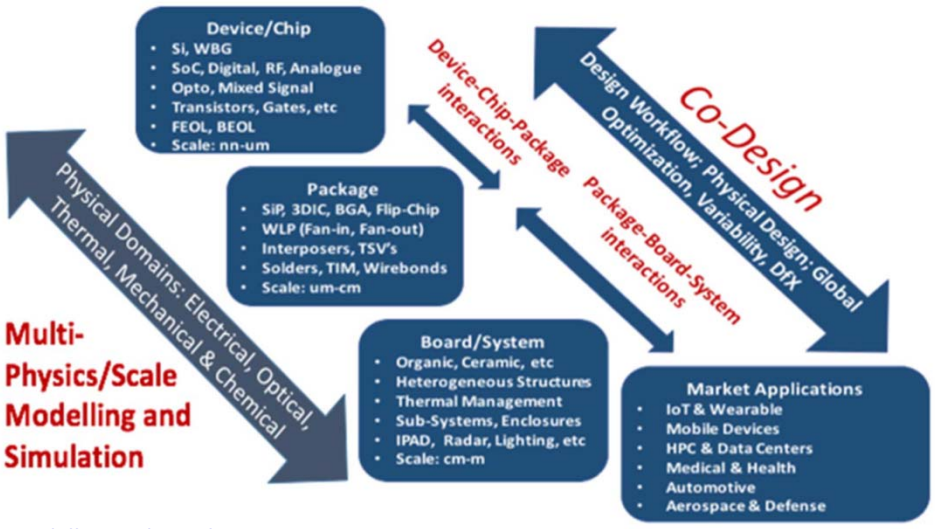
Die-scale simulation (FEA)
Input: geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.
Output: Distribution of the strain components across device layer.

Layout-scale w/feature-scale resolution (compact model):
Input: GDS; distribution of the strain components across device layer.
Output: Transistor-to-transistor variation in stress components



Source: Mentor Graphics

HI Stresses: Physics-based modeling simulation and co-design



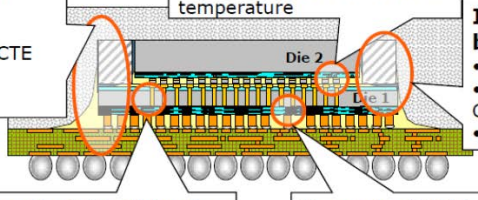
Source: HIR; Modelling and Simulation TWG

HI systems reliability

HETEROGENEOUS INTEGRATION ROADMAP

Impact of Flip Chip Package on 3D chip-stack (CPI)
- Stress induced by Cu-pillars on low-K
- Stress induced by overmold, laminates CTE mismatch
- …

Impact of TSV/uBump on top die
- Built-in stress
- Stress varies as function of temperature



Impact of 3D-SIC bonding on dies
- Stress during bonding
- Stress due to underfill CTE mismatch
- …

Impact of die thinning
- Releases stress
- Strength of die
- …

Impact of TSV on bottom die
- Built-in stress
- Stress varies as function of temperature
- …

Stress/strain can lead to
- mechanical failures due to delamination, peel, fatigue, …
- electrical impact due to parameter shifts, increased variability, EM,…

Multi-scale

Source: IMEC

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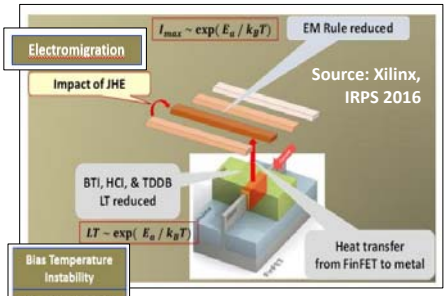
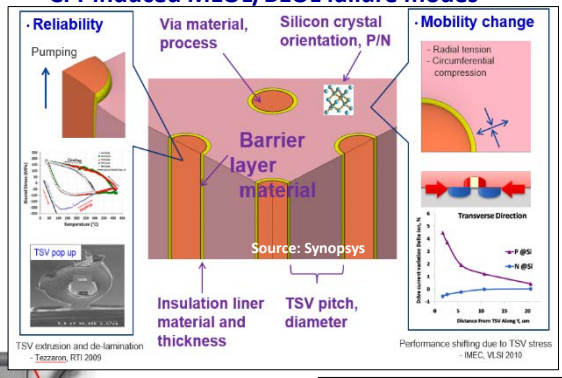
CBPI-induced degradation and failure modes

HETEROGENEOUS INTEGRATION ROADMAP

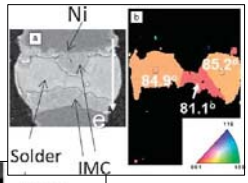
SHE-induced FEOL failure modes

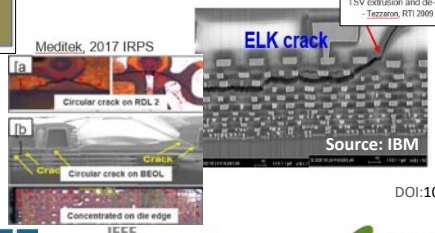


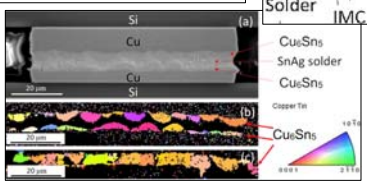
CPI-induced MEOL/BEOL failure modes



Microbumps:
- Material anisotropy
- Length-scale effects







DOI.org/10.1557/mrs.2015.29
DOI:10.1016/j.scriptamat.2020.01.005

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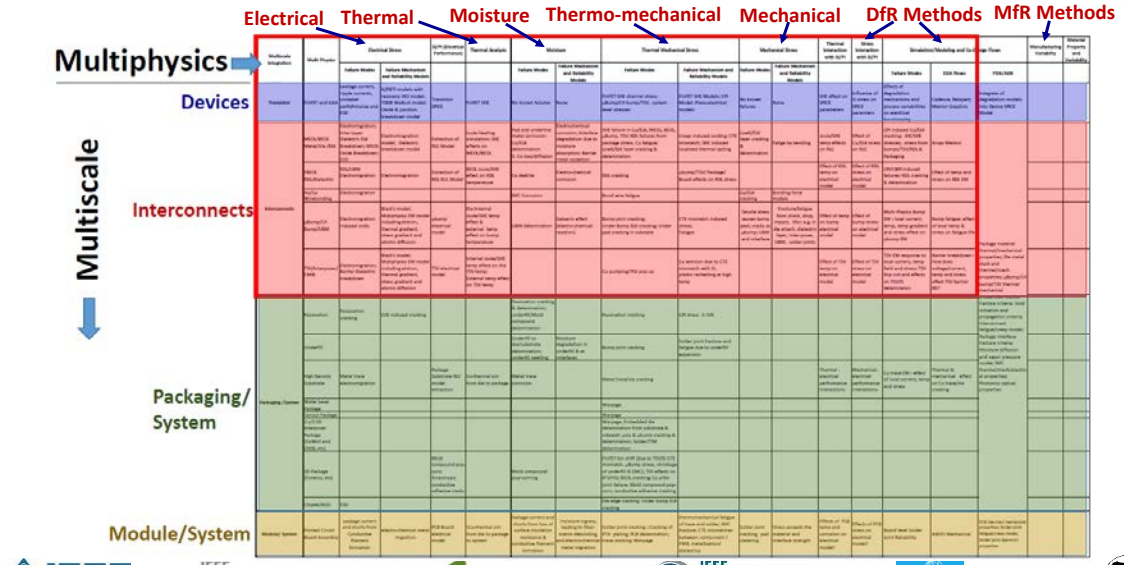
Modes/Mechanisms/Models for degradation & failure

HETEROGENEOUS INTEGRATION ROADMAP



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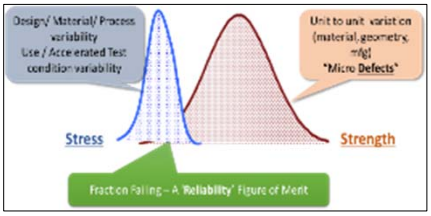
Reliability assurance activities

HETEROGENEOUS INTEGRATION ROADMAP



- Reliability Targets
- Life Cycle Conditions
- Design for Reliability
- **Manufacturing for Reliability**
- Knowledge based Testing for Qualification
- Product Health Management
- Supply chain Integration

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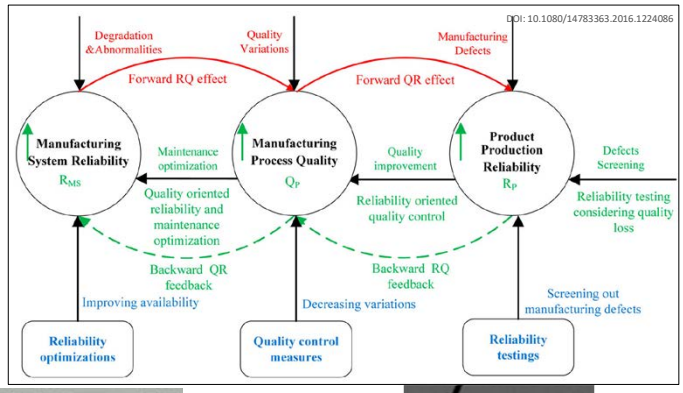
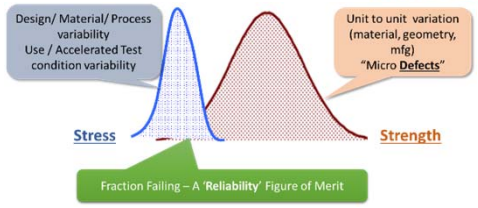
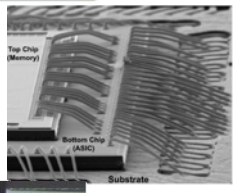
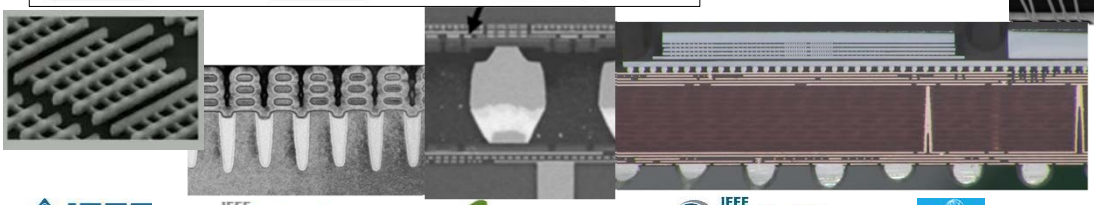
Influence of manufacturing quality on reliability





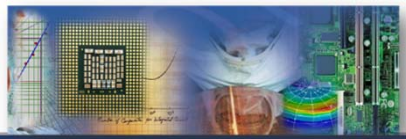
Process metrology poses significant challenge for HI Systems





Qualification and testing: Reliability validation/verification

The changing and challenging landscape



Need for dynamic, flexible models and methods

- Extreme environments
- Extreme usages/ lifetime
- Latest tech nodes
- Diverse components
- New failure modes
- Wide range of Rel tests
- Innovative FA/FI
- Stochastic modeling
- Field Telemetry
- Reliability Physics
- Test time optimizations
- Digital Twin feedback loop

Multi-physics methods to quantify 'stress' and 'strength' distributions at potential sites of failure	Qualification testing needs to be Customized, Knowledge-based and Innovative	Data feedback loop with Digital Twins to validate failure characteristics and run virtual experiments	Integrated PHM - Self-cognizant, intelligent, bio-mimetic hardware to 'age with grace'

Source: Sahasrabudhe (Intel)

Reliability challenges: Future outlook

		Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability	Qualification for Reliability	Sustainment for Reliability	Supply Chain
Applications	Mobile							
	IoT							
	Medical, Health and wearables							
	Automotive							
	HPC & Data Centers							
	Aerospace and Defense							
Package Integration	WLP (FO/FI)							
	2.5D and 3D integration							
	Wafer Singulation and Thinning							
	Chip-package interactions (CPI)							
	Interconnects (TSV8s, µbumps, wirebonds, Flip Chip solder joints)							
	Substrates/Interposers							
	Board Assembly							
	SOC/SIP/SOP[9] formats							
Technologies	Microelectronics > 10 nm							
	Microelectronics <10 nm							
	Photonics & optics							
	MEMS and sensors							
	Power electronics							
	Energy souces (Batteries/PV[6]/FC[7])							
	RF/Analog Devices							

1-5 Years:

Multi-physics fusion approaches for reliability assurance

- Bottom-up *Reliability Physics* based approaches, tools, infrastructure
- Top-down *Machine Learning & AI* based approaches, tools, infrastructure

5-10 Years:

Fusion approaches for co-design (based on 'digital twins') and life-cycle PHM of next-gen robust HI systems

- Fault-tolerant systems
- Resilient systems

10-15 Years:

Fusion approaches for intelligent, adaptive, reconfigurable products with integrated autonomous life-cycle management capability

- Intelligent, self-cognizant systems
- Self-healing systems

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