Avoiding Inelastic Strains in Solder Joint Interconnections of IC Packages

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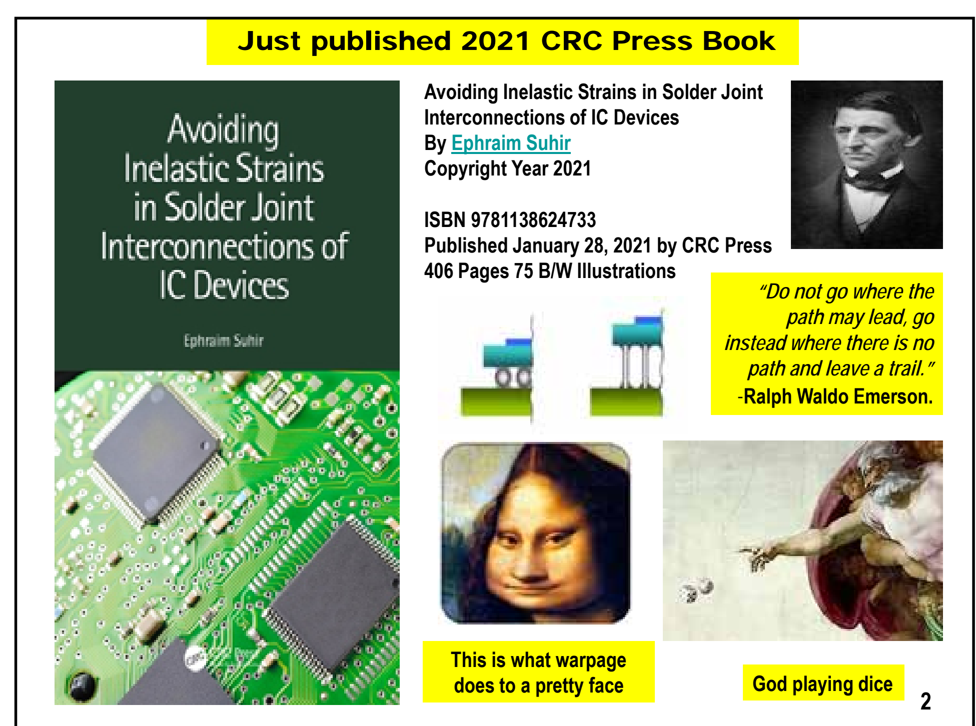
2021 IEEE-EPS REPP, November 11, 2021, Silicon Valley, CA



Contents

Kurt Z. Lewin (1890-1947)

Albert Einstein (1879-1955)

"There is nothing more practical than a good theory"
Kurt Zadek Lewin, German-American psychologist

"Predictive model should be as simple as possible, but not a bit simpler"
Albert Einstein

The following three practically important questions are addressed in this presentation:

I. Could inelastic strains in the solder material be avoided by a rational physical design, and if not, could the sizes of the inelastic strain areas be predicted and minimized (slides 4-7)?

II. Considering that the difference between an highly reliable and an insufficiently reliable product is "merely" in the level of their never-zero probability of failure, and that SJIs are typically the most vulnerable structural elements in an IC package design, could this probability be assessed at the design stage and, if possible, made adequate for the given application (slides 8-14)?

III. Should temperature cycling accelerated testing for SJIs be replaced with a more physically meaningful, less costly, less time- and labor- consuming and, most importantly, less misleading accelerated test vehicle (Slides 15-19)?

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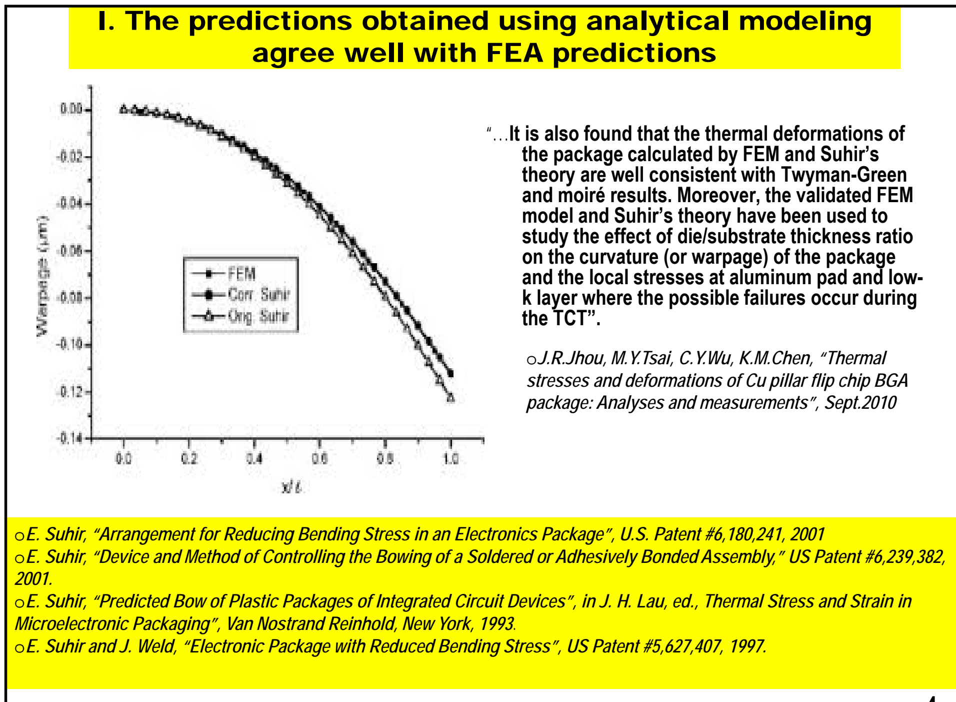
I. The predictions obtained using analytical modeling agree well with FEA predictions



"...It is also found that the thermal deformations of the package calculated by FEM and Suhir's theory are well consistent with Twyman-Green and moiré results. Moreover, the validated FEM model and Suhir's theory have been used to study the effect of die/substrate thickness ratio on the curvature (or warpage) of the package and the local stresses at aluminum pad and low-k layer where the possible failures occur during the TCT".

○*J.R.Jhou, M.Y.Tsai, C.Y.Wu, K.M.Chen, "Thermal stresses and deformations of Cu pillar flip chip BGA package: Analyses and measurements", Sept.2010*

○*E. Suhir, "Arrangement for Reducing Bending Stress in an Electronics Package", U.S. Patent #6,180,241, 2001*
○*E. Suhir, "Device and Method of Controlling the Bowing of a Soldered or Adhesively Bonded Assembly," US Patent #6,239,382, 2001.*
○*E. Suhir, "Predicted Bow of Plastic Packages of Integrated Circuit Devices", in J. H. Lau, ed., Thermal Stress and Strain in Microelectronic Packaging", Van Nostrand Reinhold, New York, 1993.*
○*E. Suhir and J. Weld, "Electronic Package with Reduced Bending Stress", US Patent #5,627,407, 1997.*

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I. Size of inelastic peripheral zones, if any-1

When half the length l_e of the elastic portion of the assembly is large and/or the parameter k of the interfacial shearing stress is significant $(kl_e \geq 2.5)$, which is typically the case for actual SMD assemblies, the following simple formula for the length of the inelastic zone:

$$l_Y = l - l_e = \frac{1}{k}\left(\frac{\tau_{\max}^{\infty}}{\tau_Y} - 1\right)$$

NUMERICAL EXAMPLE

Input data:

Structural Element	Package	PCB	Solder (96.5%Ag3.5%Sn)
Number	1	2	0
Effective Young's modulus, kgf/mm^2	4100	2200	1900.0
Poisson's ratio	0.32	0.30	0.39
Shear modulus, kgf/mm^2	1,553	846	683
CTE, 1/^{0}C	7.0x10^{-6}	17.0x10^{-6}	x
Thickness, mm	2.0	1.5	0.2

Estimated yield stress of the solder material in shear $\tau_Y = 1.3255 \text{kgf/mm}^2$;

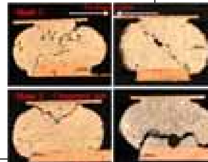
Soldering temperature 180 ^{0}C; Lowest testing temperature -70 ^{0}C;

Assumed change in temperature $\Delta t = 250^0 C$;

External thermal strain: $\Delta\alpha\Delta t = (17.0 - 7.0)10^{-6} x210 = 210.0x10^{-5}$;

Half package length $l = 15mm$

Note: The input data are very tentative



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I. Size of inelastic peripheral zones, if any-2

Maximum elastic interfacial shearing stress at the end of a long and/or stiff assembly:

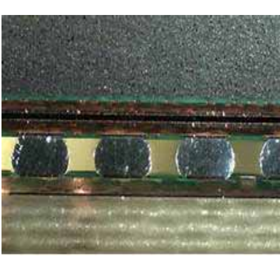
$$\tau_{\max}^{\infty} = k\frac{\Delta\alpha\Delta t}{\lambda} = 0.8774\frac{210.0x10^{-5}}{101.0793x10^{-5}} = 1.8229 kg/mm^2$$

The product $kl = 0.8774x15 = 13.1610$ is significant, so that the factor $\tanh kl$ that considers the role of the assembly size is close to one, and the same maximum interfacial stress would have occurred in the assembly in question, if the yield stress of the solder material were considerably higher than it is.

Length of the inelastic zone

$$l_Y = l - l_e = \frac{1}{k}\left(\frac{\tau_{\max}^{\infty}}{\tau_Y} - 1\right) = \frac{1}{0.8774}\left(\frac{1.8229}{1.3255} - 1\right) = 0.4277mm$$

If the diameter of the peripheral joint is, say, $0.5mm$, then 85.5% of it will experience inelastic strain.



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I. Promising ways to go to avoid inelastic strains

➢**Numerous semi-empirical inverse power law relationships of the Coffin-Manson type have been suggested during the last several decades to predict the low cycle fatigue lifetime of solder materials in IC devices.**

➢**The predictions were based on an assumption that these materials are always stressed above their yield point and, hence, inevitably experience low-cycle fatigue conditions during accelerated testing and in actual operation. But is it always true? Could the inelasic strains in solder materials be avoided?**

➢**Promising ways to go: 1)using low soldering temperatures; and/or 2)selecting low CTE substrates, with better CTE match with Si; and/or 3) using column grid array (CGA), instead of ball-grid-array (BGA) designs; and/or 4) employing inhomogeneous solder systems.**

➢**If this is possible, the elastic, instead of low-cycle fatigue, conditions will take place, and even if the induced thermal stresses are above the solder material's elastic fatigue limit (but still below its yield stress), the material's lifetime will increase dramatically.**

o *E.Suhir, "Avoiding Low-Cycle Fatigue in Solder Material Using Inhomogeneous Column-Grid-Array (CGA) Design", ChipScale Reviews, March-April 2016*
o *E.Suhir, Avoiding Inelastic Strain in Solder Material of IC Devices, CRC Press, 2020*
o *E.Suhir "Inhomogeneous Bonding in Low-Temperature-Soldering: Brief Review".,J. of Electronics and Sensors, 4(1), 2021*

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II. Probabilistic Design for Reliability (PDfR) and Failure-Oriented-Testing (FOAT): Accelerated Test Types

The golden rule of an experiment:
"*The duration of an experiment should not exceed the lifetime of the experimentalist*"

AT type	Product development testing (PDT)	Highly accelerated life testing (HALT)	Qualification testing (QT)	Burn-in testing (BIT)	Failure oriented accelerated testing (FOAT)
Objective	Technical feedback to assure that the taken design approach is acceptable	Ruggedize the product and to assess the reliability limits	Proof of reliability; demonstration that the product is qualified to serve in the given capacity	Eliminate the infant-mortality part of the bathtub curve	Understand the physics of failure, confirm the use of a particular predictive model, assess the probability of failure
End point	Type, time, level, and/or the number of observed failures	Predetermined number or percent of failures	Predetermined time and/or cycles, and/or excessive (unexpected) number of failures	Predetermined time and/or loading level	Predetermined number or percent (typically 50%) of failures
Follow-up activity	Failure analysis, design decision	Failure analysis	Pass/fail decision	Shipping of sound devices	Failure and probabilistic analyses of the test data
Ideal test	Specific definitions	No failures in a long time			Numerous failures in a short time

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II. Accelerated testing: FOAT Could Be Viewed as a Quantified Version of HALT

- High operational reliability of an electronic material or a device intended for aerospace applications is critical and cannot be assured, if the underlying physics of failure is not well understood and its never-zero probability of failure is not predicted and, if necessary, made adequate for the particular material, device and application.

- Failure-oriented-accelerated-testing (FOAT) is critical: a highly focused and highly cost effective FOAT is the experimental basis of the PDfR concept and should be conducted in addition to and, in many cases, even instead of the highly-accelerated-life-testing (HALT), especially for new product, for which no experience is accumulated.

- FOAT could be viewed as an extension of HALT and is a "transparent box", while HALT is a "black box" that is unable to shed light on the physics and the likelihood of failure.

- HALT can be used therefore for "rough tuning" of product's reliability, while FOAT could and should be employed when "fine tuning" is needed, i.e., when there is a need to quantify, assure and even specify the operational reliability of a product.

- The FOAT based approach could be viewed as a quantified and reliability physics oriented HALT and should be geared to a particular technology and application, with consideration of the most likely stressors.

○ *Suhir, E. 'Failure-oriented-accelerated-testing (FOAT) and its role in making a viable IC package into a reliable product', Circuits Assembly, July, 2013*

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II. Multi-Parametric Boltzmann-Arrhenius-Zhurkov Equation

○ S. N. Zhurkov, "Проблема прочности твёрдых тел" (The Problem of the Strength of Solids), *Vestnik Akad. Nauk SSSR* (*Bulletin of the USSR Academy of Sciences*), 11, 1957, pp. 78-82 (in Russian)

○ S. N. Zhurkov, "Kinetic Concept of the Strength of Solids", *Int. J. Fract. Mechanics*, 1965, pp. 311-323

○ S. A. Arrhenius, "Über die Dissociationswärme und den Einfluß der Temperatur auf den Dissociationsgrad der Elektrolyte", *Z. Phys. Chem.*, vol. 4, 1889, pp. 96-116 (in German)

○ L. Boltzmann, "Studien über das Gleichgewicht der lebendigen Kraft zwischen bewegten materiellen Punkten", *Wiener Berichte*, vol. 58, 1868, pp. 517–560 (in German)

Ludwig Boltzmann (1844-1906)

Svante Arrhenius (1859-1927)

Seraphim Nikolaevich Zhurkov (1905-1997)

BAZ model

$$\tau = \tau_0 \exp\left(\frac{U_0 - \gamma\sigma}{kT}\right)$$

Multi-parametric BAZ model

$$P = \exp\left[-\gamma_C C t \exp\left(-\frac{U_0 - \sum_{i=1}^{n}\gamma_i\sigma_i}{kT}\right)\right],$$

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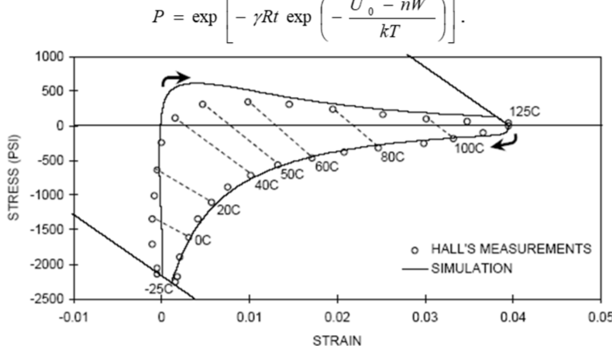
II. Pete Hall's Concept and the Application of PDfR, FOAT, and BAZ Approaches-1

Using BAZ model, the probability of non-failure of a vulnerable material, such as, e.g., solder joint interconnection experiencing inelastic strains during temperature cycling can be sought in the form:

$$P = \exp\left[-\gamma Rt \exp\left(-\frac{U_0 - nW}{kT}\right)\right].$$



Hysteresis loop area of a single temperature cycle for the plastic strain in solder material

Here U_0 is the activation energy and is the characteristic of the solder material's propensity to fracture, W is the damage caused by a single temperature cycle and measured, in accordance with Hall's concept, by the hysteresis loop area of a single temperature cycle for the strain of interest, T, K is the absolute temperature (say, the cycle's mean temperature), n is the number of cycles, $k = 8.6173 \, x10^{-5} \, eV/^0K$ is Boltzmann's constant, $t, \sec$, is time, R, Ω, is the measured (monitored) electrical resistance at the peripheral joint location, and γ is the sensitivity factor for the resistance.

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II. Pete Hall's Concept and the Application of PDfR, FOAT, and BAZ Approaches-2

It could be shown that the maximum entropy of the distribution (1) takes place at the MTTF τ expressed as

$$\tau = \frac{1}{\gamma R}\exp\left(\frac{U_0 - nW}{kT}\right).$$

Mechanical failure, associated with temperature cycling, takes place, when the number of cycles n is $n_f = \frac{U_0}{W}$. When this condition takes place, the temperature in the denominator in the parentheses of the above equation becomes irrelevant

and yields:

Allentown, PA BL facility

$$P_f = \exp\left(-\frac{t_f}{\tau_f}\right),$$

Murray Hill, NJ BL facility

where P_f is the measured probability of non-failure for the situation when failure occurred because of temperature cycling, and $\tau_f = \frac{1}{\gamma R_f}$ is the MTTF.

○ *P.M. Hall, Forces, Moments, and Displacements During Thermal Chamber Cycling of Leadless Ceramic Chip Carriers Soldered to Printed Boards, IEEE CHMT Transactions, vol. CHMT-7, No.4, Dec. 1984*

○ *P.M. Hall, "Strain measurements during thermal chamber cycling on leadless ceramic chip carriers soldered to printed boards", Proceedings, 34th Electronic Components Conference, New Orleans, LA, May 14-16, 1984*

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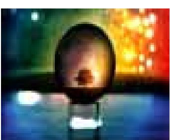
II. Pete Hall's Concept and the Application of PDfR, FOAT, and BAZ Approaches-3

If, e.g., 20 devices have been temperature cycled and the high resistance $R_f = 450\Omega$, considered as an indication of failure was detected in 15 of them, then $P_f = 0.25$.

If the number of cycles during such FOAT was, say, $n_f = 2000$, and each cycle lasted, say, for 20min=1200sec., then the time at failure is $t_f = 2000x1200 = 24x10^5 \sec$ and the above last two formulas yield:



$$\gamma = \frac{-\ln P_f}{R_f t_f} = \frac{-\ln 0.25}{450x24x10^5} = 1.2836x10^{-9}\,\Omega^{-1}\sec^{-1}.$$

$$\tau_f = \frac{1}{1.2836x10^{-9}x450}\sec = = 480.9 hrs = 20.0 days.$$

Applied Probability for Engineers and Scientists

According to Hall's concept, the energy W of a single cycle should be evaluated, by running a specially designed test, in which strain gages should be used.

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II. Pete Hall's Concept and the Application of PDfR, FOAT, and BAZ Approaches-4

Let, e.g., in the above tests this energy (the area of the hysteresis loop) was

$$W = 2.5x10^{-4} eV.$$

The real risk is doing NOTHING

Then the stress-free activation energy of the solder material is

$$U_0 = n_f W = 2000x4.5x10^{-4} = 0.9 eV.$$

In order to assess the number of cycles to failure in actual operation conditions one could assume that the temperature range in these conditions is, say, half the accelerated test range, and that the area W of the hysteresis loop is proportional to the temperature range.

Then the number of cycles to failure is

$$n_f = \frac{U_0}{W} = \frac{0.9x2.0}{2.5x10^{-4}} = 7200.$$

If the duration of one cycle in actual operation conditions is one day, then the time to failure will be

$$t_f = 7200\ days = 19.726\ years.$$

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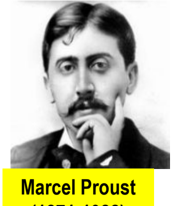
III. Low-temperature/random-vibrations bias as an attractive substitute for temperature cycling accelerated testing-1



Marcel Proust (1871-1922)

Oscar Wilde (1854-1900)

"The only real voyage of discovery consists not in seeing new landscapes, but in having new eyes"
Marcel Proust, French writer

"The truth is rarely pure and never simple"
Oscar Wilde, Irish dramatist, novelist, and poet, The Importance of Being Earnest

- **Temperature cycling as the most widespread today accelerated test is costly, time- and labor consuming, but, most importantly, <u>can result in misleading information</u>, since testing is done in a wide temperature range, much wider than what the material might encounter in actual operation, and, as is known, electronic material's properties are temperature dependent.**

- **Because of that, there is a clear motivation to find another <u>test vehicle that would be less costly and more physically meaningful.</u>**

- **Since the highest stresses occur in SJIs of AS&A at low temperature conditions and crack propagation is accelerated, as is known, by random vibrations, a <u>low-temperature/random-vibrations bias</u> is considered as an attractive substitute for temperature cycling, especially for AS&A applications, when such a bias reflects the actual loading conditions in the field.**

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III. Low-temperature/random-vibrations bias as an attractive substitute for temperature cycling accelerated testing-2

- **Combination of low-temperature, random-vibrations and elevated humidity stressors are suggested therefore as an <u>attractive alternative to temperature cycling</u>.**

- **In our <u>effort reduced to practice</u> random vibrations were considered as a white noise of the given ratio of the acceleration amplitudes squared to the vibration frequency.**

- **<u>Testing</u> has been carried out for two PCBs, with surface-mounted packages on them, at the same level (with the mean value of 50g) of three-dimensional random vibrations.**

- **One board was subjected to the <u>low temperature</u> of -20◦C and another one – to -100◦C.**

- **It has been found, by <u>preliminary calculations</u>, that the solder joints at -20◦C will still perform within the elastic range, while the solder joints at -100◦C will experience inelastic strains. No failures were detected in the joints of the board tested at -20◦C, while the joints of the board tested at -100◦C failed after several hours of testing.**

◦*E. Suhir and R. Ghaffarian, "Solder Material Experiencing Low Temperature Inelastic Thermal Stress and Random Vibration Loading: Predicted Remaining Useful Lifetime", Journal of Materials Science: Materials in Electronics, vol.28, No.4, 2017*

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III. Low-temperature/random-vibrations bias as an attractive substitute for temperature cycling accelerated testing-3

TEST VEHICLE AND DATA

- The actual testing has been carried out at the Reliant Labs, Inc., 925 Thompson Place, Sunnyvale, CA. Two PCB boards, serial numbers QFN-P-07 and QFN-P-08, provided by the customer, were tested.
- Qualmark OVS 2.5LF HALT/HASS Chamber (model # 2.5LF) was used to accommodate the test specimens (one at a time).
- Omega thermocouples were used to measure temperature, and Dytran accelerometer control was used to measure the applied accelerations.
- All test equipment that requires periodic calibration was in current calibration at time of test.
- The test results could be summarized as follows.
- Board #1 was tested at the temperature of -20^0C and the (identical) board #2 at the temperature of -100^0C.
- In both cases the established level of the random 3D vibrations was $50g$.

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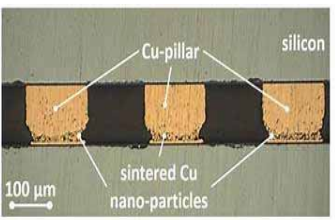
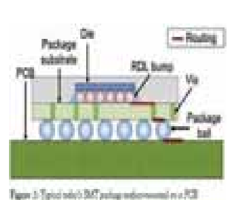
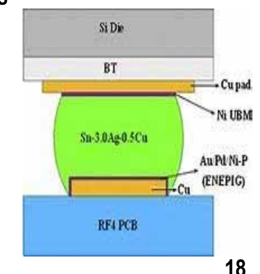
III. Low-temperature/random-vibrations bias as an attractive substitute for temperature cycling accelerated testing-4

- The reason why these temperatures were chosen, is that, according to the above calculations, the -20^0C temperatures were not expected to lead to inelastic static strains, while the -100^0C temperature was supposed to result in appreciable plastic deformations and, hence, in a considerably shorter fatigue life of the solder material.
- Electrical resistance was continuously measured in four corner packages of each board. Prior to testing all the joints showed resistance of about $0.15\mu\Omega$.
- For the board #1 (tested at -20^0C) this level of resistance has not changed after five hours of testing. For the board #2 (tested at -100^0C) opens in two packages were detected after about 1.5 hours of testing, and an increase in the resistance to about 0.9Ω was detected for the remaining two corner packages after about 3.5 hours of testing.
- The total time of testing of the board #2 was about 4.0 hours.







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III. Low-temperature/random-vibrations bias as an attractive substitute for temperature cycling accelerated testing-5

- Hence, the test results have confirmed the general concept that low temperatures in combination with random vibrations might be an attractive accelerated test vehicle for electronic materials and packages, and that there is a significant difference in the fatigue lifetime (remaining useful life) for the solder material that remains within the elastic region (when subjected to moderately low temperatures) and the material that is stressed above this region at significant low temperatures.
- The tests were not continued beyond the above times, since no substantial new information was expected if they would be.
- It should be emphasized, however, that the FOAT should be always conducted, if there is an intent to quantify the RUL.
- For materials that failed within the elastic region the probabilistic Palmgren-Miner "rule of the linear accumulation of damages" can be used to predict the RUL.

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Conclusions

I. It has been determined that there are several promising ways to relieve stresses in SJIs. The viability of these ways should be confirmed experimentally

II. The PDfR concept and highly focused and highly cost-effective FOAT can be used to predict the probability of failure of SJIs and make this it adequate for particular applications

III. The current practice of accelerated testing of electronic products should be revised. Particularly low-temperature/random-vibrations bias seems to be adequate and has a number of advantages over the currently widely used temperature cycling

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THANK YOU FOR COMING

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ANY QUESTIONS?
BUT DO NOT ASK HARD ONES THOUGH

If you, Mr. US President, will put me on the spot with your questions, I , Russian President, will put you on the spot with my answers

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