The Santa Clara Valley (Silicon Valley) Chapters:

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Advanced Packages and Their Reliability Challenges

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Acknowledgments: Ravi Mahajan , Pooya Tadayon, Sandeep Sane, Thomas Huber, Kemal Aygun, Kaladhar Radhakrishnan, Debendra Mallik, Gaurang Choksi, Rahul Manepalli, Chris Baldwin, Sergey Shumarayev, Ram Viswanath, Pat Stover, Wilfred Gomes, Gans Ganesan, Sriram Srinivasan, Ahmet Durgun, CM Jha, Weihua Tang, Upendra Sheth

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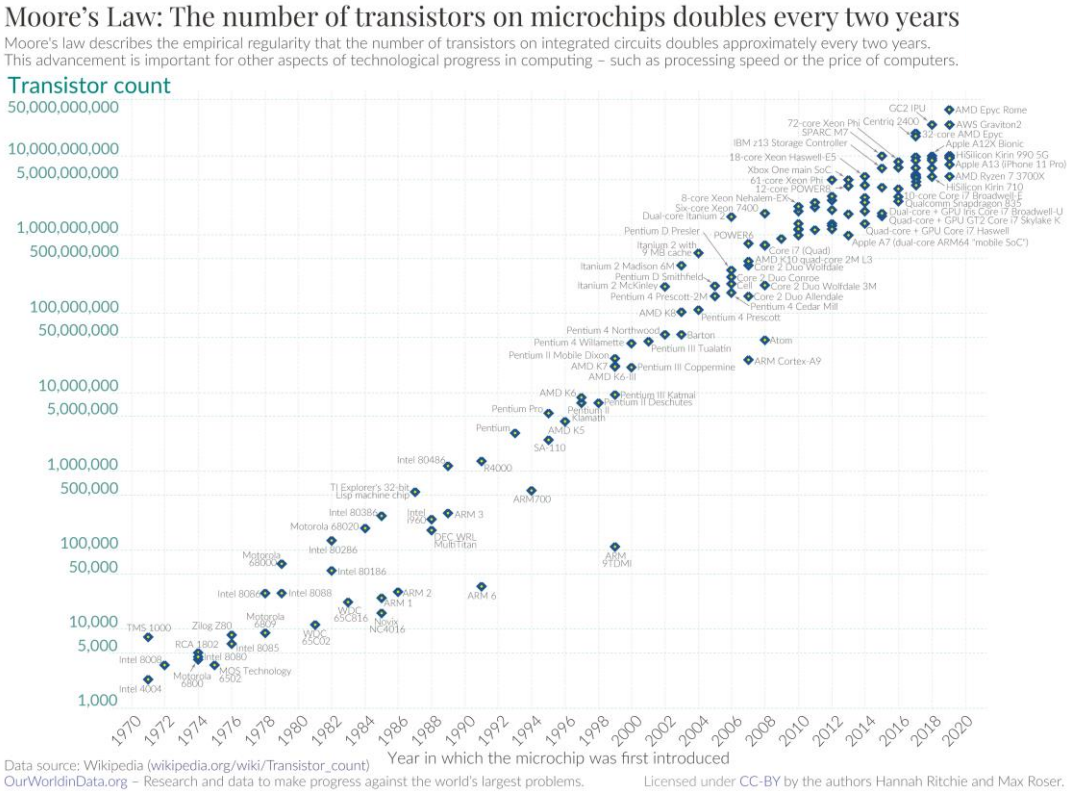
Outline

- Moore’s Law, Challenge and Package Solution
- Key Drivers for Heterogeneous Integration
- Intel Advanced Package Overview
- Challenges and Opportunities
- Summary

Moore's Law, Challenge & Package Solution



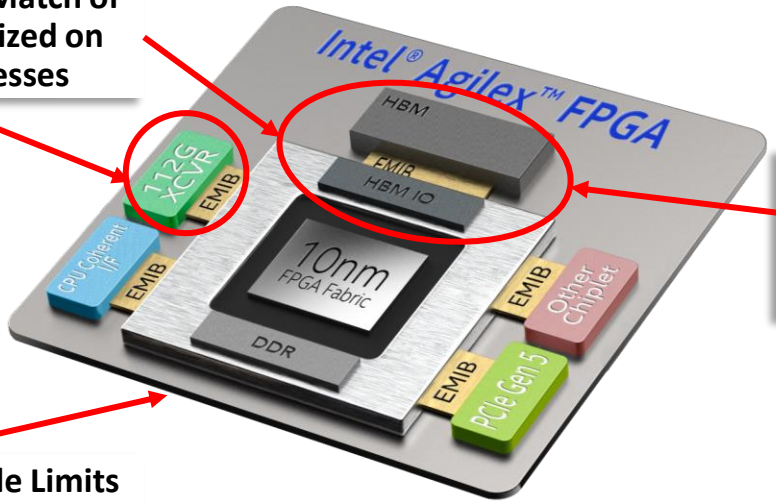
Moore's Law guides the industry to achieve higher performance and lower cost chips

Moore's Law has been challenged since its creation

Heterogeneous Integration (HI) further boosts Moore's Law

Increased Interest in Heterogenous Integration is Driven by

Need to Mix and Match of Diverse IP Optimized on Different processes

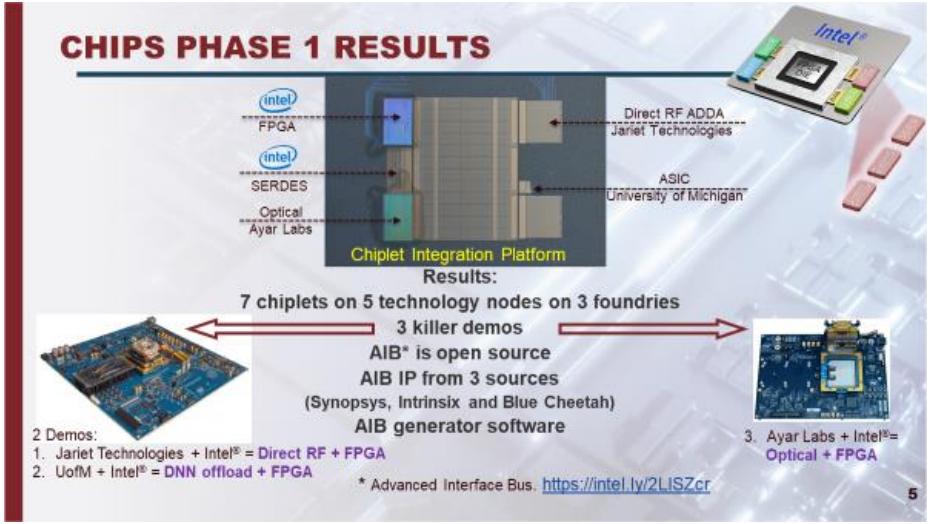


Need for Proximate Memory with a High BW Low Power Interface

Escape from Reticle Limits

Additionally, Yield Resiliency and Time to Market Advantages Make On-Package HI Attractive

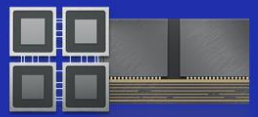
The Package is a Compact HI Platform For Several Interesting Use Cases



Sources: Intel Architecture Day (2021) & ERI Summit (2020). The CHIPS work is supported by the DARPA MTO office (DARPA CHIPS Program))

Intel Advanced Heterogenous Integration Packaging

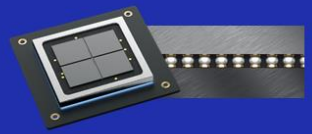
Embedded Multi-die Interconnect (EMIB)



bump pitch **55-40 micron**

- first 2.5D embedded bridge solution
- die to die connection through embedded bridges in substrates

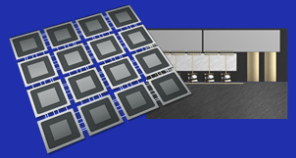
Foveros Technology



bump pitch **50-18 micron**

- wafer level packaging through TSV
- first-of-its-kind 3D stacking solution
- Die to die connection through active interposer

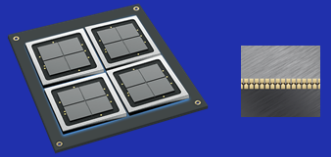
Foveros Omni



bump pitch **25-18 micron**

- next generation Foveros
- Unbounded flexibility with performance 3D stacking technology for die to die interconnect and modular designs

Foveros Direct



bump pitch ⩽ **10 micron**

- Direct Cu-Cu bonding for low resistance interconnects
- Blurs the boundary between where the wafer ends and the package begins

EMIB Technology can be combined with Foveros technologies

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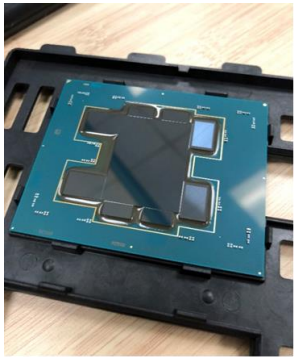
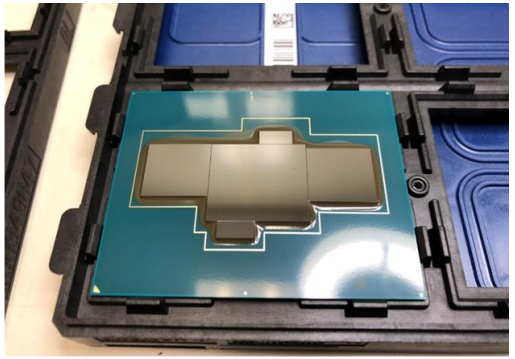
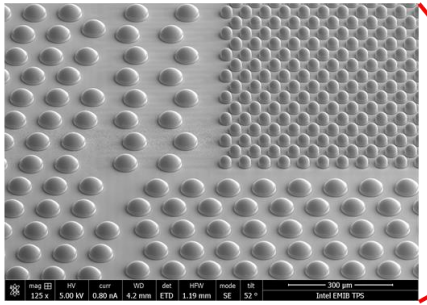
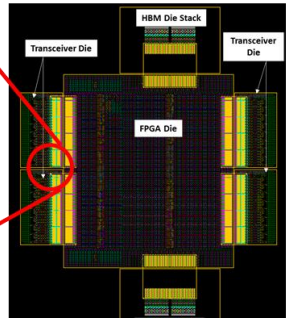
EMIB: Embedded Multi-Die Interconnect Bridge

- Localized high-density wiring
- Multiple Bridges, Multiple Bridge Sizes and Bridge Technologies
- Bridge Mix and Match → Enhanced Design Flexibility
- Bridge silicon costs << Silicon interposer
  - No TSVs, Significantly less silicon area
- Die from Different Foundries
- Large Overall Die Area enabled
- 2x areal bandwidth density
- 4x better PHY power efficiency

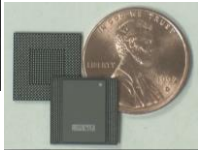


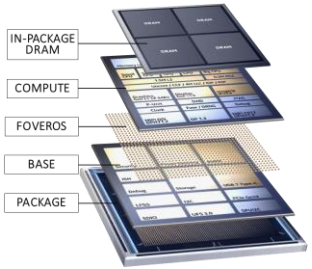


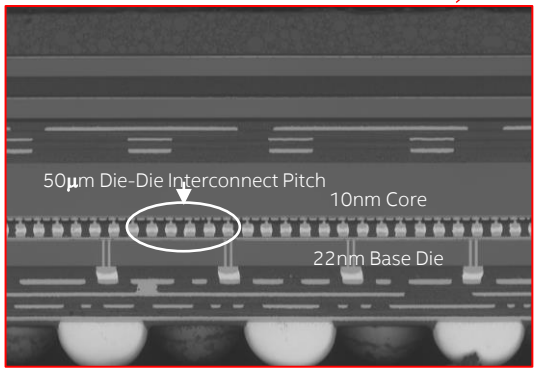


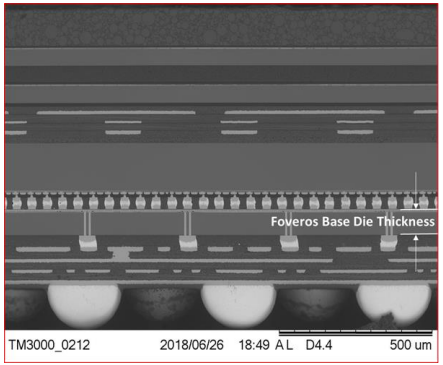


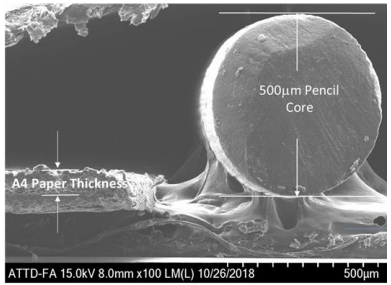
Foveros : High Density 3D Active Stacking

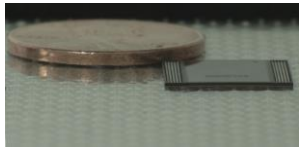












Compact Active Die Stacking : Initial Offering is Single Tile on Base die @ 50µm pitch

We are systematically Scaling tile count, Bump pitch

Meteor Lake @ 36µm Bump pitch

1. *D. Ingerly, et al. "Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices," 2019 IEDM*
2. *W. Gomes et al., "8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm2, 1mm Package-on-Package," 2020 ISSCC*

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Blending Planar and 3D MCPs (EMIB + Foveros)

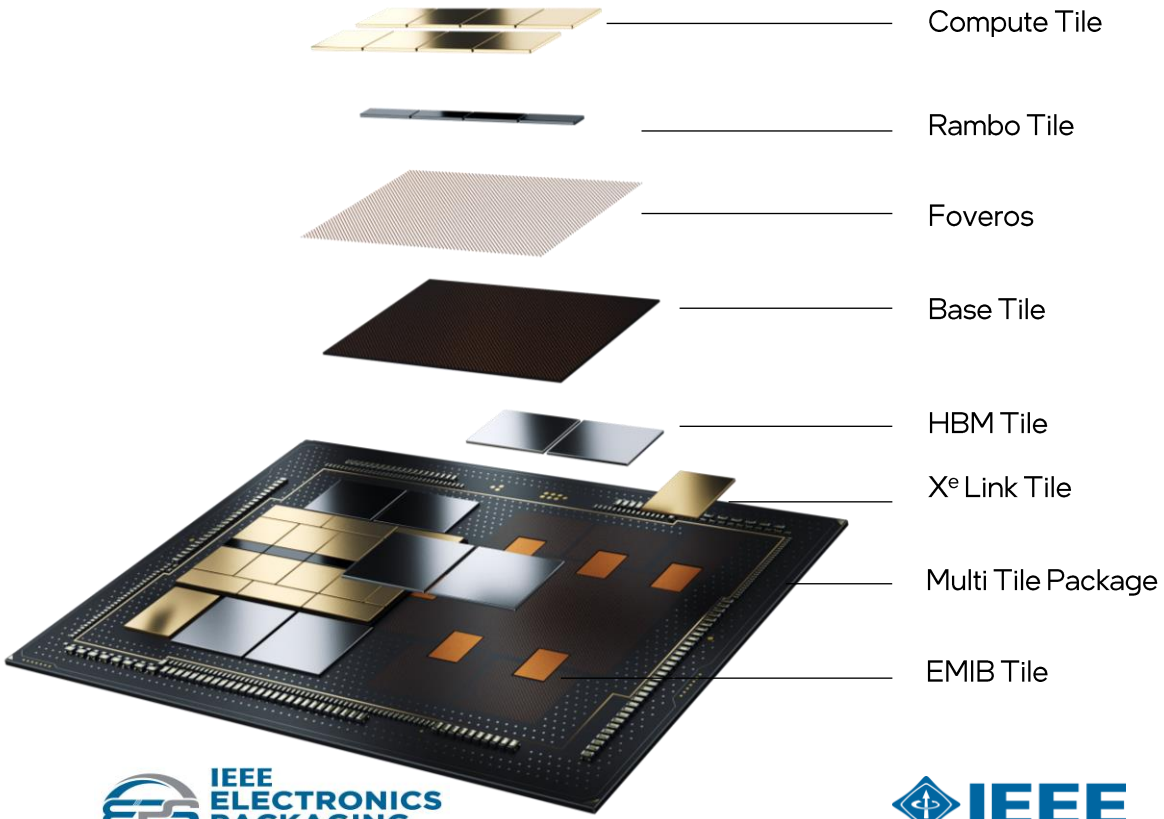
Ponte Vecchio

SOC

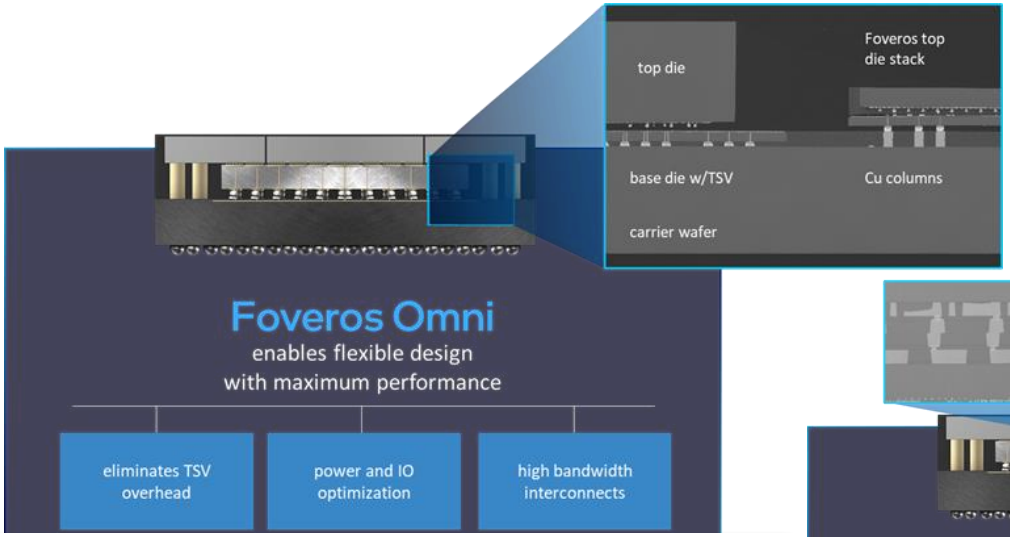
>100 Billion Transistors

47 Active Tiles

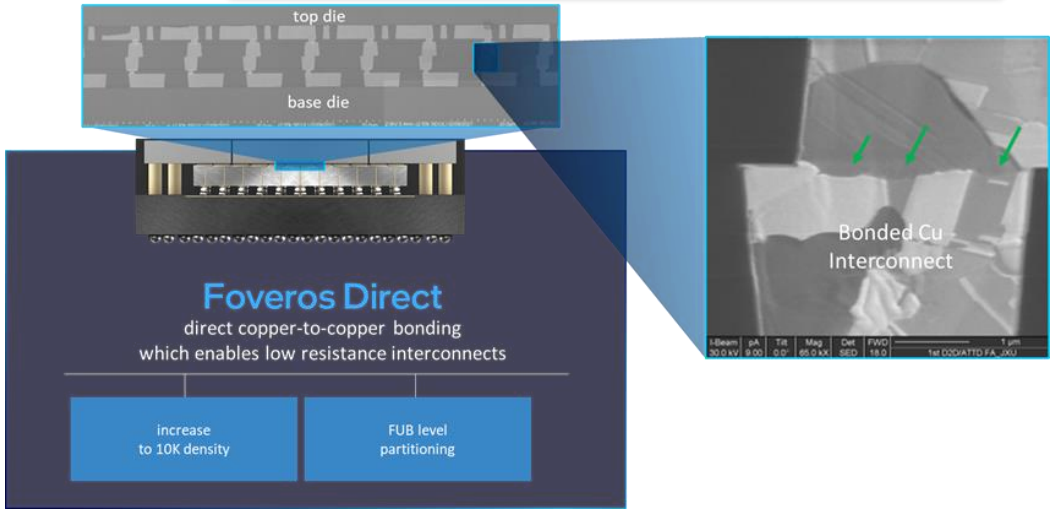
5 Process Nodes



Packaging Innovations In The Near Future: Foveros Omni and Foveros Direct



- Rich Interconnect Portfolio allows greater mix-and-match and better/independent interconnect optimization for Power and IO



- Pitch Scaling from 25µm → ≤ 10µm leads to an order of magnitude increase in IO/mm^2 (1600 → ≥ 10,000)

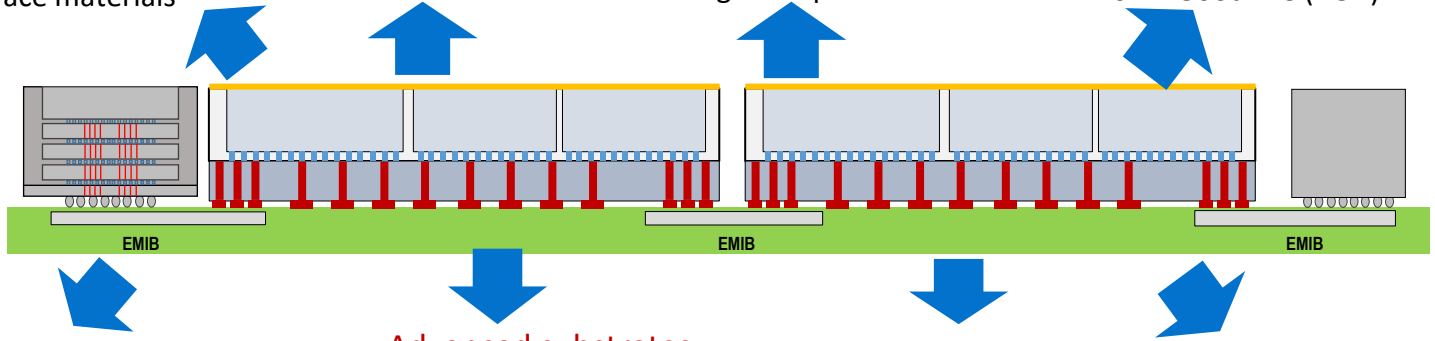
Challenges and Opportunities

Better materials
- UF/mold: Flow, Reliability, Warpage
- Fluxes: joint quality/cleanability
- Thermal interface materials

Thermal Management
- Design/process co-optimization
- Thermal materials

Improved Electrical
- Bump Current carrying capability
- HSIO and Power Delivery
- Design co-optimization

Package yield
- Die-Die, Die-Wafer, Die- Substrate
- Improved alignment/ bump Coplanarity
- Stacked die coplanarity
- Known Good Die (KGD)



External IP/die/pkg integration
- Passivation/bump compatibility
- Design rule/ Design co-optimization

Advanced substrates
- Improved bump coplanarity
- Fine pitch/ Multi diameter bumping
- High density routing

Warpage Management
- Design-Process-Materials co-optimization
- Nova SMT total solution

Acceptable Reliability
- Temperature cycling
- Electromigration
- Temperature/humidity/Bias

Equipment/ Material/Process/ Design Co-optimization key to Heterogeneous Assembly & Packaging

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Sources: R Mahajen and S. Sane, " Advanced Packaging Technologies for Heterogeneous Integration " , ***HOT CHIPS 2021***

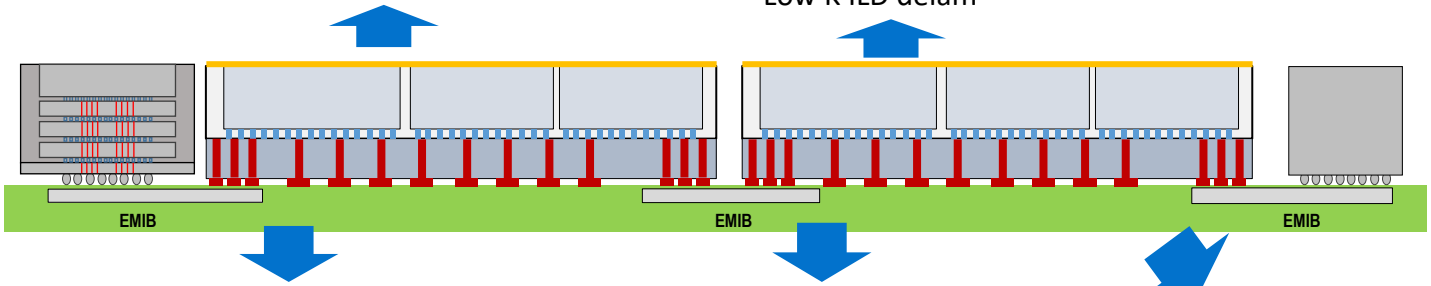
Reliability Challenges

Thermal Reliability

- TIM1 delam/ degradation
- Lid delam/degradation

Si Reliability

- Die crack
- Passivation crack/delam
- UBM / Via delam/crack
- Low K ILD delam



Substrate Reliability

- Trace Crack / Short
- Via Crack/delam
- Dielectric crack/delam
- Solder Resist crack/delam

Package Reliability

- UF/mold crack/delam
- Interconnect joint crack
- Imax / Electromigration
- Solder extrusion

Board Level Joint Reliability

- Solder joint fatigue/crack
- Pad delam or cratering

Equipment/ Material/Process/ Design Co-optimization Key to Meet Reliabilities

Summary

- **Heterogenous integration is a key enabler of performance and cost moving forward**
- **Intel invented several advanced packaging architectures and applied them in Client, Server and Discrete Graphics products to provide unprecedented levels of Heterogeneous Integration**
- **The next generation of Innovations in Heterogeneous Integration will offer increased partitioning opportunities with an enhanced interconnect portfolio and significant increases in interconnect density**
- **Equipment/ Material/Process/ Design Co-optimization is the key to meet yield, performance, cost and reliability targets of complex advanced packages**

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