Santa Clara Valley Section Chapters of

IEEE Electronics Packaging Society | IEEE Photonics Society | IEEE Reliability Society

Call for Abstracts -- REPP

Symposium on Reliability for Electronics and Photonics Packaging

Reliability, Failure Modes and Testing for Integration of Electronics and Photonics (SiPh)

12-13 November 2020 Silicon Valley, CA USA

General Chair
Gnyan Ramakrishna, Cisco

Technical Program Chair
Richard Rao, Inphi

Keynote Speakers
Ephraim Suhir

Asia Liaisons
Xueren Zhang, Xilinx
Dr Pei-Haw Tsao, TSMC

Europe Liaison
Gromala Jakub, Bosch

Administrative Chair
Paul Wesling, HP (retired)

This symposium will focus on quantified reliability, accelerated testing and probabilistic assessments of the useful lifetime of electronic, photonic, MEMS and MOEMS materials, assemblies, packages and systems in electronics and photonics packaging. This includes failure modes, mechanisms, testing schemes, accelerated testing, stress levels, and environmental stresses.

The intent is to bring together electrical, reliability, materials, mechanical, and computer engineers and applied scientists to address the state-of-the-art in all the interconnected fields of electronic and photonic packaging, with an emphasis on various reliability-related aspects: design-for-reliability, manufacturing, reliability modeling and accelerated testing.

Proposals for presentations in the fields of Reliability for Electronic and Photonic Packaging are solicited, addressing the following technical areas:

At the Component/Sub Component Level
- Lasers, Diodes, Fan-out IC, PLC fabrication challenges and developments
- Multiphysics interactions
- 2.5D/3D/Heterogeneous integration
- On-chip integration of subcomponents
- Wafer scale technology

System Level of Integration
- Integration challenges for electronics and photonics co-packaging
- Optical coupling and index matching at the system level
- Thermal management challenges at the system level

Testing for Yield
- Burn-in testing
- Testing methods at subcomponent level
- Testing methods at co-packaging level
- Methods and methodology to track yields
- System level testing and yields at scale

Co-Design and Simulation
- Modeling schemes
- Global optimizations

Accelerated testing
- Accelerated testing techniques and methodologists for different electronic, photonic and MEMS technologies, designs and applications
- Accelerated testing and how it translates to Field conditions and deployment
- Highly focused and highly cost-effective failure-oriented-accelerated-testing (FOAT) to understand the physics of failure

Failure modes/Failure Mechanisms
- Accelerated models
- Sub-component specific FA modes
- FA techniques
- Material characterization and failure criteria

Abstracts or proposals should include a title and a summary of **300-500 words** with one or two optional figures or diagrams, clearly showing the relationship of the talk to the topics of the Symposium. Acceptance of proposed presentations will be announced by **15 September 2020**. Presentations will be 30 minutes long, supplemented by keynotes and invited talks. **No formal papers will be due**; however, speakers may submit a PDF suitable for use by attendees. Your proposals may be submitted at **https://attend.ieee.org/repp**

You may also email your proposal to Richard Rao, REPP Program Chair, at **richard.rao@ieee.org**

Please add your name and email address to our **IEEE ListServ Dlist.**