Recent Prospectives and Challenges of 3D Heterogeneous Integration

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Introduction

- As Moore's Law approaches its limits, the process of chip process miniaturization has been slowing down and the industry needs to create new paradigms.

- Semiconductor product packaging efficiency has gradually developed from 10% to 90% or even 100%.

- Advanced packaging technologies have emerged in the way of heterogeneous integration technology implementation.
Introduction

- Looking ahead, more 3D FO-WLP forms (e.g., Package on Package) are expected to be available for making thin-shell high-performance storage.

- Advanced packaging platforms will use different processes for different package types and require relevant testing to ensure product quality after packaging.


Recent advance of 3D heterogeneous integration

- DARPA proposed the state-of-the-art heterogeneous integrated packaging (SHIP) program in **mid-2019**. The SHIP program demonstrates a new set of state-of-the-art integration, design, assembly, and test methods.

  ![SHIP Diagram](image)

  **Sources:** DARPA, DARPA Common Heterogeneous Integration and IP Reuse Strategies (CHIPS), 2020.

- AMD launched data core CPU with a **3D chip stack**, the third-generation EPYC Milan-X processor with 3D V-Cache technology, on **March 21, 2022**.

  ![AMD Processor Diagram](image)

Recent advance of 3D heterogeneous integration

In July 2020, Intel introduced "Lakefield", using the new high-density Co-EMIB interconnect technology, which combines EMIB 2D packaging and Foveros 3D packaging technology, its process and relationship with previous technologies.


IMEC focused its 3D integration technology development in 2006 on three different directions.

IMEC uses "hybrids" for W2W bonding.

With 3D interconnect pitches of 5 m and below now required, so 3D SoC integration technology solutions require wafer-to-wafer (W2W) bonding methods to meet performance requirements.

Recent advance of 3D heterogeneous integration

➢ At TSMC’s Annual Technology Symposium in **August 2020**, TSMC announced their 3D Fabric technology for Communication, IoT, transportation and HPC.

➢ 3D Fabric offers fully integrated chip designs from front-end to back-end and different kinds of integrated packaging, including TSMC-SoIC, CoWoS and InFO.

Challenges of 3D heterogeneous integration

**• Thermal Management**

➢ HIR proposes a novel cooling method for 3D chip stack structures by designing embedded channels.

➢ At the same time, the embedded cooling imposes new requirements on the 3D chip stack co-design, including the layout and size of the fluid channels and the compatibility with the chip stack power and signal electrical interconnections.
Challenges of 3D heterogeneous integration

### Thermal Management

For 3D heterogeneous integration of microsystems, new thermal technologies are gradually being developed, and new thermal management technologies and their characteristics are currently being developed as shown in the table.

<table>
<thead>
<tr>
<th>Thermal solution</th>
<th>High end chip scale heat flux</th>
<th>First Chip to heat sink/cold plate</th>
<th>Heat sink/cold plate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced multi-chip air cooling with integrated vapor chamber</td>
<td>0.85 W/mm²</td>
<td>0.1 °C/W for Al</td>
<td>0.085 °C/W for Cu</td>
</tr>
<tr>
<td>Water cooled separable module level cold plate</td>
<td>2.50 W/mm²</td>
<td>0.35 cm²K/W</td>
<td>0.028 cm²K/W</td>
</tr>
<tr>
<td>Water jet impingement</td>
<td>4.6 W/mm²</td>
<td>N/A</td>
<td>0.025 cm²K/W</td>
</tr>
<tr>
<td>Water immersion cooling</td>
<td>0.82 W/mm² (A device area of 12.5 mm² at thermal budget of 50 °C Fluid temperature = 25 °C)</td>
<td>N/A</td>
<td>0.18 cm²K/W</td>
</tr>
<tr>
<td>Two-phase immersion cooling</td>
<td>1 W/mm² (A device area of 12.5 mm² at thermal budget of 50 °C Fluid temperature = 25 °C)</td>
<td>N/A</td>
<td>0.5 °C/cm²W</td>
</tr>
<tr>
<td>Micro channels in the device with single phase water flow</td>
<td>About 7.60 W/cm² 71 °C temp rise, chip size = 1 cm²</td>
<td>N/A</td>
<td>0.09 °C/cm²W</td>
</tr>
<tr>
<td>Micro channels in the device with two phases</td>
<td>About 10.20 W/mm² 58 °C temp rise, chip size = 0.25 cm²</td>
<td>N/A</td>
<td>0.056 °C/cm²W</td>
</tr>
</tbody>
</table>


### Test and Reliability

Due to the increasing complexity of micro and nano manufacturing processes, micro systems need to consider reliability related issues during processing.

The table illustrates several types of problems that often arise in 3D heterogeneous integration and the measures to solve them.

<table>
<thead>
<tr>
<th>Reliability Issue</th>
<th>Consequences</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV related stresses</td>
<td>A significant CTE mismatch can occur between Cu and Si, which can lead to local stress in the surrounding Si matrix during thermal excursions.</td>
<td>The TSV is filled with appropriate physical properties polymer.</td>
</tr>
<tr>
<td>Solder-based joints</td>
<td>Chip thermal cycling leading to embrittlement and voiding leading to fatigue induced failure. Stress mismatch caused by built-in warpage of the tube core and PCB.</td>
<td>Use additional adhesive filler as underfill.</td>
</tr>
<tr>
<td>Underfill</td>
<td>During the capillary filling process, flux residues are trapped in the bottom filler material and eventually voids appear, leading to reduced strength and corrosion.</td>
<td>Flux will be completely removed after the bonding process.</td>
</tr>
<tr>
<td>Passivation and moisture ingress</td>
<td>The poor adhesion of the passivation layer due to the presence of impurities generates osmotic pressure leading to moisture intrusion causing corrosion.</td>
<td>Use organic materials that are as hermetically sealed as possible.</td>
</tr>
<tr>
<td>Electromigration</td>
<td>soldered contacts can form voids, where electromigration and heat migration superimpose and amplify the void effect.</td>
<td>Improve metallization system and use dry processes.</td>
</tr>
<tr>
<td>Micro-bump technology</td>
<td>Excessive pressure during the welding process can cause the solder to bridge. Heat cracking can occur at the interconnections during operation.</td>
<td>Use solder resist and set better parameters for the soldering process.</td>
</tr>
</tbody>
</table>

Conclusion

- 3D heterogeneous integration technology of microsystems is gradually developing in the direction of **3D stacking, multi-functional integration and hybrid heterogeneous integration**, which makes microsystems have the advantages of **high integration, low power consumption, micro-miniaturization and high reliability**.

- 3D heterogeneous integration will become a means for microsystems to achieve the **optimal comprehensive performance, function and cost, and become a technical link between chip and system integration**.

- **The new materials, processes, and methods** in 3D heterogeneous integration technology will definitely play a great role in promoting the development and manufacturing of the whole industrial chain.

THANKS

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