Electronics quality and reliability for critical applications that adopt new technologies and designs

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Purpose and Abstract

- **Title**
  - Electronics quality and reliability for critical applications that adopt new technologies and designs.
- **Purpose**
  - Review and adapt the quality and reliability methods for design and qualification of leading-edge microelectronic technologies for critical and safe applications.
- **Abstract**
  - Modern societies are accustomed to low-cost, ubiquitous applications and underlying technologies to enhance life experiences and increase productivity. People interact with each other, machines and technology using low-cost semiconductors that are efficient, sufficiently capable and short-lived. Networked computation and automated electronic-mechanical systems with a mix of heterogeneous technologies are expected to perform, be safe for humans and dependable for up to 15 yrs. The challenge for designers, manufactures, test validation and technologies is to predict the dependability of the systems by adapting quality and reliability assessments and to qualify new products for known, unknown and changing uses. Failure-oriented acceleration testing; contemporary computational methods and field assessment can help respond to the challenge. Robustness testing, HALT/HASS potential enhancements are introduced for additional development. This presentation shows how adapted methods can be used to qualify safe and dependable products for their expected use while presenting methods to account for unexpected use.
- **Keywords:**
  - thermal mechanical simulation, reliability models, thermal cycling, shock/vibration and application use conditions

Outline

- **Motivation and Introduction**
- **Demand – drivers for quality and reliability**
- **Use environments**
- **Failure Oriented Accelerated Testing**
- **Physics of Failure models**
- **Statistical models and implications**
- **Highly Accelerated Life Tests and Highly Accelerated Stress Screens**
- **Summary**

Motivation – a simplified model

- **Electronic devices are ubiquitous and enhance our lives**
  - Access devices are short lived – mobile phones, tablets, gaming
  - Productivity devices have medium life – design devices, business computers, workstations, data centers
  - Infrastructure and safe devices are long lived – networks, manufacturing systems

- **Devices are connected**
  - Access devices exploit capabilities / outputs of productivity and infrastructure devices – at low cost
  - Productivity devices create/optimize content and use other connected device capabilities – med. cost
  - Infrastructure devices preserve connectivity and capabilities at a higher cost
    - Safe devices preserve lives and safety at higher cost

- **New technologies and devices are expensive and come with risk or challenges**
  - New evaluation protocols are required to introduce capable and dependable products
  - Existing testing can be adapted for efficacy in improving dependability

Introduction

- **Dependability is most important for shared use and safety (at reasonable cost)**
  - Compute/networking availability impacts many people with potential for lost time/opportunity
  - Safety and health considerations are the highest priority
  - Contemporary components highly integrate functionality (SOC qual. includes dependability)
- **Reliability must be designed into components and systems apriori**
  - Knowledge of end use must be considered at design / technology research stage
  - Design for quality and reliability must be informed by physics of failure / FMEA
- **Quality and reliability estimates are validated upon qualification**
  - Use test to failure or failure oriented accelerated testing
  - Margin and operating limits must be known at qualification

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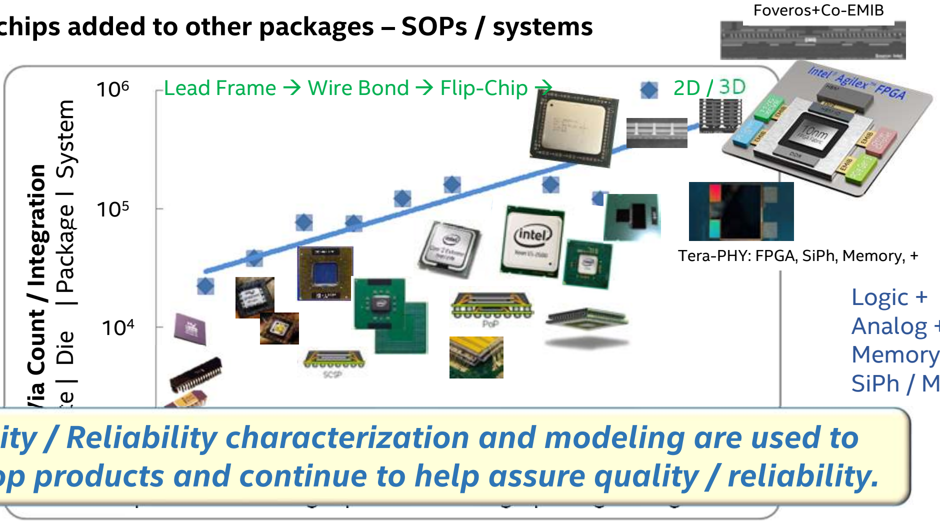
Heterogeneous Products Integrate Many Functions and Types of Devices

- **Devices integrated into the chip – add functionality – SOC**
- **Chips integrated into a package – add functions & improve performance – SOP or *module***
- **Packages with chips added to other packages – SOPs / systems**

Logic or
Analog or
Memory



Logic +
Analog +
Memory +
SiPh / MEMs

Quality / Reliability characterization and modeling are used to develop products and continue to help assure quality / reliability.

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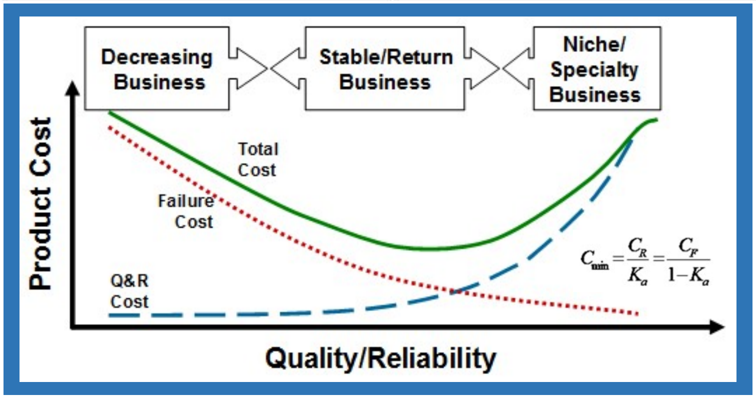
Demand: Balance of Long-Term Product Cost with Q/R

Appliance – adequate performance, low cost, 3yrs.	**Productivity** – good performance, reasonable cost, 5-7 yrs.	**Infrastructure** – critical performance, higher cost, 5-10-15 yrs.



High Q&R expectation @ higher costs High Quality/Reliability, 100 dpm/0.1%-Safe/High Dependability

Balanced Q&R expectation @ target cost 500 dpm/1% based on knowledge of use, market expectations

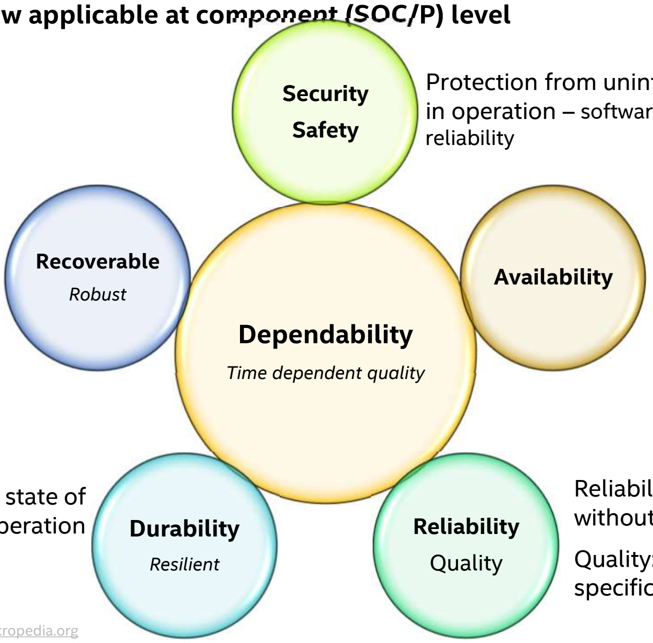
Moderate Q&R & low cost based on knowledge of limited use conditions, segment market expectations, hi-dpm

Product quality and reliability is targeted to customer expectations

"Package Reliability – Professional Development Course", A. Lucero et al, IEEE - ECTC 2010
"Probabalistic Design for Reliability-PDfR in Electronics & Photonics" E. Suhir, Delft Inst. Tech., 2014

Demand: dependability — to perform as and when required

- system construct now applicable at component (SOC/P) level



Security
Safety

Protection from unintended deviation in operation – software, tampering, reliability

Recoverable
Robust

Ability to recover from a failure or event

Dependability
Time dependent quality

Availability

Available to be in a state to perform to specification

Durability
Resilient

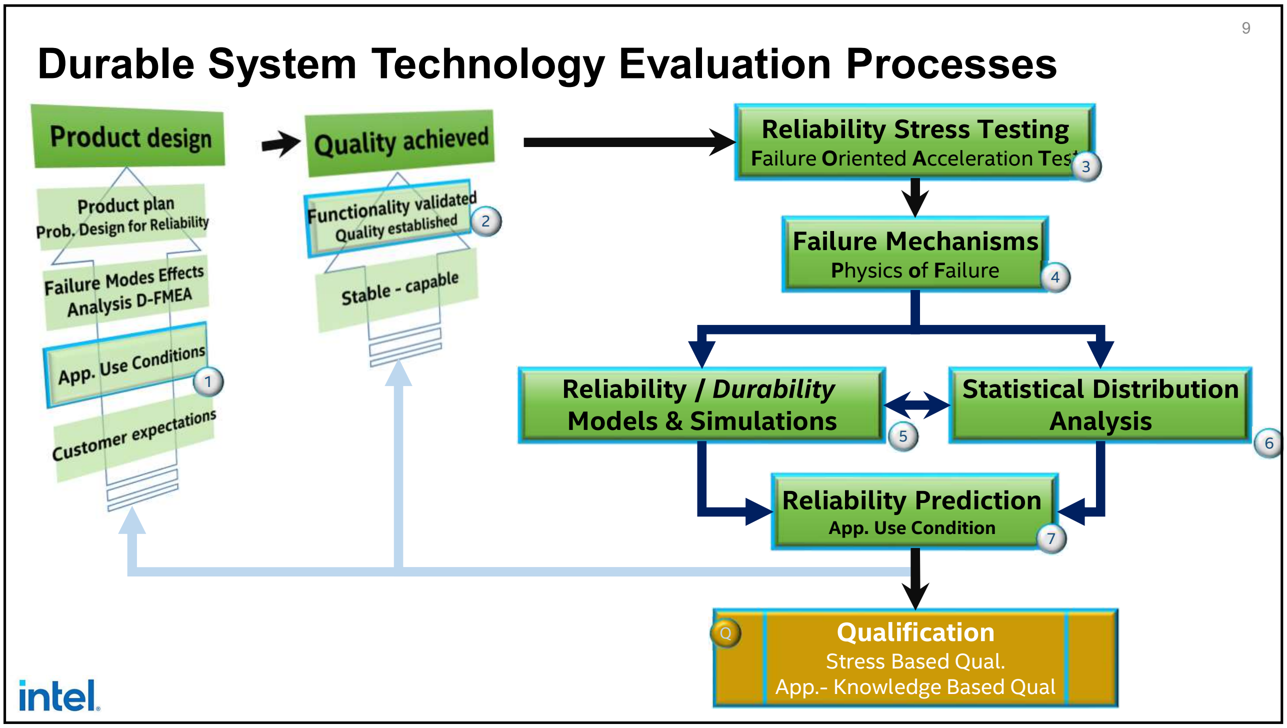
Maintainable to a state of operation

Reliability
Quality

Reliability: meet specification without fail for expected life

Quality: achieve specification at delivery

Adapted:
IEC Electropedia, https://electropedia.org
A. Aal, VW, CATRENE, resilient integrated systems principles, DKE-VDE, & TRACE, 2015



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Durable System Technology Evaluation Processes

Product design

Product plan
Prob. Design for Reliability

Failure Modes Effects Analysis D-FMEA

App. Use Conditions ①

Customer expectations

Quality achieved

Functionality validated
Quality established ②

Stable - capable

Reliability Stress Testing
Failure Oriented Acceleration Test ③

Failure Mechanisms
Physics of Failure ④

Reliability / *Durability* Models & Simulations ⑤

Statistical Distribution Analysis ⑥

Reliability Prediction
App. Use Condition ⑦

Ⓠ **Qualification**
Stress Based Qual.
App.- Knowledge Based Qual

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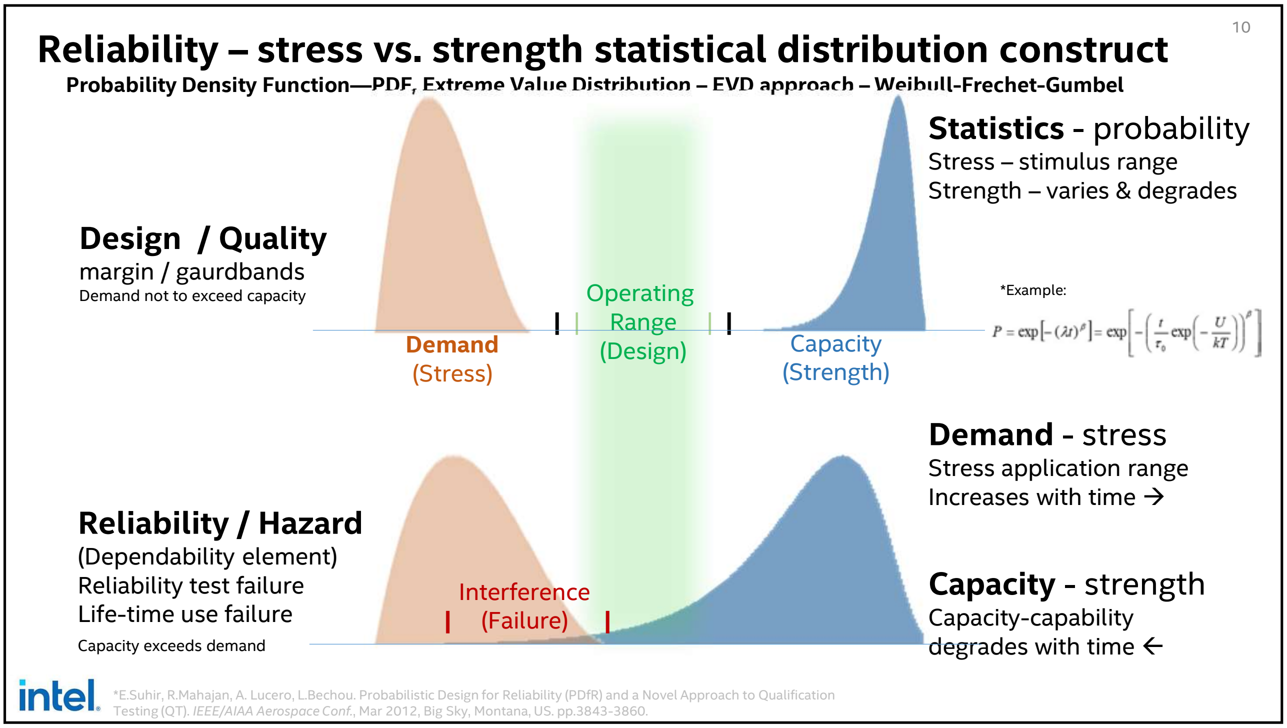

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Reliability – stress vs. strength statistical distribution construct

Probability Density Function—PDF, Extreme Value Distribution – EVD approach – Weibull-Frechet-Gumbel

Design / Quality
margin / gaurdbands
Demand not to exceed capacity

Statistics - probability
Stress – stimulus range
Strength – varies & degrades

*Example:

$$P = \exp\left[-(\lambda t)^{\beta}\right] = \exp\left[-\left(\frac{t}{\tau_0}\exp\left(-\frac{U}{kT}\right)\right)^{\beta}\right]$$

Reliability / Hazard
(Dependability element)
Reliability test failure
Life-time use failure
Capacity exceeds demand

Demand - stress
Stress application range
Increases with time →

Capacity - strength
Capacity-capability
degrades with time ←

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*E.Suhir, R.Mahajan, A. Lucero, L.Bechou. Probabilistic Design for Reliability (PDfR) and a Novel Approach to Qualification Testing (QT). *IEEE/AIAA Aerospace Conf.*, Mar 2012, Big Sky, Montana, US. pp.3843-3860.

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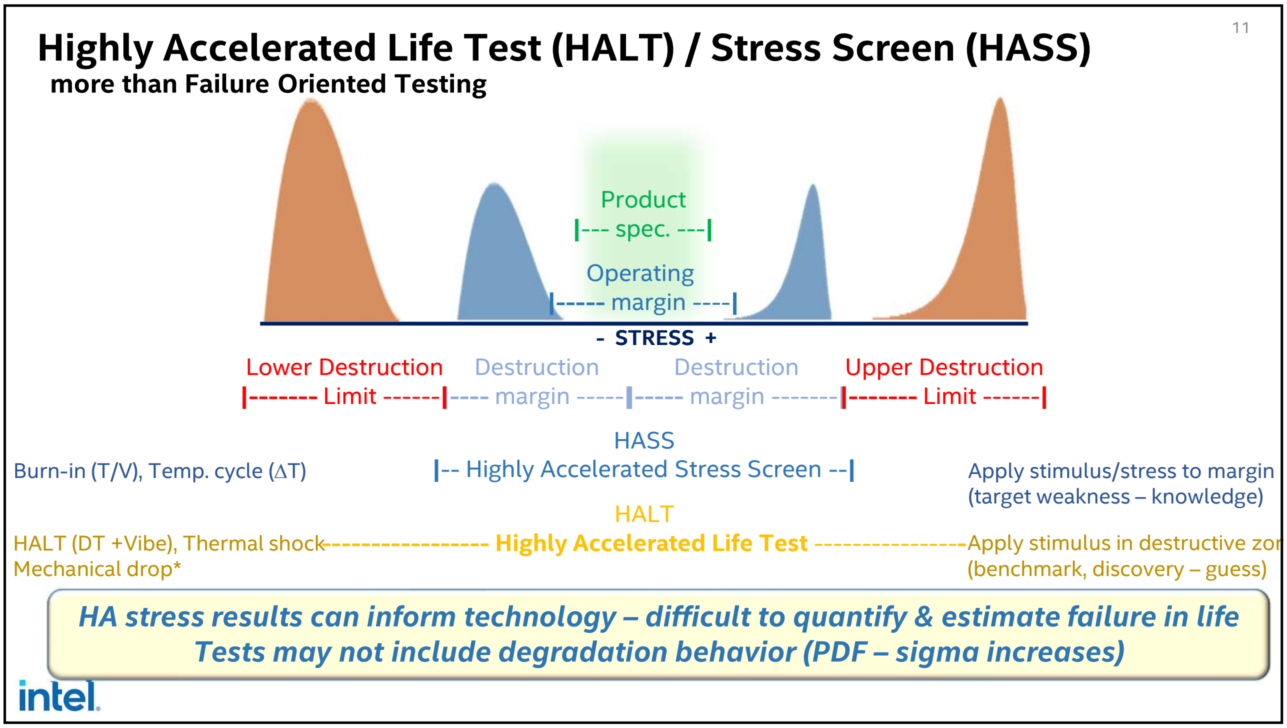

Highly Accelerated Life Test (HALT) / Stress Screen (HASS)

more than Failure Oriented Testing

Lower Destruction |------- Limit ------|

Destruction |---- margin -----|

Destruction |----- margin -------|

Upper Destruction |------- Limit ------|

HASS

Burn-in (T/V), Temp. cycle (ΔT) |-- Highly Accelerated Stress Screen --| Apply stimulus/stress to margin (target weakness – knowledge)

HALT

HALT (DT +Vibe), Thermal shock<----------------- **Highly Accelerated Life Test** ----------------->Apply stimulus in destructive zor

Mechanical drop* (benchmark, discovery – guess)

HA stress results can inform technology – difficult to quantify & estimate failure in life
Tests may not include degradation behavior (PDF – sigma increases)

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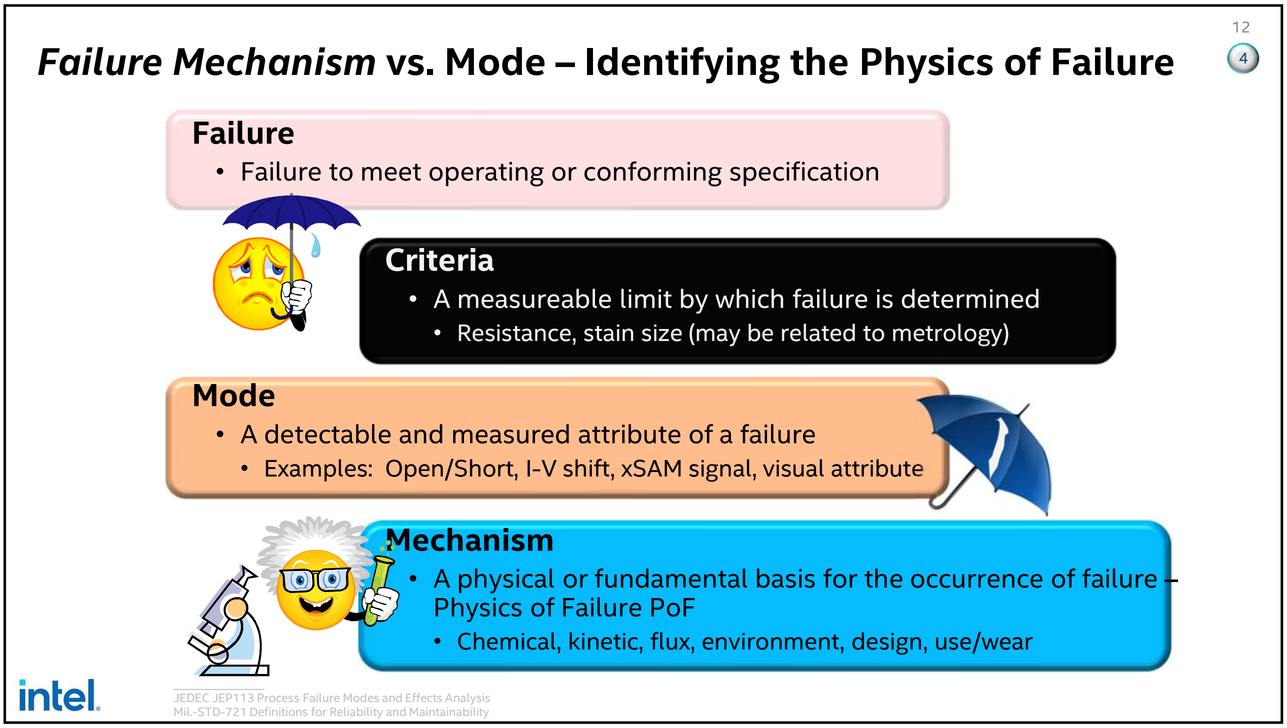

Failure Mechanism vs. Mode – Identifying the Physics of Failure

④

Failure
- Failure to meet operating or conforming specification

Criteria
- A measureable limit by which failure is determined
  - Resistance, stain size (may be related to metrology)

Mode
- A detectable and measured attribute of a failure
  - Examples: Open/Short, I-V shift, xSAM signal, visual attribute

Mechanism
- A physical or fundamental basis for the occurrence of failure – Physics of Failure PoF
  - Chemical, kinetic, flux, environment, design, use/wear

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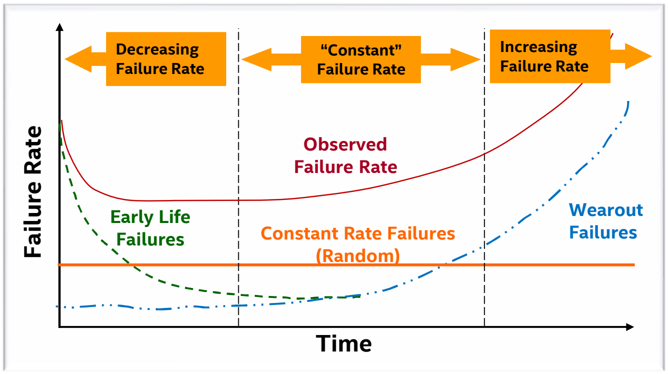
JEDEC JEP113 Process Failure Modes and Effects Analysis
MIL-STD-721 Definitions for Reliability and Maintainability

Quality & Reliability "Bathtub" Curve



Failure rate is the frequency with which a device fails, expressed in failures per hour or cycle.

CHALLENGE

Create reliability tests & models to mimic or early fails & accelerate life

- Failure Oriented Accelerated Tests (FOAT)
- Physics of Failure & models (PoF)

QUALITY:

- Defects, early fails or non-conformance to standard – early life
  - Decreasing failure rate
  - Quality marginality results in latent reliability fails

RELIABILITY:

- Intrinsic, wearout / extended use failure following material / physical behavior
- Fails to perform to intended function over time
  - Increasing failure rate.

RANDOM EVENTS:

- Failure due to "random" event or "unforeseen" event – NOT accelerated
  - Constant failure rate / probability

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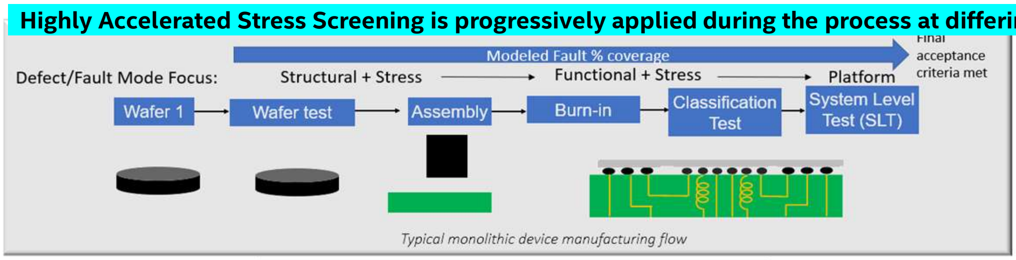
"Package Reliability – Professional Development Course", A. Lucero et al, IEEE - ECTC 2010

Quality / Reliability and the Role of "Test"

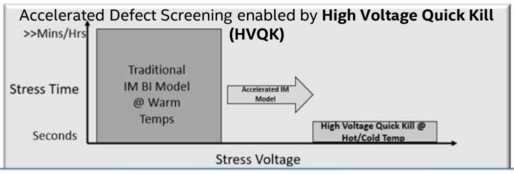
- **"Test" is the scheme by which all devices are screened for quality and performance assurance.**
- **Coverage is defect-based detection and screening.**
  - Derived from known and modeled structural or functional device fault modes → Highly Accelerated Stress Screen (HASS)

Highly Accelerated Stress Screening is progressively applied during the process at differing levels.



Typical monolithic device manufacturing flow

Accelerated Defect Screening enabled by **High Voltage Quick Kill (HVQK)**



This methodology will play a key role in enabling cost competitive future package architectures.

Traditional Package architectures allow flexible stress conditions across multiple sockets, but the methodology needs to be robust to meet demands of future package architectures.

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Quality / Reliability → Technology Environment Changes

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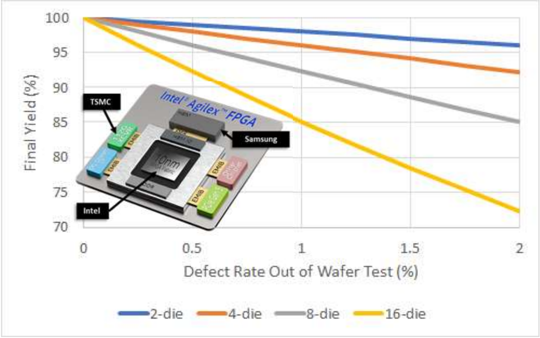
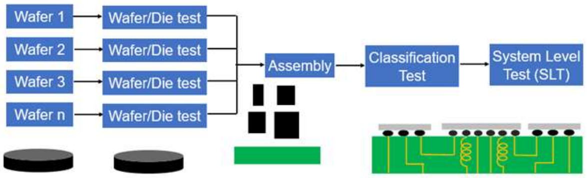
Shift to heterogenous packaging drives the need for Known Good Die – to lower product yield risk



Typical Heterogenous Manufacturing Flow



Typical 2D/2.5D manufacturing flow

Heterogenous Test Flow

Move content to enable KGD

Wafer/Die Level → *Package Level*

Structural Defect / ***Functional Testing*** **/ Hot HVQK** → Burn-In and Functional Testing → Platform based Validation

← Move Coverage to Die Level

Concept of accelerated defect screening other test methods still apply but requires implementation in a new test environment under different conditions.

Known good die (KGD) are critical to making die disaggregation and heterogenous integration work → Drives Test Challenges

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Reliability test challenge: mimic failures in time during life

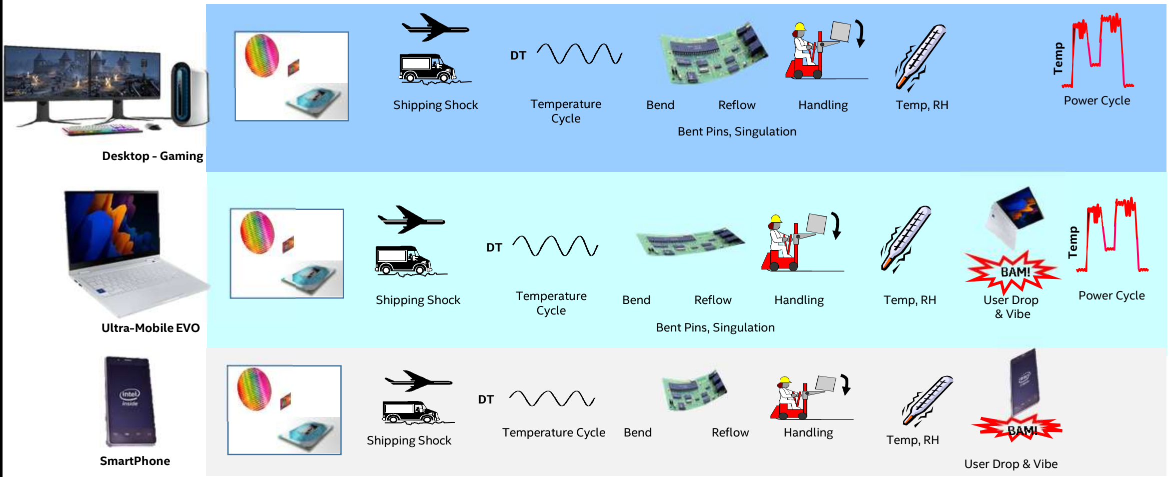
③

Life Test	Accelerated Life Test	Highly Accelerated Stress/Life Test
A life test simulates a use condition **without acceleration**	**Accelerates** a given physical mechanism **without inducing any artifacts** or new failure mechanisms not representative of the use environment.	Benchmark test to that accelerates failure by **increasing the stress beyond the capability-strength** to identify failures
Typically **time scale compression** at the use condition. Used when an accelerated test does not adequately simulate the actual use environment.	An accelerated test is a reliability test where one or more **conditions/stimuli (e.g., temperature, voltage, etc.) are increased** to reduce times to failure to a manageable time frame.	Highly accelerated test where one or more **conditions/stimuli exceed strength / capability** to create and identify failure modes, assess marginality and trends. Creates failures in a very short time.
Examples: Power Cycling (PC, duty - thermal cycling) Drop, a cell phone on concrete) Vibration (shipping via rail) Preconditioning (store/ship & SMT)	**Examples:** Temperature cycle (TC), Bake (HTSL) Highly accelerated stress test (HAST) Electromigration (EM) Time Dep. Dielectric Breakdown (TDDB)	**Examples:** Highly Accelerated Life Tests (**HALT**, TC+Vibe), Shock (dynamic pulse) Highly Accelerated Stress Test (**HSS**, ELT, Burn-in)
Challenge: Test time is very long **Advantage:** Fail time distribution and AF undisputable	**Challenge:** Prevent test artifacts & deconvolute stimuli **Advantage:** Reasonable time to fail & Fail time distribution	**Challenge:** Strength and stress unknown (most often), failure data of limited use to solve issues or provide true, scaleable comparisons. **Advantage:** Fast time to fail and uncovers failures

Accelerated Tests (AT) ≠ Life test
Accelerated Tests ∝ Life test

Market Segment Dependent Use Conditions

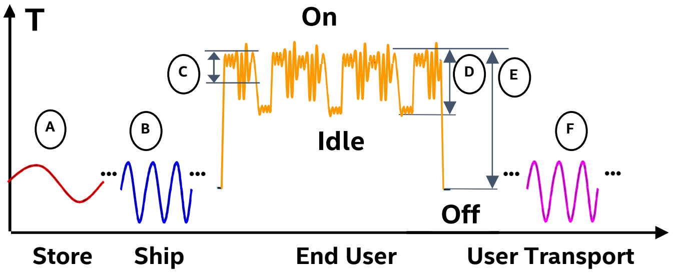
Assembly → Shipping → Storage → OEM/ODM Assembly → End-user environment



These can get quite complicated !

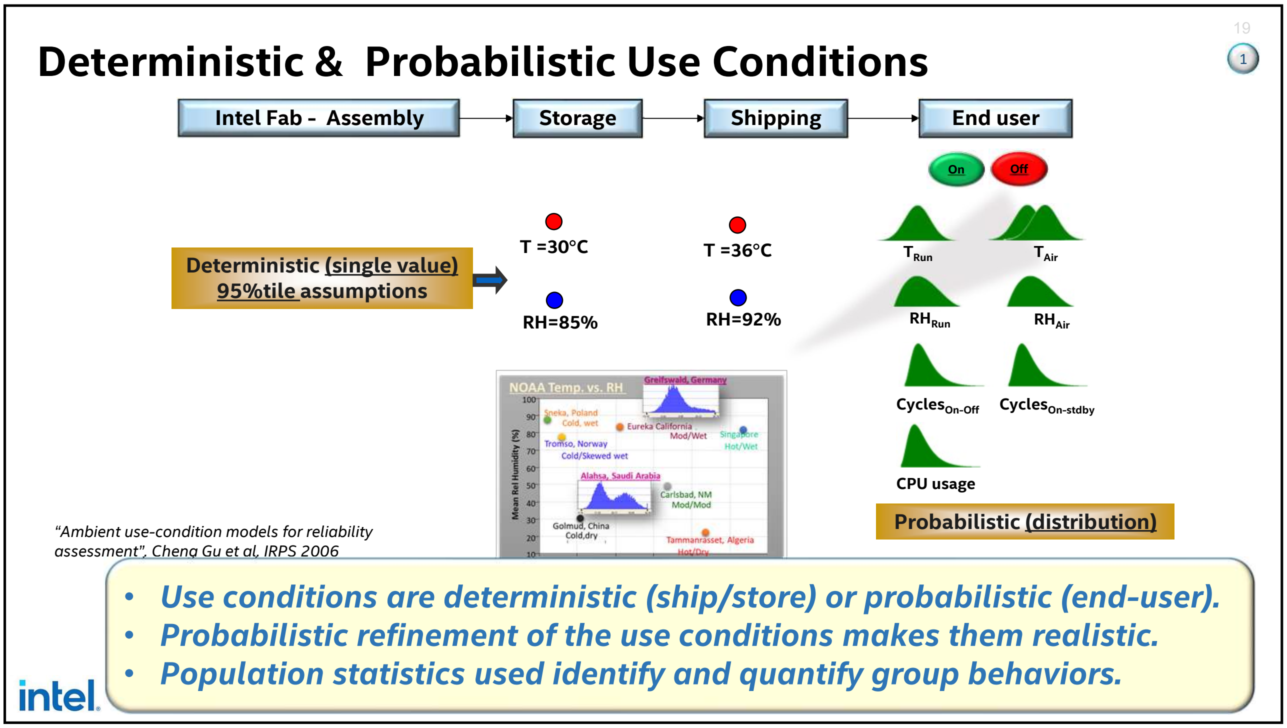
Temperature UC: Thermal Events History

- **Temperature changes caused by:**



	Usage	Evolution
A, B	Shipping, storage	Relatively stable once studied
C, D, E	End user use variations & power cycles	Evolves with products / apps.
F	User transport	Stable in usage segment
--	Ambient environment change	Represented by climate data

Continuing work needed for faster evolving elements



Deterministic & Probabilistic Use Conditions

Intel Fab - Assembly → **Storage** → **Shipping** → **End user**

Deterministic (single value) 95%tile assumptions

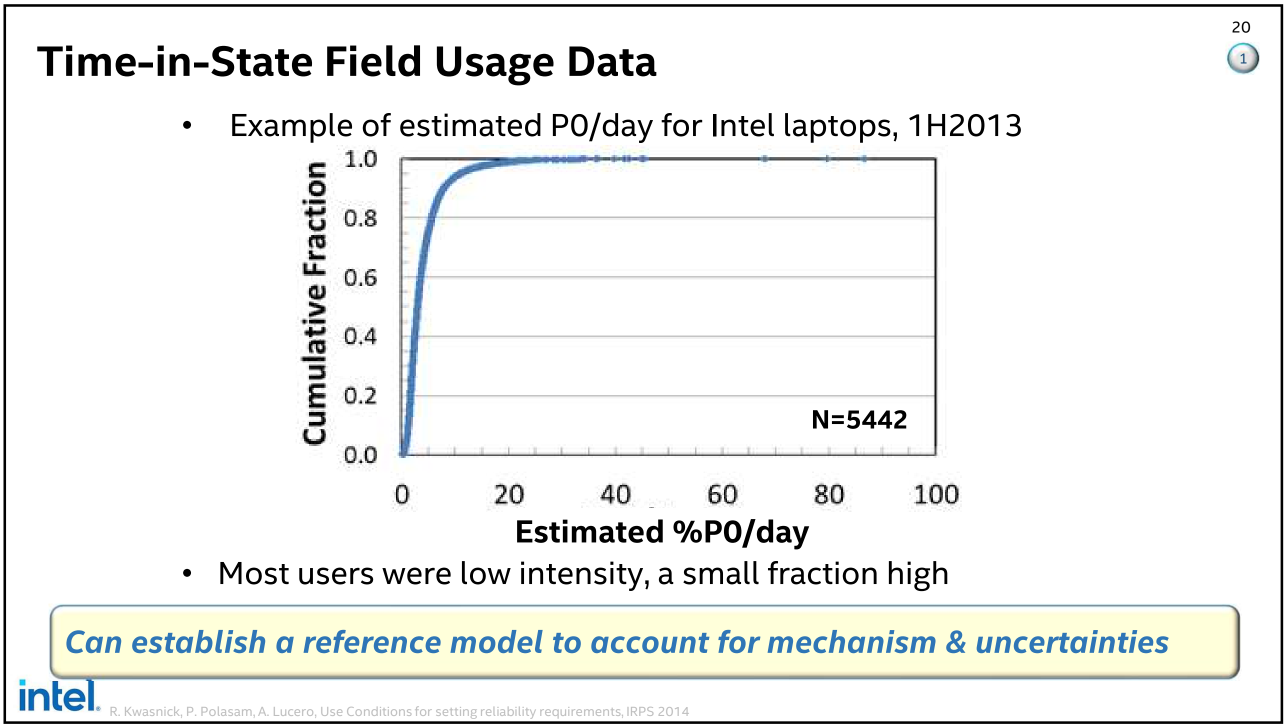
Storage: T =30°C, RH=85%

Shipping: T =36°C, RH=92%

Probabilistic (distribution)

"Ambient use-condition models for reliability assessment", Cheng Gu et al, IRPS 2006

- *Use conditions are deterministic (ship/store) or probabilistic (end-user).*
- *Probabilistic refinement of the use conditions makes them realistic.*
- *Population statistics used identify and quantify group behaviors.*



Time-in-State Field Usage Data

- Example of estimated P0/day for Intel laptops, 1H2013

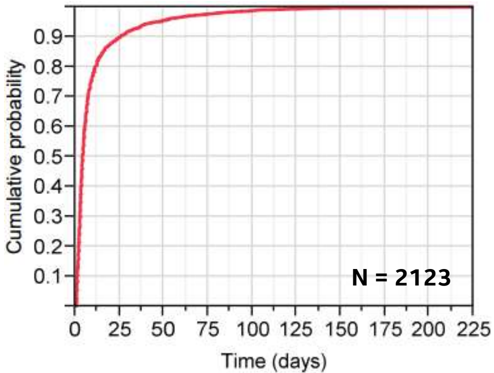
- Most users were low intensity, a small fraction high

Can establish a reference model to account for mechanism & uncertainties

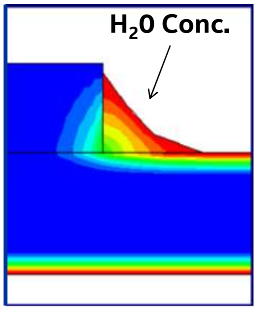
R. Kwasnick, P. Polasam, A. Lucero, Use Conditions for setting reliability requirements, IRPS 2014

Off-time and Humidity Exposure

- Longest off or stand-by time is UC driver of failure due to H_2O diffusion/effusion, e.g., corrosion and delamination
- Risk is highest for long duration events



Longest notebook non-on time over 1 y



x-section of simulation, 100 h off-time

Can guide realistic HAST condition and duration

S Rangaraj, D Kwon, M Pei, J Hicks, G Leatherman, A Lucero, T Wilson, , IRPS 2013

Qualification Requirements –
Use Condition and Rel. Estimation Model Considerations

Q&R Goal Setting: customer demand, use and capability

- **To set goals balance:**

Consideration	Question
Customer requirements	What does the customer want?
Competitive pressure	What do competitors target?
Engineering **capabilities**	Can you achieve the goal?
Engineering **costs**	What's the cost of achieving goal?

- **Other insights:**
  - Goals are market segment specific (automotive, phone…) – drive process/material development
  - Products in same market may have the same goal
  - Goals are a business or mission-specific decision

Qualification: Stress-Based Qual. vs. Knowledge-Based Qua

PRODUCT DEV. PLAN	FMEA	DESIGN	DEVELOPMENT	TESTING CHARACTERIZE	IMPROVE	CERTIFY TECHNOLOGY	PRODUCT QUAL	SYSTEM QUAL
STRESS BASED QUALIFICATION			**Assumed use, environment, duty cycling, software, models, validity of tests (fr. history & tables)**					
Customer requirement	Heuristics	Use EDA kit Estimate Q&R durability from models/history	Foundry report	Test prod. design	Test-Fail-Improve	Foundry, OSAT report	Stress based Quality & reliability – test to pass	Stress based
KNOWLEDGE APPLICATION QUALIFICATION			Defined use case, environment, duty cycling, software, failure-oriented testing, physics of fail models (FOAT, POF, Knowledge Based Qual. KBQ/App. Specific Qual.)					
Customer functionality, use, environ.	Physics POF model Heuristics	Use EDA kit Estimate Q&R, durability from POF model	Validate physics of failure models	Failure oriented tests to failure statistics	Tech./model refinement, validate	Design rules validated; performance model valid, UC KBQ Report	Test to target define by use environment to stat. confidence Test to pass	Test to target define by use environment to stat. confidence Test to pass

Stress Based Qual. – benchmark: assumed/measured use, model, & requirement
Knowledge Based Qual.: use documented, POF models, FOAT limits established

Failure Mechanisms and Stimuli

MFG	OEM	User[1]	Mechanism	Cause	Stimuli[2]
			Process Charging	Process-induced EOS	V
		Const	Electrical Overstress	ESD and Latchup	V, I
		IM	Infant Mortality	Extrinsic Defects	V, T
		IM	Logic Failure	Test Coverage	n/a
		WO	Hot Carrier	e^- Impact ionization	V, I
		WO	Neg. Bias-T Instability	Gate dielectric damage	V, T
		WO	Electromigration	Atoms move by e- wind	I, T
		WO	Time-Dep Diel. B'down	Gate dielectric leakage	V, T
		WO	Stress Migration	Metal diffusion, voiding	T
		WO	Interlayer Cracking	Interlayer stress	DT
		WO	Solder Joint Cracking	Atoms move w/ stress	DT
		WO	Corrosion	Electrochemical reaction	V, T, RH
		Const	Soft Error	n & α e^-h pair creation	radiation

Use Conditions (V, T…) cause specific failure mechanisms

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1. Const = Constant, IM = Infant Mortality, WO = Wearout
2. V = Voltage, I = Current, T = Temperature, ΔT = Temp cycle, RH = Relative Humidity

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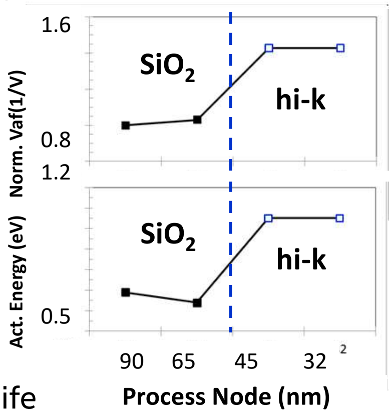
Impact of Technology Evolution of Requirements: HTOL

- **JESD-47I, specifies 1000 h with 0 fails/231 units**

Example Assessment	Typ. Conditions
High Temp. Operating Life (HTOL)	1.1-1.2 x Vnom 125°C

- **Issues:**
  - High-k, Hf gate accel. factors are higher* (Ea & Vaf) →
    - 1000 hrs. could be >> intended use life
    - Std allows adjustments, but some customers may be cautious
  - Some products have varying V states**, e.g., to save power, so more difficult to determine stress time ≡ use life



- ***Stress-based qualification without FOAT gives inadequate reliability assessment of new technologies***
- ***Significant example of the impact of scaling – new technology-material***

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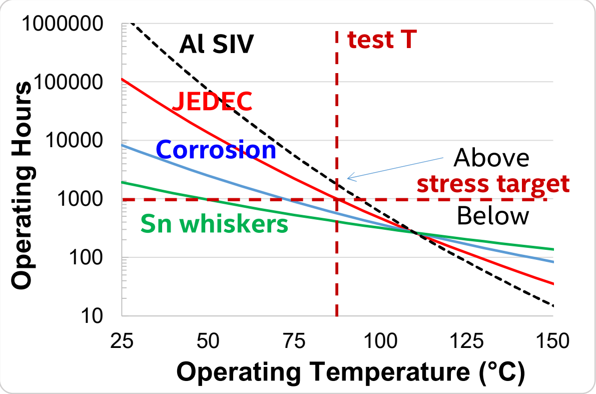
* Kwasnick et al., IRPS 2012, ** Kwasnick et al., IRPS 2011

Examination: THB Stress Hr. – Fail Oriented Accel. Test Level / Time

- **THB (Temp Humidity Bias, JESD47)**
  - AF: Arrhenius
  - Targets Ea=0.7 eV
    - Surface metal migration
  - Tuse= 85°C
  - 1000 h represent 7-10 y
- **Issue**
  - If Ea < 0.7 eV, then
    - under-stressed at 1000 h
- **Under-stressed mech.**
  - Corrosion (Ea = 0.4 eV)
  - Sn whisker (Ea = 0.23 eV)
- **Over-stressed mech.**
  - Al stress-induced voids (Ea = 1 eV)

Relative Acceleration

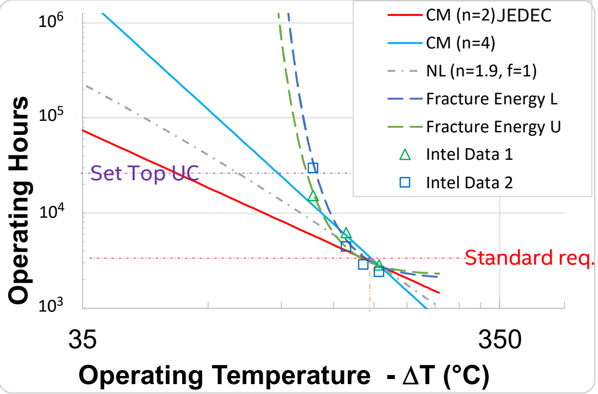


See JEDEC JEP 122

- **Stress based qualification without FOAT gives inadequate reliability assessment of new technologies**
- **Knowledge based qualification suited to uncover issues not exposed by std, e.g., if low Ea**

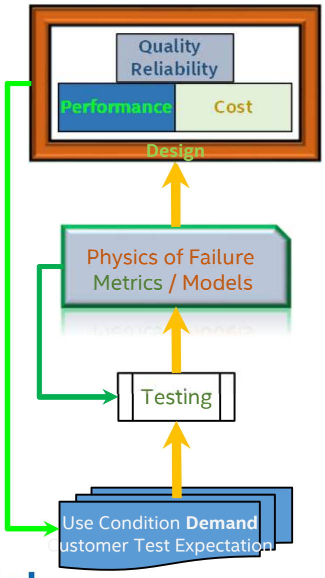
Examination: Temp. Cycle Count Requirement – Physics Of Fail model

- **Temperature Cycle:**
  - Requirement from: Coffin-Manson, N=2
  - T_{use}=85°C
  - $Time_{use}$=7-10 yrs.
- **Limitations**
  - AF: non-power law: Critical stress-strain-crack energy
  - SetTop use >> standard (meets standard, fails life)
- **Optimizations lost**
  - Geometry "simplified out"; results in testing of all package form-factors to the wrong requirement.
  - BGA corner glue for shock protection fails TC requirement-passes in use
  - Preconditioning missed –added to standard c. 1996



- ***Stress based qualification without FOAT gives inadequate reliability assessment of new technologies***
- ***Over/under test due to simplified AFs – cost/risk passed to customers***
- ***Design to meet standards eliminates viable technology options that will not fail during use***

Probabilistic Design for Reliability & Rel. Test to Fail (FOAT) ⑤



- **Use Condition & Goals - Demand**
  - Benchmarks – design practices or standards
  - Generational – design re-use
  - Use Condition – Customer Expectation → measured
- **Failure Oriented Accelerated Test (FOAT) with Failure Metrics**
  - Measured / computed values represent physical failure – capability
  - Computed: stress – critical at failure location; E-field; Flux
  - Measured: strain – at / near fail location; I-V shift, V_T / I_{Dsat} shift
- **Models – equations & tools translate between test & use**
  - Predict response in use or in test – reliability estimation
  - Predictive metrics at each level of integration / test
- **Design – optimizations to achieve customer needs - Demand**
- **Feedback drives improvement**
  - Metrics – Models improve tests and data
  - Optimized designs – feed use condition and expectations

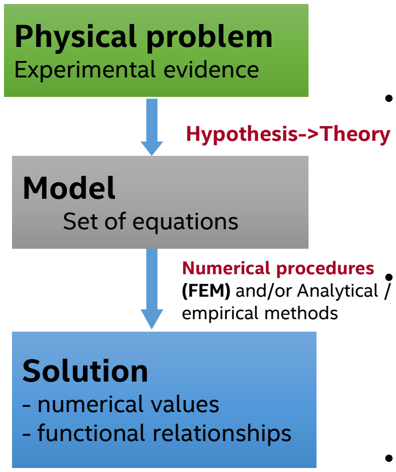
Physics of Failure Reliability Metrics: generalizable

- **Metrics are based on physics of failure / characterization**
- **Metric correlates test to use condition demand**
- **Common metric is actionable: drives design, testing & quantifies demand**
  - Common currency for trade – off decisions

FAILURE RISK	RELIABILITY TEST METRIC	MECHANISM	USE CONDITION	PoF KBQ METRIC (computed)
Brittle cracks	Cycles: Temp. cycle	Crack initiation – exceed critical strength, energy	$T_{on/off/standby/turbo}$, $T_{Spatial/Transient-mass}$	$G_{critical-crack\ energy\ release}$
Fatigue creep	Cycles: Temp.cycle (isothermal)	Dislocation evolution w/i solid-state reaction	time, $T_{on/off/standby/turbo}$, $T_{Spatial/Transient}$	Accumulated Fatigue-Creep damage
Oxide breakdown	Time Dep.Dielectric Breakdown Temp.Bias Op. Life (TBOL/HTOL)	Oxide wearout in an electric field resulting in tunneling current through the gate dielectric	T_{on} (time), $V_{0\ on}$	I_g–V_d or freq. degradation
BGA crack – dynamic load	G & Num.drop/shocks on test board or system	Exceed critical strength ~ energy	Sys. Board / HS dyn. Load events	Strength: F or $\sigma_{critical}$ for N_{min}
Metal migration	Hrs.: ThB HAST	Moisture diffusion, Cath/Anod reduction	$T_{on/off}$ (time), $[C_{H2O}](t)$, V_0	Time, $[C_{H2O}]$, $\varepsilon_{potential}$

- ***Physics of failure, reliability metrics link testing, field use conditions & design***
- ***Common basis for decisions and trending are enabled with PoF metrics***

Model Formulation



Physical problem
Experimental evidence

Hypothesis->Theory

Model
Set of equations

Numerical procedures
(FEM) and/or Analytical / empirical methods

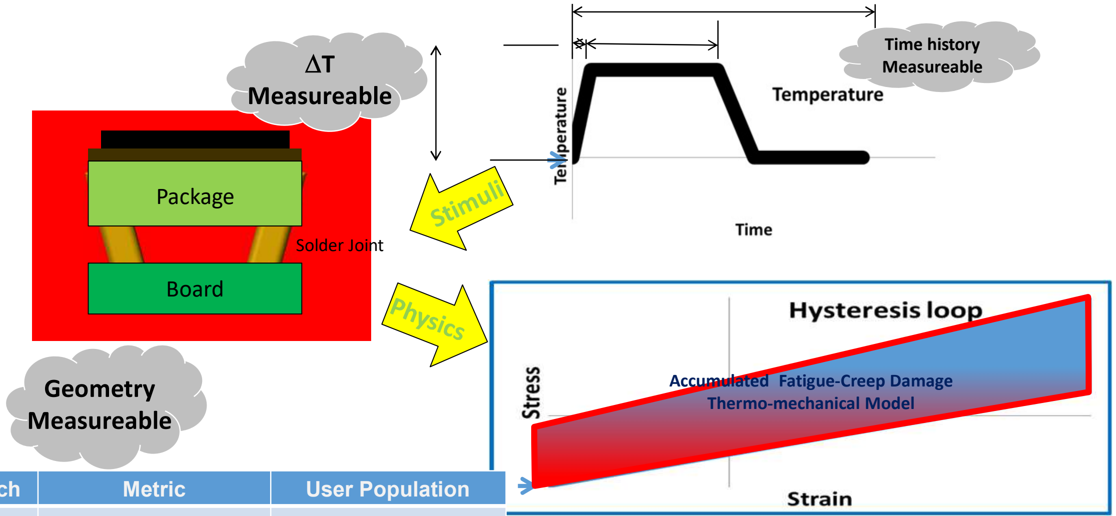
Solution
- numerical values
- functional relationships

- **Use failure analysis to identify the failure mechanism and physics of failure**
- **Develop or select a model based on the physics of failure**
  - Mechanistic models: diffusion, oxidation
  - Empirical models: characterized data fit by regression analysis to psuedo-physical relations
- **Models are represented by equations**
  - Finite Element or Numeric methods solve equations but may not dictate solutions
  - Statistical distribution model is extracted from empirical data and field data correlations
- **Models are best understood by evaluating the experimental evidence**

"All models are wrong, but some are useful" – George Box

Thermal Cycle / Power Cycle

Observations – Solder Joint Temperature Cycling



Approach	Metric	User Population
Previous	ΔT, cycle number	Representative user
Proposed	Accum. Fatigue-Creep	Field measured users

Strain, ε, measurable
Stress, σ, computed
Damage, computed-integral

---

⑤

Common Temp. Cycle Failure Models

- **Coffin Manson - Cyclic Failure: N = C($\varepsilon_{inelastic}$)^n**
  - $\varepsilon_{inelastic}$ is the inelastic strain in the material
  - Constant C is a *material property* known as fatigue coefficient
  - Constant n is a *material property* known as fatigue exponent
  - Fatigue "Law" – Empirical rule of thumb
  - Developed for cyclic stress in beams/load carrying elements
- **Adapted for Thermal Cycling for solders, etc.**
  - Substituting γ for $\varepsilon_{inelastic}$, N = C (γ)^n = C (L Δα ΔT / h)^n = K (ΔT)^n
    - L, Δα, and h are constant for a geometric configuration
    - K is a constant *dependent on a given geometric configuration*

$$AF_{CM} = \left(\frac{life_{use}}{life_{accel}}\right) = \left(\frac{\Delta T_{use}}{\Delta T_{accel}}\right)^{-n}$$

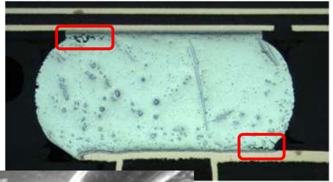
(a) Coffin-Manson for TC

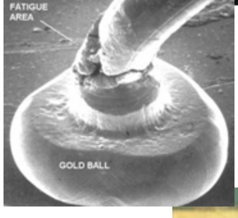
- **Acceleration Factor AF = N_1 / N_2 = (ΔT_1 / ΔT_2)^n**
  - AF allows us to scale performance between 2 different Temperature Cycling conditions *for a given geometric configuration*
    - It removes the package and board dependent constant K from the equation

$$AF = \frac{N_0}{N_s} = \left(\frac{f_0}{f_s}\right)^m \left(\frac{\Delta T_s}{\Delta T_o}\right)^n \left(e^{\frac{Ea}{K}\left(\frac{1}{T_{o\max}} - \frac{1}{T_{s\max}}\right)}\right)$$

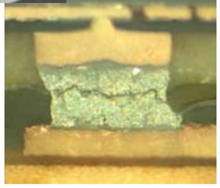
(b) Norris-Landzburg – adapted for freq. & creep

SLI Solder Fatigue



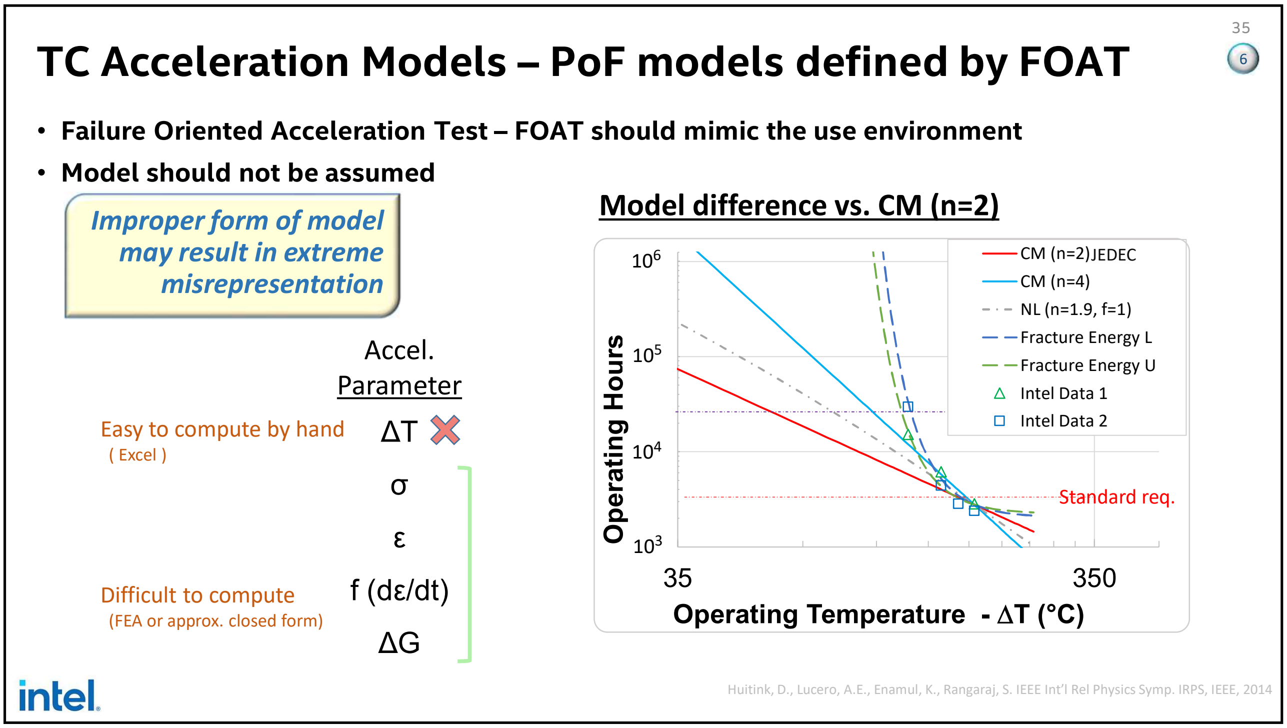


Wirebond fatigue



FLI Solder Crack

Wirebond Image Credit: Raytheon
https://www.reliabilityanalysislab.com/tl_hd_0401_RecognizingWireBondDamage.html



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6

TC Acceleration Models – PoF models defined by FOAT

- **Failure Oriented Acceleration Test – FOAT should mimic the use environment**
- **Model should not be assumed**

Improper form of model may result in extreme misrepresentation

	Accel. Parameter
Easy to compute by hand (Excel)	ΔT ✗
	σ
	ε
Difficult to compute (FEA or approx. closed form)	f (dε/dt)
	ΔG

Model difference vs. CM (n=2)

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Huitink, D., Lucero, A.E., Enamul, K., Rangaraj, S. IEEE Int'l Rel Physics Symp. IRPS, IEEE, 2014

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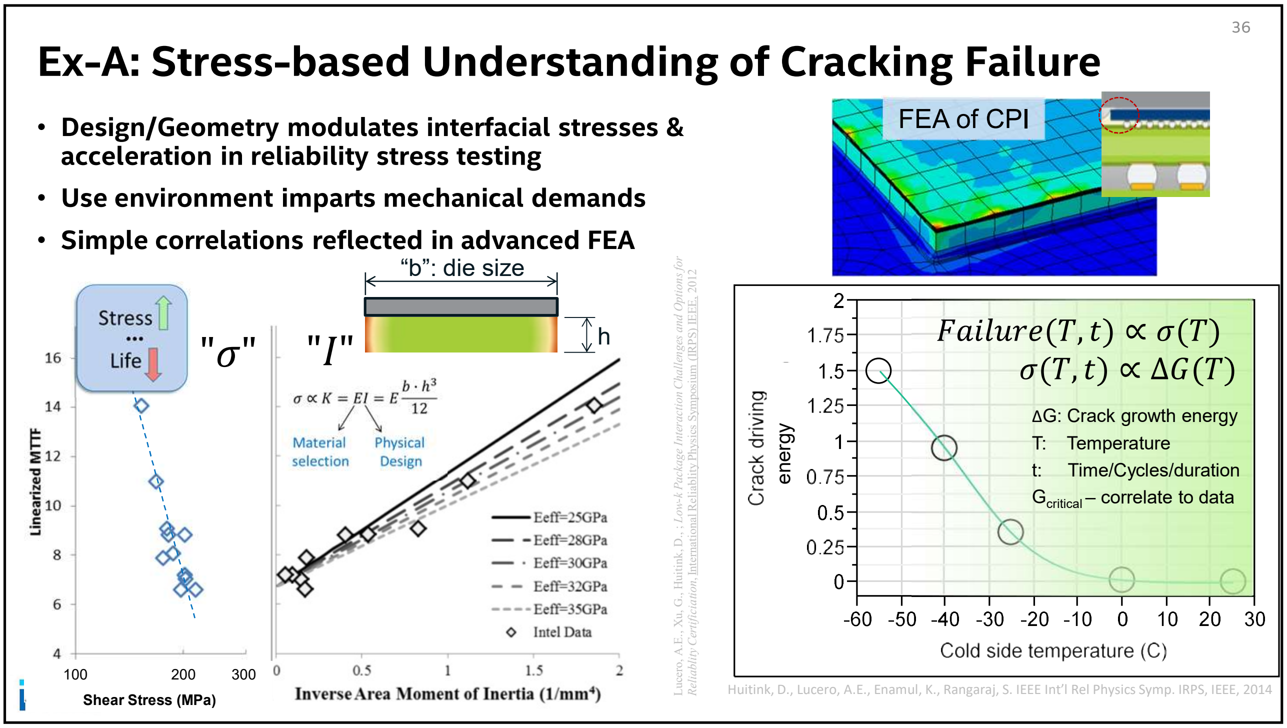

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Ex-A: Stress-based Understanding of Cracking Failure

- **Design/Geometry modulates interfacial stresses & acceleration in reliability stress testing**
- **Use environment imparts mechanical demands**
- **Simple correlations reflected in advanced FEA**

$$\sigma \propto K = EI = E\frac{b \cdot h^3}{12}$$

$$Failure(T,t) \propto \sigma(T)$$

$$\sigma(T,t) \propto \Delta G(T)$$

ΔG: Crack growth energy
T: Temperature
t: Time/Cycles/duration
$G_{critical}$ – correlate to data

Lucero, A.E., Xu, G., Huitink, D., ; *Low-k Package Interaction Challenges and Options for Reliablity Certificiation*, International Reliablity Physics Symposium (IRPS) IEEE, 2012

Huitink, D., Lucero, A.E., Enamul, K., Rangaraj, S. IEEE Int'l Rel Physics Symp. IRPS, IEEE, 2014

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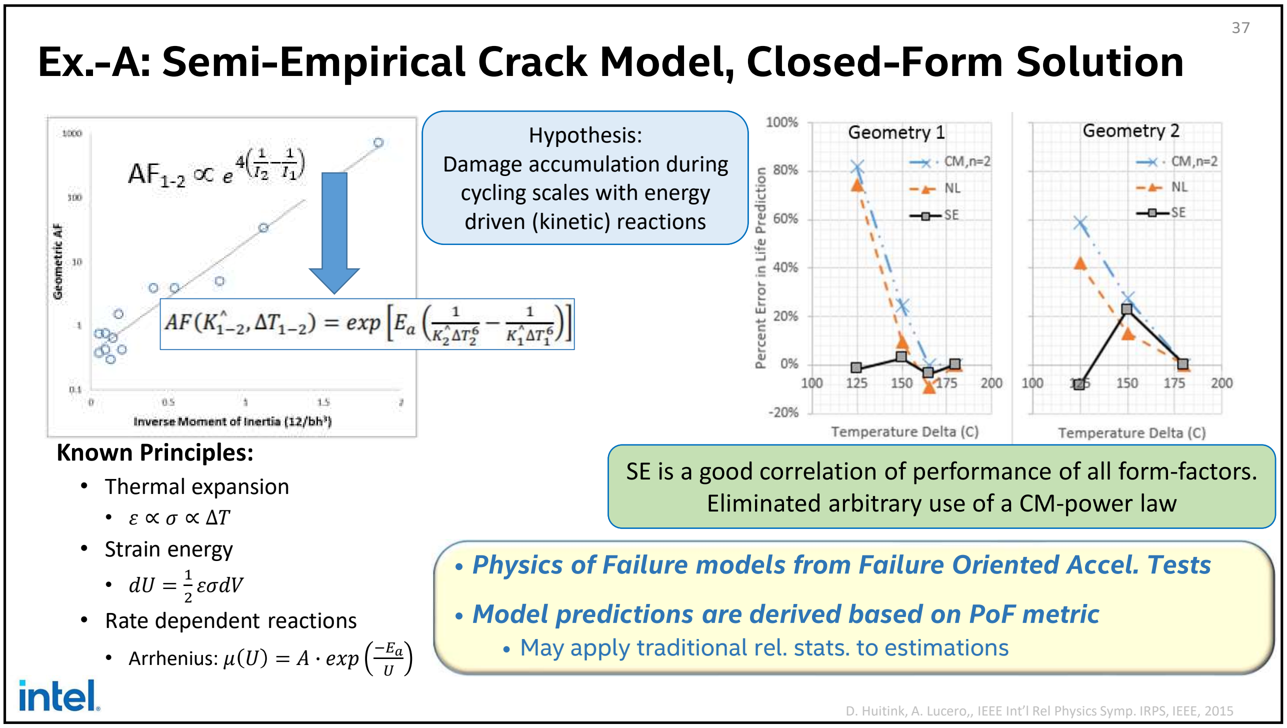


Ex.-A: Semi-Empirical Crack Model, Closed-Form Solution

$AF_{1\text{-}2} \propto e^{4\left(\frac{1}{I_2}-\frac{1}{I_1}\right)}$

$AF(\hat{K_{1-2}}, \Delta T_{1-2}) = exp\left[E_a\left(\frac{1}{\hat{K_2}\Delta T_2^6} - \frac{1}{\hat{K_1}\Delta T_1^6}\right)\right]$

Hypothesis:
Damage accumulation during cycling scales with energy driven (kinetic) reactions

SE is a good correlation of performance of all form-factors.
Eliminated arbitrary use of a CM-power law

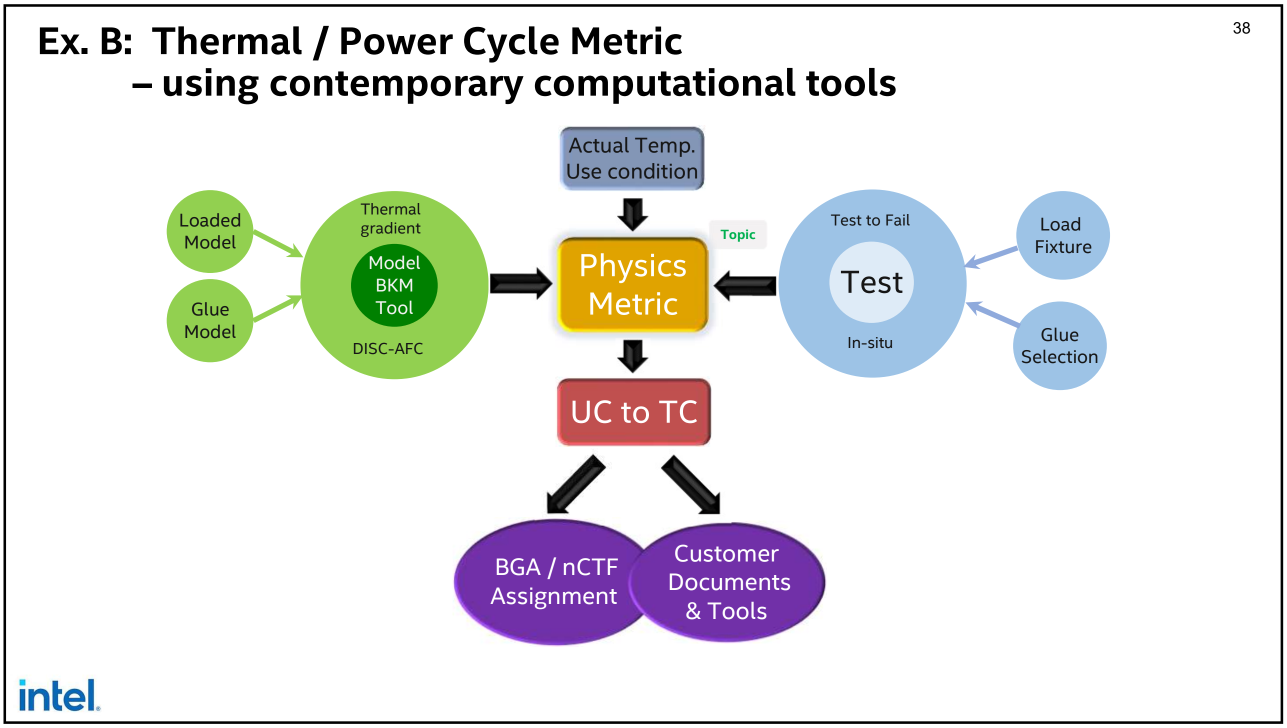
Known Principles:

- Thermal expansion
  - $\varepsilon \propto \sigma \propto \Delta T$
- Strain energy
  - $dU = \frac{1}{2}\varepsilon\sigma dV$
- Rate dependent reactions
  - Arrhenius: $\mu(U) = A \cdot exp\left(\frac{-E_a}{U}\right)$

- ***Physics of Failure models from Failure Oriented Accel. Tests***
- ***Model predictions are derived based on PoF metric***
  - May apply traditional rel. stats. to estimations

intel.

D. Huitink, A. Lucero,, IEEE Int'l Rel Physics Symp. IRPS, IEEE, 2015



Ex. B: Thermal / Power Cycle Metric
– using contemporary computational tools

Actual Temp.
Use condition

Loaded Model

Glue Model

Thermal gradient

Model BKM Tool

DISC-AFC

Topic

Physics Metric

Test to Fail

Test

In-situ

Load Fixture

Glue Selection

UC to TC

BGA / nCTF Assignment

Customer Documents & Tools

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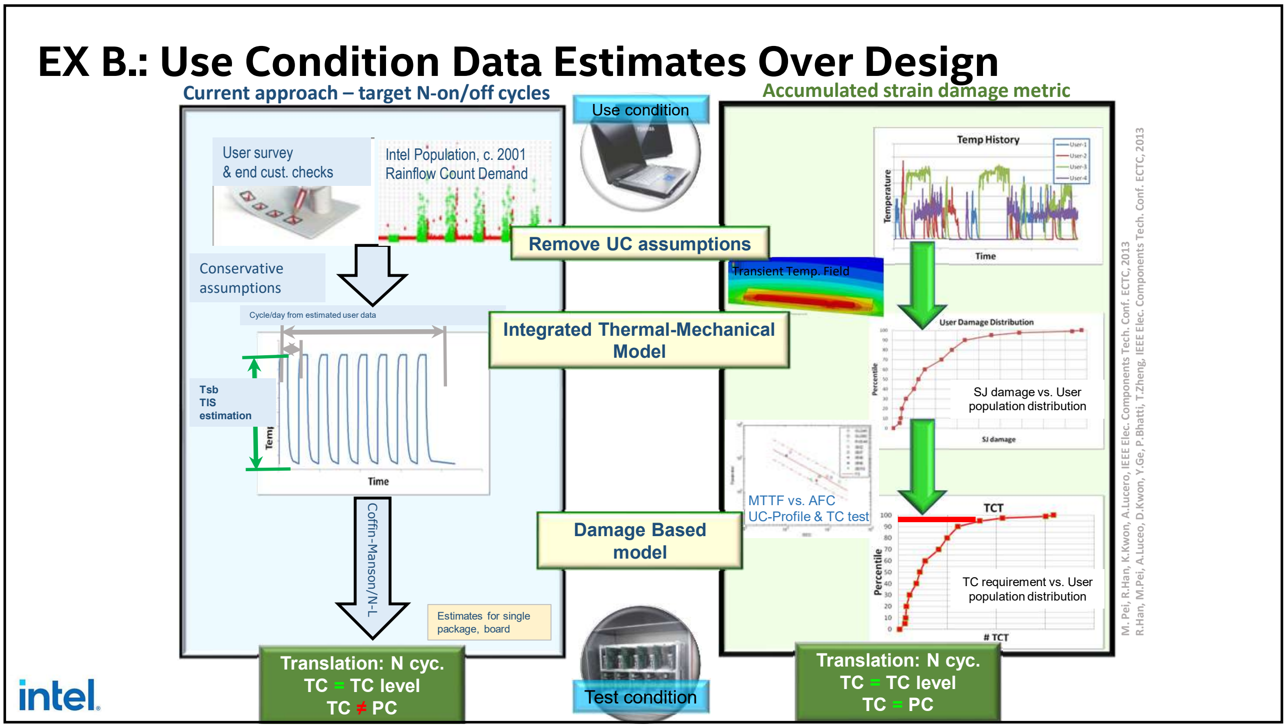


EX B.: Use Condition Data Estimates Over Design

Current approach – target N-on/off cycles

User survey
& end cust. checks

Intel Population, c. 2001
Rainflow Count Demand

Conservative assumptions

Cycle/day from estimated user data

Tsb
TIS
estimation

Coffin-Manson/N-L

Estimates for single package, board

Translation: N cyc.
TC = TC level
TC ≠ PC

Use condition

Remove UC assumptions

Integrated Thermal-Mechanical Model

Damage Based model

Test condition

Accumulated strain damage metric

Transient Temp. Field

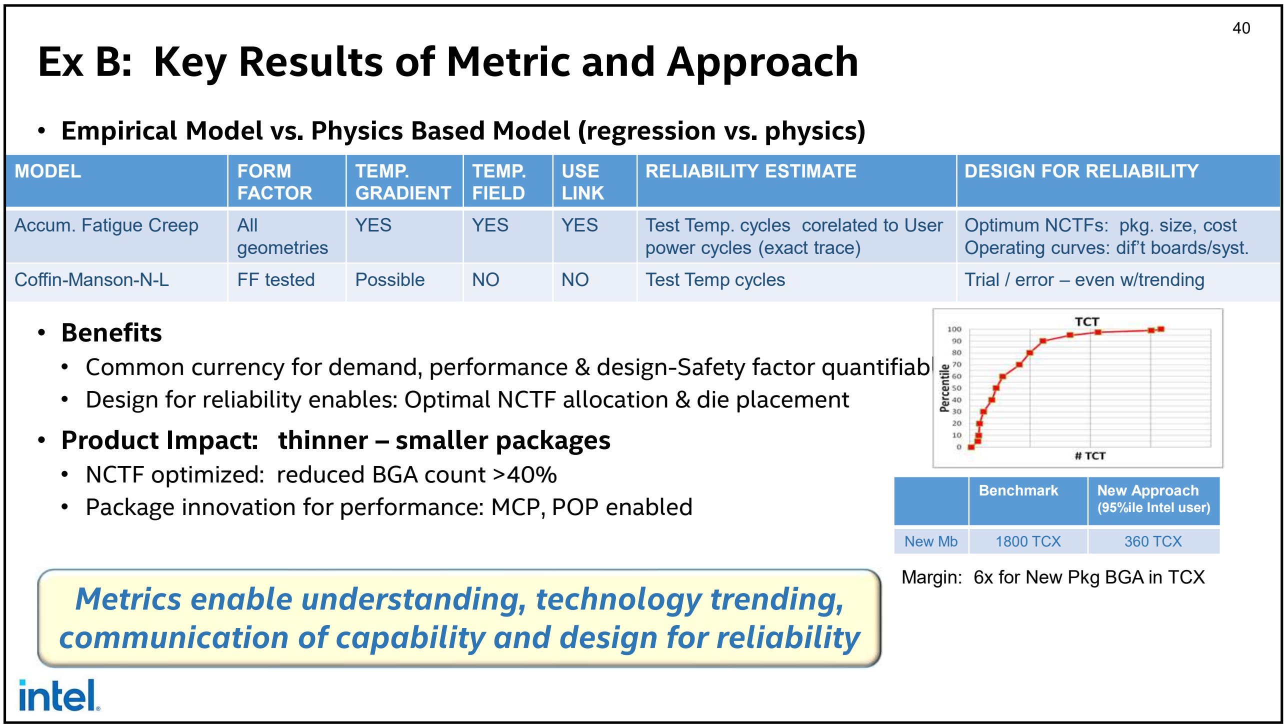
SJ damage vs. User population distribution

MTTF vs. AFC
UC-Profile & TC test

TC requirement vs. User population distribution

Translation: N cyc.
TC = TC level
TC = PC

M. Pei, R.Han, K.Kwon, A.Lucero, IEEE Elec. Components Tech. Conf. ECTC, 2013
R.Han, M.Pei, A.Luceo, D.Kwon, Y.Ge, P.Bhatti, T.Zheng, IEEE Elec. Components Tech. Conf. ECTC, 2013



Ex B: Key Results of Metric and Approach

- **Empirical Model vs. Physics Based Model (regression vs. physics)**

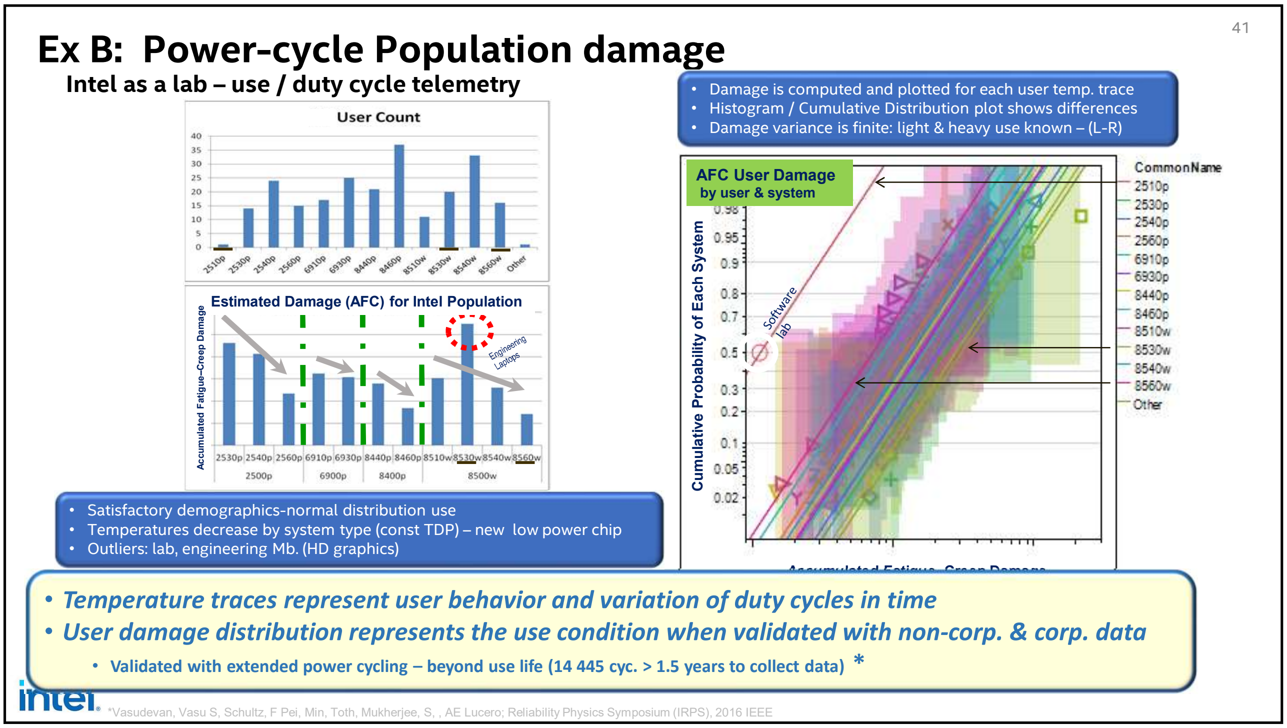
MODEL	FORM FACTOR	TEMP. GRADIENT	TEMP. FIELD	USE LINK	RELIABILITY ESTIMATE	DESIGN FOR RELIABILITY
Accum. Fatigue Creep	All geometries	YES	YES	YES	Test Temp. cycles corelated to User power cycles (exact trace)	Optimum NCTFs: pkg. size, cost Operating curves: dif't boards/syst.
Coffin-Manson-N-L	FF tested	Possible	NO	NO	Test Temp cycles	Trial / error – even w/trending

- **Benefits**
  - Common currency for demand, performance & design-Safety factor quantifiabl
  - Design for reliability enables: Optimal NCTF allocation & die placement
- **Product Impact: thinner – smaller packages**
  - NCTF optimized: reduced BGA count >40%
  - Package innovation for performance: MCP, POP enabled

	Benchmark	New Approach (95%ile Intel user)
New Mb	1800 TCX	360 TCX

Margin: 6x for New Pkg BGA in TCX

Metrics enable understanding, technology trending, communication of capability and design for reliability



Ex B: Power-cycle Population damage

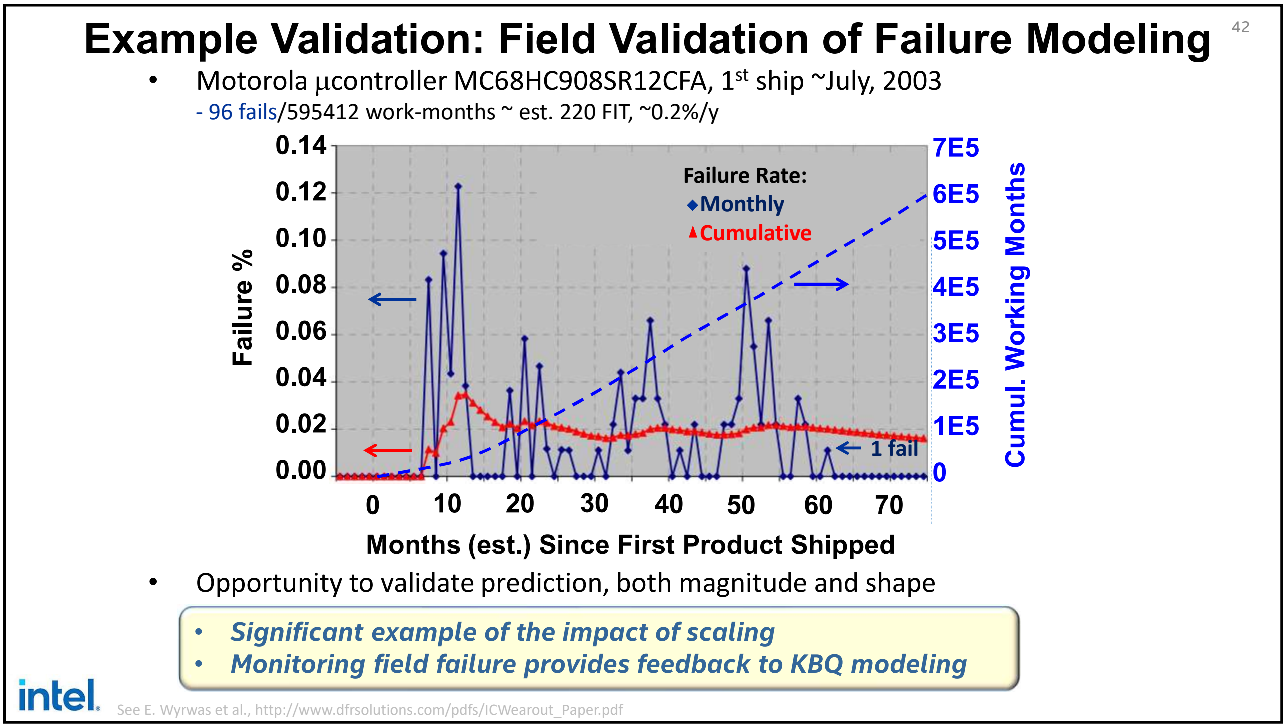
Intel as a lab – use / duty cycle telemetry

- Damage is computed and plotted for each user temp. trace
- Histogram / Cumulative Distribution plot shows differences
- Damage variance is finite: light & heavy use known – (L-R)

- Satisfactory demographics-normal distribution use
- Temperatures decrease by system type (const TDP) – new low power chip
- Outliers: lab, engineering Mb. (HD graphics)

- ***Temperature traces represent user behavior and variation of duty cycles in time***
- ***User damage distribution represents the use condition when validated with non-corp. & corp. data***
  - **Validated with extended power cycling – beyond use life (14 445 cyc. > 1.5 years to collect data)** *

*Vasudevan, Vasu S, Schultz, F Pei, Min, Toth, Mukherjee, S, , AE Lucero; Reliability Physics Symposium (IRPS), 2016 IEEE



Example Validation: Field Validation of Failure Modeling

- Motorola µcontroller MC68HC908SR12CFA, 1st ship ~July, 2003
  - 96 fails/595412 work-months ~ est. 220 FIT, ~0.2%/y

- Opportunity to validate prediction, both magnitude and shape

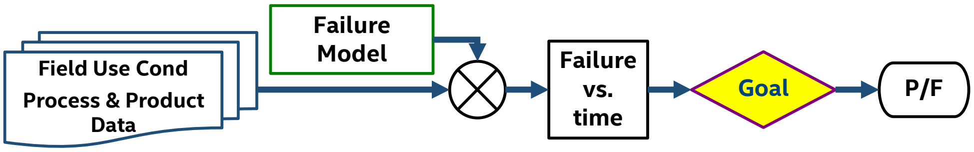
- ***Significant example of the impact of scaling***
- ***Monitoring field failure provides feedback to KBQ modeling***

See E. Wyrwas et al., http://www.dfrsolutions.com/pdfs/ICWearout_Paper.pdf

Knowledge-Based Qualification (KBQ)

A Definition: Using **knowledge of failure** mechanisms to adjust qualification to better meet customers' quality & reliability needs:

1) Adjust standard stress time to represent customer need
   - Increase (cover risk) or decrease (reduce cost and qual time)
2) Create unique stresses to expose specific mechanism
   - Ex: JESD22-A117A, non-volatile memory data patterns
3) Predict field failure to better meet customer expectations
   - Most needed for extremes of environment, usage or design



Failure Model

Field Use Cond
Process & Product Data

Failure vs. time

Goal

P/F

KB methods are discussed in standards body & other docs

See JEDEC JESD 94 & JEP 148 and Sematech 00053958A-XFR & 99083810A-XFR

Dynamic mechanical loading:

Highly Accelerated Life Test

(or Reliability Test ?)

Metric: Stress
External → Internal
Use condition → Test
Internal → External Demand
Test → Use condition

Highly Accelerated Life Test (HALT) / Stress Screen (HASS)

more than Failure Oriented Testing

- STRESS +

Lower Destruction | Destruction | Destruction | Upper Destruction
|------- Limit --|--|----- margin ---|--|---- margin ----|--|--- Limit ------|

HASS
Burn-in (T/V), Temp. cycle (ΔT) |-- Highly Accelerated Stress Screen --| Apply stimulus/stress to margin
(target weakness – knowledge)

HALT
HALT (ΔT +Vibe), Thermal shock --------------- **Highly Accelerated Life Test** --------------Apply stimulus in destructive zone
Mechanical drop* (benchmark, discovery – guess)

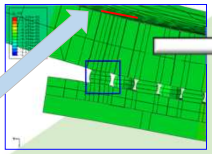
HALT applies a demand, not a stress
HALT identifies a threshold, not a strength
Is HALT useful to compare different designs (geometries) without knowledge?

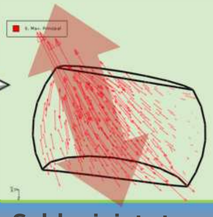
Solder Joint Dynamic Load

Translation

System Level – Use Condition
DEMAND

Component level
TESTING

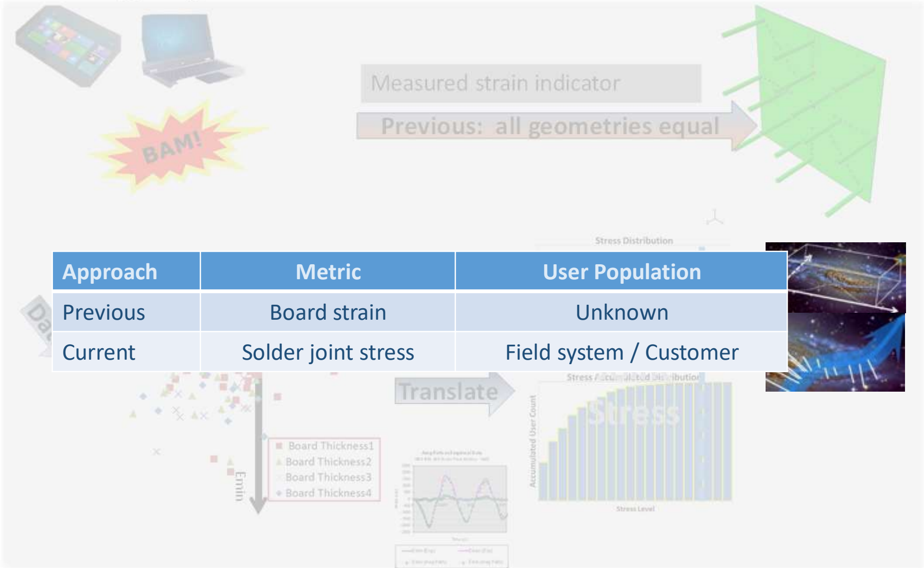




Board Bending:
strain

Solder joint stress:
dynamic FEM model

Dynamics: Legacy Benchmark vs. Metric Based



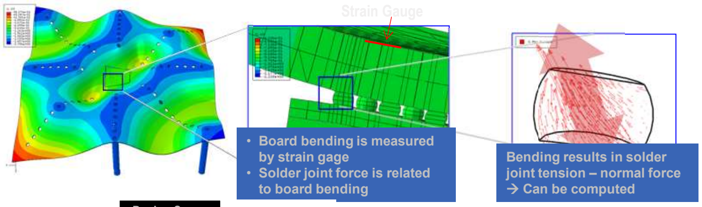
Approach	Metric	User Population
Previous	Board strain	Unknown
Current	Solder joint stress	Field system / Customer

A. Keynote: Predictive Modeling and Drop/Shock Tests for Reliability Assessment of Lead-Free BGA Structures, M Vujosevic, A Lucero, IEEE ASTR 2008
B. Use condition based qualification of BGA components, A. Lucero V. Kulkarni, M. Pei, P. Bhatti, IEEE ESTC 2013
C. Keynote: Use Condition Based BGA Shock Reliability Development, Vijay Kulkarni, Pardeep Bhatti, Min Pei, ASME, 2008.

BGA Solder Joint Stress: Reliable Operating Map

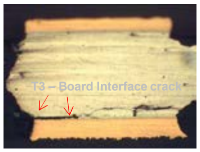
- **Average solder joint stress at the interface is a correlated failure metric**
  - Most common failure mode on board side for FCBGA packages
  - Failure & location depends on:
    - board strength, modulus, thickness, pad geometries, resin under the pad

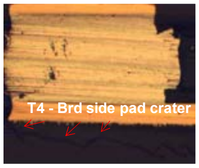
BOARD/PKG DEFORMATION **PKG BENDING** **SOLDER JOINT LOADING**



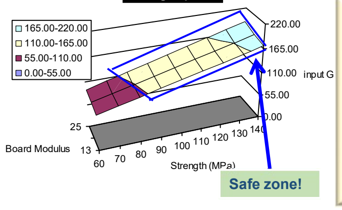
- Board bending is measured by strain gage
- Solder joint force is related to board bending

Bending results in solder joint tension – normal force → Can be computed





Design Space



Safe zone!

Shock Performance Modulators:
- Materials: board, component stiffness   (time/temp. dependent E for HALT)
- Geometry: pad size, layout
- Board quality: intrinsic strength and repeatability

Knowledge of the expected use condition and metric enables Design for Reliability & Guidance Measurement

Summary & Conclusions

- **Overview of the elements required for probabilistic design for reliability was shared**
  - Failure oriented accelerated testing
  - Physics of Failure models and metrics
  - Concepts of statistics that can be applied to all models and predictions
- **Examples of the use of the methods were shown from FOAT to prediction**
- **Comparisons of knowledge – based qualification and application specific qual. were shown**
- **Discussion on Highly Accelerated Stressing benefits, limitations and approaches**
- **Integration of SiPh and optics on to packaging will follow the same process**

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Acknowledgements: collaborative / self-reinforcing innovation

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- **Wade Hazeltine**
- **Zack Eckbladt**
- **Pramode Malakar**
- **Yun Ge**
- **Helia Rahmani**
- **Kevin Semenuk**
- **Shaw Fong Wong**
- **Vasu Vasudevan**
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- **Emre Armagan**
- **Richard Harries**
- **Daeil Kwon**
- **Sibashish Mukherjee**
- **Robert Kwasnik**

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Certification / Qual. Methods Comparison

AREA	STANDARDS	KNOWLEDGE BASED
Rel. Models	Fixed model & Parameters	Failure Physic Parameter Characterized
Failure distribution	scale/μ implied by sampling	Physics/design rule specific w/defects
Lifetime	10 yr.	Market specific
Goal	Zero Defect: 1% / 10k rDPM FIT – linear time	Market or Physics specific Non-linear in time – true
Metric	Test duration	Physics metric ∝ reliability life estimate
Rel. Test	Singe condition tested	Many - report to standard test condition
Output	0 fails infer reliability	Margins characterized
Investments	None	Invest in ongoing knowledge, assessments and estimation
Histor	[illegible]	[illegible]

- **Method may align to technology or change**
- **KBQ – most appropriate for new technologies**
- **Metrics for reliability are different**